

No. 25-_____

**IN THE UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT**

**IN RE SANDISK TECHNOLOGIES, INC. and WESTERN DIGITAL
TECHNOLOGIES, INC.,**

Petitioners.

PETITION FOR A WRIT OF MANDAMUS

**On Petition for a Writ of Mandamus to the United States Patent and
Trademark Office, Patent Trial and Appeal Board, in
Nos. IPR2025-00515, IPR2025-00516, IPR2025-00517**

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CERTIFICATE OF INTEREST

Case Number	TBD
Short Case Caption	In re Sandisk Technologies, Inc. and Western Digital Technologies, Inc.
Filing Party/Entity	Sandisk Technologies, Inc.; Western Digital Technologies, Inc.

Instructions: Complete each section of the form. In answering items 2 and 3, be specific as to which represented entities the answers apply; lack of specificity may result in non-compliance. **Please enter only one item per box; attach additional pages as needed and check the relevant box.** Counsel must immediately file an amended Certificate of Interest if information changes. Fed. Cir. R. 47.4(b).

I certify the following information and any attached sheets are accurate and complete to the best of my knowledge.

Date: September 17, 2025

Signature: /s/ Debra J. McComas

Name: Debra J. McComas

1. Represented Entities. Fed. Cir. R. 47.4(a)(1).	2. Real Party in Interest. Fed. Cir. R. 47.4(a)(2).	3. Parent Corporations and Stockholders. Fed. Cir. R. 47.4(a)(3).
Provide the full names of all entities represented by undersigned counsel in this case.	Provide the full names of all real parties in interest for the entities. Do not list the real parties if they are the same as the entities.	Provide the full names of all parent corporations for the entities and all publicly held companies that own 10% or more stock in the entities.
<u> </u> None/Not Applicable	<u> X </u> None/Not Applicable	<u> </u> None/Not Applicable
Sandisk Technologies, Inc.		Sandisk Corporation
Western Digital Technologies, Inc.		Western Digital Corporation

4. Legal Representatives. List all law firms, partners, and associates that (a) appeared for the entities in the originating court or agency or (b) are expected to appear in this court for the entities. Do not include those who have already entered an appearance in this court. Fed. Cir. R. 47.4(a)(4).

<u>None/Not Applicable</u>		<u>Additional pages attached</u>
David M. O'Dell (Haynes and Boone, LLP)	Hong Shi (Haynes and Boone, LLP)	Calmann J. Clements (Haynes Boone, LLP)

5. Related Cases. Other than the originating case(s) for this case, are there related or prior cases that meet the criteria under Fed. Cir. R. 47.5(a)?

X Yes (file separate notice; see below) No N/A (amicus/movant)

If yes, concurrently file a separate Notice of Related Case Information that complies with Fed. Cir. R. 47.5(b). **Please do not duplicate information.** This separate Notice must only be filed with the first Certificate of Interest or, subsequently, if information changes during the pendency of the appeal. Fed. Cir. R. 47.5(b).

6. Organizational Victims and Bankruptcy Cases. Provide any information required under Fed. R. App. P. 26.1(b) (organizational victims in criminal cases) and 26.1(c) (bankruptcy case debtors and trustees). Fed. Cir. R. 47.4(a)(6).

<u>X</u> None/Not Applicable		<u>Additional pages attached</u>

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STATEMENT OF RELATED CASES

The three patents at issue in these *inter partes* review (“IPR”) proceedings (U.S. Patent Nos. 9,183,085, 8,601,346, and 8,554,968) are being asserted in *Polaris PowerLED Technologies, LLC v. Western Digital Corp.*, No. 2:24-cv-02864 (C.D. Cal.) (filed Apr. 9, 2024). That case is currently stayed.

RELIEF SOUGHT

Sandisk Technologies, Inc. and Western Digital Technologies, Inc. (“Petitioners”) respectfully request a writ vacating the non-institution decisions in IPR2025-00515, IPR2025-00516, and IPR2025-00517.¹ The Court should direct the USPTO to reconsider institution solely under the statutory criteria, not the agency’s extra-statutory framework. At a minimum, the Court should direct the USPTO to reconsider institution without the USPTO’s new “settled expectations” rule and solely under the guidance in place when the petitions were filed.

¹ Petitioners are challenging all three denials in a single mandamus petition because the USPTO issued a single decision for all three IPRs, the denials were substantively identical, and the relief requested here is the same.

INTRODUCTION

Mandamus is available in extraordinary circumstances, and the USPTO's assertion of unbridled authority over IPR institution is extraordinary. Here, the USPTO denied institution based on a rule that "old" patents gain "settled expectations" that immunize them from IPR. That rule is lawless on every level. It is not found in any statute. It did not exist when Petitioners filed their IPR petitions. And it was imposed without notice-and-comment regulation.

This "settled expectations" rule has dramatically transformed IPR practice. For the past thirteen years since IPR's inception in 2012, all patents were equally eligible for IPR no matter their age. After all, Congress designed IPR with no deadline for "old" patents. Consistent with that framework, the USPTO regularly instituted IPR and canceled claims for patents of every vintage, including "old" patents. But everything changed this year. Out of nowhere, the Acting Director began denying institution because patents were too "old." In just two months, the USPTO denied 64 IPR petitions on that ground—despite the USPTO's consistent, *decade-plus* practice to the contrary, instituting and resolving IPRs in 2,269 cases with similarly "old" patents.² Now, would-be petitioners must scour newly issued patents, predict

²Jonathan DeFosse et al., *Data Undermines USPTO's 'Settled Expectations' Doctrine*, Law360 (Aug. 29, 2025), *available at* <https://www.law360.com/articles/2381350>

which might someday be asserted against them (however baselessly), then launch pre-emptive IPR challenges in the first few years of the patent’s life—or forfeit their statutory rights to seek IPR.

That rule would be news to Congress, which enacted the AIA without any “old”-patent limit on IPR. It was certainly news to Petitioners, who filed their IPR petitions before the “settled expectations” rule abruptly appeared. Yet the USPTO applied that new rule to Petitioners post-hoc—after they already paid to have their petitions reviewed under the old standards, and after the window for challenging these patents under the new rule had long closed.

And this is only the latest twist in the USPTO’s dizzying reconstruction of its institution authority. Over the past few months, the Acting Director has replaced preexisting institution rules with an unpredictable flurry of new ones—all without notice and comment. These novel, erratic, demanding hurdles have already drawn at least four other mandamus challenges.³

(Appx699-703).

³ *In re SAP America, Inc.*, No. 25-132 (Fed. Cir., filed June 16, 2025); *In re Motorola Solutions, Inc.*, No. 25-134 (Fed. Cir., filed June 23, 2025); *In re Google LLC, et al.*, No. 25-144 (Fed. Cir., filed Aug. 18, 2025); and *In re HighLevel, Inc.*, No. 25-148 (Fed. Cir., filed Aug. 29, 2025).

Now the USPTO has gone even further, inventing a retroactive “settled expectations” rule and disregarding legal limits along the way. The agency violated due-process anti-retroactivity constraints. It transgressed APA limits on retroactive regulation and requirements of reasoned decisionmaking. It ignored APA notice-and-comment obligations. And most fundamentally, it exceeded the power Congress gave it, by inventing an extra-statutory “settled expectations” rule—violating the APA and the Constitution’s separation of powers.

While 35 U.S.C. §314(d) generally bars appeals attacking institution determinations in “ordinary” case-specific “dispute[s],” §314(d) does not bar review of agency “shenanigans,” including rulings that violate constitutional rights or exceed statutory authority. *Cuozzo Speed Techs. v. Commerce for Intellectual Prop.*, 579 U.S. 261, 271, 274-75 (2016). The retroactive “settled expectations” rule, unilaterally created from thin air, is a prototypical “shenanigan” requiring judicial redress. Mandamus is the sole mechanism available to obtain that relief, and the Court should grant this petition.

ISSUES PRESENTED

1. Did the USPTO violate due process by applying its “settled expectations” rule post-hoc to pre-filed petitions?

2. Did the USPTO violate the APA by applying its “settled expectations” rule post-hoc, without authority and without considering relevant concerns?

3. Did the USPTO violate the APA and AIA by skipping notice-and-comment procedures for its “settled expectations” rule—a new IPR limit determining stakeholder rights?

4. Did the USPTO exceed its authority—violating the APA and the Constitution’s separation of powers—by inventing an extra-statutory “settled expectations” rule for “old” patents?

BACKGROUND

I. Congress established IPR, and the USPTO created its own IPR institution criteria without notice and comment.

In enacting the AIA, Congress believed “questionable patents” were “too easily obtained” and “too difficult to challenge.” H.R. Rep. No. 112-98, at 39-40 (2011). It therefore established IPR, allowing anyone to petition the USPTO to conduct a limited review of granted patents. 35 U.S.C. §311. In the first 9 months of a patent’s life, a different form of USPTO review is available: post-grant review (PGR). §§321-329. From then on (after 9 months, and after PGR terminates), Congress made patents eligible for IPR—with no maximum patent age. §311(c).

To decide whether to institute an IPR, Congress instructed the Director to determine whether “there is a reasonable likelihood that the petitioner would

prevail.” §314(a). Congress further instructed the Director to “prescribe regulations” providing “the standards” for “showing” “sufficient grounds to institute a review under section 314(a).” §316(a)(2).

The USPTO repeatedly began—and abandoned—the notice-and-comment process to “prescribe regulations.” *Id.* In 2023, it issued an advance notice of proposed rulemaking. 88 Fed. Reg. 24,503 (Appx26-41). In 2024, it issued a notice of proposed rulemaking. 89 Fed. Reg. 28,693 (Appx42-55). In 2025, it reiterated plans “to pursue notice-and-comment rulemaking.” Theresa Schliep, *Patent Office Plans Rulemaking For New PTAB Denial Process*, Law360, <https://www.law360.com/articles/2324147> (Apr. 17, 2025). But these false-starts are the sum total of the USPTO’s efforts. No actual notice-and-comment regulation has issued.

Instead, the USPTO has resorted to “precedential” decisions and “guidance” documents. In this process, it designated as precedential the *Fintiv* factors, governing IPR institution in the face of parallel district-court litigation. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, 2020 WL 2126495, at *2 (PTAB Mar. 20, 2020) (precedential). It then “issue[d] binding agency guidance” governing institution, reaffirming the *Fintiv* factors. Appx19 (Memorandum from USPTO Director to PTAB, *Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with*

Parallel District Court Litigation (June 21, 2022) (Appx17-25)). At the same time, it announced limits on its own discretion: “the PTAB will not discretionarily deny institution in view of parallel district court litigation” if a petitioner “stipulat[es] not to pursue in a parallel proceeding” grounds “that could have reasonably been raised before the PTAB.” Appx19 (a so-called “*Sotera* stipulation”). These were the rules in place when Petitioners filed their IPR petitions.

II. Petitioners filed IPR petitions.

In 2024, non-practicing entity Polaris PowerLED Technologies sued Western Digital Corporation and Western Digital Technologies, Inc., alleging infringement of three patents concerning memory systems (U.S. Patent Nos. 8,554,968; 8,601,346; and 9,183,085). Appx248-307.

In January 2025, Petitioners—Western Digital Technologies, Inc. and former-subsidiary⁴ Sandisk Technologies, Inc.—filed IPR petitions challenging those patents. They paid \$71,250 in non-refundable filing fees (Appx8, Appx12, Appx16 (receipts)) and incurred substantial costs preparing the petitions and supporting declarations.

⁴ Sandisk Corporation, Annual Report (Form 10-K) (Aug. 20, 2025), *available at* <https://investor.sandisk.com/static-files/342a38e2-e204-4f50-ad22-3e3a28e2f6ff>.

Western Digital immediately sought a litigation stay pending the IPRs, which the court granted. Appx313-321. Consistent with USPTO guidance, Western Digital also submitted a *Sotera* stipulation, agreeing not to litigate any grounds raised or that could reasonably have been raised in any instituted IPR. Appx308-312.

III. After the IPR petitions were filed, and without notice and comment, the USPTO invented a new, evolving “settled expectations” rule.

After Petitioners’ filings, the USPTO upended its existing institution criteria with a stream of new pronouncements. In February 2025, the USPTO rescinded the 2022 guidance in a website post. Appx56-57. On March 24, the Chief Administrative Patent Judge issued a memo with new institution rules. Appx58-60. Two days later, the Acting Director issued another memo with more new rules. Appx61-63. That memo announced a new “discretionary consideration”: the parties’ “[s]ettled expectations,” “such as the length of time the claims have been in force.” Appx62. The memo explained nothing further about that factor, like what “length of time” qualifies or what connection this has to the AIA. These official actions were taken without notice-and-comment rulemaking, despite the USPTO’s statutory obligations and repeated earlier commitments to pursue that path.

In June, again without notice and comment, the Acting Director denied IPR institution for the first time on the ground that “the challenged patent has been in force” too long, “creating settled expectations.” *Dabico Airport Sols. Inc. v. AXA*

Power ApS, IPR2025-00408, Paper 21, at 2 (AD June 18, 2025) (Appx64-68); *see id.* at 3 (“the longer the patent has been in force, the more settled expectations should be”). She further declared this rule applies irrespective of “actual notice of a patent or of possible infringement.” *Id.*

This rule prompted an immediate rash of institution denials (with an emerging pattern roughly tracking a patent’s six-year mark). *See* Appx697 (article)⁵; *e.g.*, *Cambridge Indus. USA, Inc. v. Applied Optoelectronics, Inc.*, IPR2025-00433, 2025 WL 1773382 (AD June 26, 2025) (seven- and nine-year-old patents had “strong settled expectations” but five- and six-year-old patents did not); *Amazon.com, Inc. v. VirtaMove, Corp.*, IPR2025-00561, 2025 WL 1913383 (AD July 11, 2025) (“settled expectations” sole reason justifying denial).⁶

⁵ Ryan Davis, *Stewart Says New Patent Policies Aim to Bring Stability*, Law360 (Sept. 8, 2025), *available at* <https://www.law360.com/articles/2364638/stewart-says-new-patent-policies-aim-to-bring-stability> (Appx696-698).

⁶ Here are further examples (without including the dozens more post-dating the decision here): *Sig Sauer Inc. v. Lone Star Future Weapons*, IPR2025-00410, 2025 WL 1773118 (AD June 26, 2025); *Samsung Elecs. Co. v. Sinotechnix LLC*, IPR2025-00331, 2025 WL 1836417 (Acting Deputy Chief APJ July 2, 2025); *Apotex Inc. v. Alkermes Pharma Ireland Ltd.*, IPR2025-00514, 2025 WL 1853593 (AD July 2, 2025); *Samsung Elecs. Co. v. Mobile Data Techs., LLC*, IPR2025-00535, 2025 WL 1908154 (Acting Deputy Chief APJ July 10, 2025); *NXP USA, Inc. v. Redstone Logics LLC*, IPR2025-00485, 2025 WL 1909554 (AD July 10, 2025); *SAP Am., Inc. v. Valtrus Innovs. Ltd.*, IPR2025-00414, 2025 WL 1909114 (AD July 10, 2025); *Caihong Display Devices v. Corning, Inc.*, IPR2025-00439, 2025 WL 1912302 (AD July 10, 2025); *Google LLC v.*

The agency now updates its institution guidance on a rolling basis through a website.⁷

IV. The USPTO denied institution here based solely on “settled expectations.”

In mid-July, the Acting Director rejected Petitioners’ IPR petitions articulating a single justification: “settled expectations.” She repeated standard boilerplate that her “determination” considered “a holistic assessment” and she did not find “persuasive” Petitioners’ view that IPR was “an appropriate use of Board resources.” Appx2. But she identified only a single concrete consideration favoring denial: “the challenged patents have been in force for approximately nine, twelve, and twelve years, creating strong settled expectations.” Appx2. Despite admitting that the agency’s prior *Fintiv* guidance supported review (because the litigation “ha[d] been stayed”), she never justified departing from that standard and imposing the agency’s new “settled expectations” rule on these IPR petitions retroactively.

VirtaMove, Corp., IPR2025-00487, 2025 WL 1913566 (AD July 11, 2025); *Kingston Tech. Co. v. Vervain, LLC*, IPR2025-00614, 2025 WL 1953666 (AD July 16, 2025); *Analog Devices, Inc. v. Number 14 B.V.*, IPR2025-00550, 2025 WL 1953257 (AD July 16, 2025); *Kangxi Commc’n Techs. v. Skyworks Sols., Inc.*, IPR2025-00372, 2025 WL 1959071 (AD July 16, 2025).

⁷ See Interim Director Discretionary Process, USPTO.gov, *available at* <https://www.uspto.gov/patents/ptab/interim-director-discretionary-process>.

STANDARD OF REVIEW

This Court has “jurisdiction to review any petition for a writ of mandamus denying institution of an IPR.” *Mylan Labs. Ltd. v. Janssen Pharmaceutica, N.V.*, 989 F.3d 1375, 1381 (Fed. Cir. 2021). A petitioner must show “a clear and indisputable legal right,” the lack of “other adequate method of obtaining relief,” and the writ’s “appropriate[ness]” “under the circumstances.” *Id.* at 1382.

REASONS WHY THE WRIT SHOULD ISSUE

I. The USPTO’s errors are clear and indisputable.

A “reviewing court shall” “hold unlawful and set aside agency action” that is “arbitrary, capricious, an abuse of discretion, or otherwise not in accordance with law,” “contrary to constitutional right, power, privilege, or immunity,” “in excess of statutory jurisdiction, authority, or limitations,” or “without observance of procedure required by law.” 5 U.S.C. §706(2). On four independent grounds, the USPTO’s “settled expectations” rule here was unlawful and must be set aside: (1) its retroactive application violated due process; (2) its retroactive application exceeded statutory authority and was arbitrary and capricious; (3) the agency ignored notice-and-comment procedures; and (4) the new institution criterion exceeds statutory authority and the agency’s constitutional power.

A. The USPTO violated due process by retroactively applying a new bar to these IPR petitions.

According to the USPTO, the “settled expectations” rule barred these IPRs because the patents were too “old.” But that restriction did not exist when the petitions were filed. Instead, by the time the USPTO sprung the rule on Petitioners, it was far too late to satisfy the rule by (somehow) petitioning when the patents were younger. And it was too late for them to recover the \$71,250 in filing fees they wasted (unaware each petition was now futile under a theretofore-unannounced rule).

The USPTO’s retroactive application of the “settled expectations” rule flouts due process. “Retroactivity is not favored in the law.” *Princess Cruises, Inc. v. United States*, 397 F.3d 1358, 1362 (Fed. Cir. 2005) (citation omitted). “The Due Process Clause limits the extent to which the Government may retroactively alter the legal consequences of an entity’s or person’s past conduct.” *PHH Corp. v. CFPB*, 839 F.3d 1, 46-47 (D.C. Cir. 2016) (Kavanaugh, J.), *order vacated* (Feb. 16, 2017), *reinstated in relevant part*, 881 F.3d 75, 83 (D.C. Cir. 2018). “Due process therefore requires agencies to ‘provide regulated parties fair warning of the conduct a regulation prohibits or requires.’” *Id.* (citation omitted). And “an administrative agency may not apply a new rule retroactively when to do so would unduly intrude upon reasonable reliance interests.” *Heckler v. Cmty. Health Servs. of Crawford Cnty., Inc.*, 467 U.S. 51, 61 n.12 (1984).

This Court, applying the “retroactivity doctrine,” examines the “‘nature and extent of the change in the law,’ ‘the degree of connection between the operation of the new rule and a relevant past event,’ and ‘familiar considerations of fair notice, reasonable reliance, and settled expectations.’” *Princess Cruises*, 397 F.3d at 1362, 1364 (quoting *Landgraf v. USI Film Prods.*, 511 U.S. 244, 270 (1994)). “If, under this test, a rule or regulation appears to have a retroactive effect, then the rule or regulation cannot be applied to cases pending at the time of its promulgation.” *Rodriguez v. Peake*, 511 F.3d 1147, 1153 (Fed. Cir. 2008).

For example, in *Princess Cruises*, this Court held it impermissible to apply an agency ruling to conduct preceding the ruling (which imposed a new standard governing cruise-ship taxes and a new evidentiary presumption). 397 F.3d at 1363-67. The new ruling qualified as a significant change in law because it established an evidentiary presumption “nowhere to be found in” the “statute or regulations.” *Id.* at 1365. The ruling disadvantaged parties for past conduct: cruise lines had not kept records to meet the new evidentiary presumption. *Id.* at 1366. And it would have been unfair to apply the new rule too late for parties to change their behavior to comply. *Id.*⁸

⁸ In *Princess Cruises*, the agency also sent the party a letter indicating that one rule would apply before imposing a new one retroactively. 397 F.3d at 1366. But that fact

Similarly, a “new rule concerning the filing of complaints would not govern an action in which the complaint had already been properly filed under the old regime.” *Landgraf*, 511 U.S. at 275 & n.29. So too for a new limit on notices of appeal “if it would render invalid a notice that was valid when filed.” *Durr v. Nicholson*, 400 F.3d 1375, 1380 (Fed. Cir. 2005); *see also Woodward v. DOJ*, 598 F.3d 1311, 1315 (Fed. Cir. 2010) (new burden of proof cannot be applied to already-pending case).

The USPTO violated those anti-retroactivity principles here. It did just what the Supreme Court and this Court have denounced: imposing a new constraint on already-filed IPR petitions (just like complaints or notices of appeal) is impermissible. *See Landgraf*, 511 U.S. at 275; *Durr*, 400 F.3d at 1380.

Applying the “settled expectations” rule here flunks every prong of this Court’s retroactivity framework. To begin, a “settled expectations” rule is “nowhere to be found in” the “statutes or regulations” and thus effects a significant change in law. *Princess Cruises*, 397 F.3d at 1365.

was not essential; even without it, retroactive application was unlawful. *Carnival Cruise Lines, Inc. v. United States*, 404 F.3d 1312, 1319 (Fed. Cir. 2005). And the entire point of public agency guidance is to assure regulated stakeholders what to expect; the USPTO’s surprise retroactive shift here is just as invalid as in *Princess Cruises* and *Carnival Cruise Lines*.

Next, applying this change disadvantaged Petitioners for past events. *See id.* at 1366. The USPTO’s “settled expectations” rule penalizes them for not petitioning for IPR sooner, before the patents gained “settled expectations.” Yet Petitioners had no idea they needed to do this. To the contrary, as in *Princess Cruises*, there was a “common [industry] understanding” that parties “had no need to” do what the agency’s new rule required. *Id.*

The resulting unfairness is obvious. Had Petitioners known the rule—that the patents’ age would immunize them from IPR—they could have behaved differently. To meet the USPTO’s rule, Petitioners could have searched for these patents and petitioned for IPR years earlier. Petitioners alternatively could have offered to purchase the patents. And certainly, they would not have filed futile IPR petitions, expending over \$71,250 in unrecoverable funds.

The USPTO’s surprise new rule also destroyed reasonable reliance interests. Petitioners detrimentally relied on the institution standards existing when they filed for IPR. Under those standards, the petitions were meritorious. The USPTO’s decision shows as much: it mustered no reason for denying institution besides the new “settled expectations” rule. Appx2. The USPTO even acknowledged the *Fintiv* inquiry *supported* institution (because parallel litigation was already stayed). *Id.*; *see Fintiv*, 2020 WL 2126495, at *2-3. Petitioners had an especially strong expectation

that those pre-existing standards would hold, because the USPTO had repeatedly indicated that any change would come through notice-and-comment rulemaking—and the proposed rules never mentioned “settled expectations.” *See supra* 7; 88 Fed. Reg. 24,503 (Appx26-41) (discussing institution discretion and stating “USPTO intends to make policy changes through notice-and-comment rulemaking”); 89 Fed. Reg. 28,693 (Appx42-55) (proposing rules for institution discretion).

The USPTO attempted no explanation for applying the “settled expectations” rule retroactively, either in its decision here or in the earlier decision it cited. Appx2; *Dabico*, IPR2025-00408, Paper 21, at 2-3 (Appx65-66). Nor is any such justification possible. It is unreasonable to induce payment of \$71,250 in filing fees by announcing one set of institution standards, only then to deny petitions under a harsher standard.

All that is more than enough to establish a violation of due-process anti-retroactivity principles. *Princess Cruises*, 397 F.3d at 1362; *Rodriguez*, 511 F.3d at 1153. No analysis of other due-process frameworks is necessary. *GPX Int’l Tire Corp. v. United States*, 780 F.3d 1136, 1141 (Fed. Cir. 2015) (when party challenges a law “because it operates retroactively,” “we do not think that the outcome of the due process analysis depends upon a determination that a vested right exists”).

But for good measure, other frameworks point the same way. The USPTO impaired protected interests. Money is property, and Petitioners lost property—sizeable filing fees—they would not have surrendered had they known of the USPTO’s new rule. And the USPTO subverted their property and liberty interests in having their petitions adjudicated fairly under the then-existing standards. *See Logan v. Zimmerman Brush Co.*, 455 U.S. 422, 429-30 (1982) (“[The] Due Process Clause has been interpreted as preventing the States from denying potential litigants use of established adjudicatory procedures, when such an action would be the equivalent of denying them an opportunity to be heard upon their claimed rights.” (citation and alterations omitted)). Petitioners received no notice or opportunity to be heard “at a time when the deprivation c[ould] still be prevented” —that is, before filing the IPR petitions. *Fuentes v. Shevin*, 407 U.S. 67, 81 (1972). Whether assessed as a deprivation of property and liberty without notice and opportunity to be heard, or as a violation of anti-retroactivity doctrine, the use of the “settled expectations” rule here was impermissibly retroactive.

B. The USPTO violated the APA by retroactively applying the “settled expectations” rule without authority or reasoned decisionmaking.

Retroactively applying the “settled expectations” rule also violated bedrock APA limits. The USPTO lacked statutory authority to regulate retroactively, 5

U.S.C. §706(2)(A)-(C), and in any event failed to consider crucial factors, §706(2)(A), (D).

An agency lacks “power to promulgate retroactive rules unless that power is conveyed by Congress in express terms.” *Bowen v. Georgetown Univ. Hosp.*, 488 U.S. 204, 208 (1988); *see Bd. of Cnty. Comm’rs of Weld Cnty. v. EPA*, 72 F.4th 284, 292 (D.C. Cir. 2023). The AIA confers no power—let alone in express terms—to make IPR rules retroactive. Yet the USPTO retroactively penalized Petitioners for noncompliance with a post-hoc rule in all the ways just discussed—including by requiring IPR filings years before the rule existed and refusing to give the petitions the consideration promised when they were filed. *Supra* 16-17.

The USPTO also acted arbitrarily and capriciously, ignoring its basic “mandate to engage in reasoned decisionmaking under the APA.” *In re Brunetti*, — F.4th—, 2025 WL 2446503, at *7-8 (Fed. Cir. Aug. 26, 2025) (precedential). Agencies must “develop coherent and rational rules” and “articulate a satisfactory explanation for [an] action including a rational connection between the facts found and the choice made.” *Id.* at 7 (citation and quotation marks omitted). Changing policy requires “provid[ing] a reasoned explanation for the change, display[ing] awareness that they are changing position, and consider[ing] serious reliance

interests.” *FDA v. Wages & White Lion Invs., L.L.C.*, 604 U.S. 542, 568 (2025) (citation and alterations omitted).

The USPTO failed to justify its post-hoc imposition of “settled expectations.” It never even attempted “a reasoned explanation” (*id.*) for imposing that new rule retroactively. *Supra* 17.

Indeed, it failed to address *any* relevant consideration. It never acknowledged that the rule did not exist before the IPR petitions were filed or before the patents grew too “old”—let alone “display[ed] awareness” of a changed position, *Wages & White Lion*, 604 U.S. at 568. It mentioned no effect on Petitioners or “reliance interests.” *Id.* It never articulated when “settled expectations” arise, leaving stakeholders to scour dozens of decisions to divine some pattern. *Brunetti*, 2025 WL 2446503, at *8 (agencies may not take “an ‘I know it when I see it’ approach”).

And the agency ignored a basic logical defect at the rule’s core. Patentees had no “settled expectation” that old patents were immune from challenge until the USPTO decreed it. Parties were always free to challenge a patent’s validity, no matter how old. Even today, that remains true in district-court litigation. So it is unclear how patentees could have developed “settled expectations” (and for IPRs alone). And it was impossible for Petitioners to anticipate that the USPTO would create such a rule and impose it retroactively.

The USPTO failed to confront any of that. It could not identify statutory authority or reasoned justification for imposing the new rule retroactively on Petitioners. It did not even try. That APA violation warrants mandamus.

C. The USPTO violated the APA and AIA by imposing a limitation on institution without notice-and-comment rulemaking.

The “settled expectations” rule violates another basic administrative-law requirement. Notice and comment “assure[s] fairness and mature consideration of rules of general application.” *NLRB v. Wyman-Gordon Co.*, 394 U.S. 759, 764 (1969). Agency action disregarding that procedural requirement must be set aside. *See, e.g., Coal. for Common Sense in Gov’t Procurement v. Sec’y of Veterans Affs.*, 464 F.3d 1306, 1317 (Fed. Cir. 2006). The “settled expectations” rule, imposed without notice-and-comment procedures, violates the APA and AIA and should be set aside.

The APA requires notice-and-comment rulemaking for substantive rules. 5 U.S.C. §553. The APA defines as a “rule” any “agency statement of general or particular applicability and future effect designed to implement, interpret, or prescribe law or policy.” §551(4). Substantive rules, but not “interpretative rules, general statements of policy, or rules of agency organization, procedure, or practice,” require notice and comment. §553(b). Rules are “substantive” if they

“effect a change in existing law or policy” or “affect individual rights and obligations.” *Paralyzed Veterans of Am. v. West*, 138 F.3d 1434, 1436 (Fed. Cir. 1998).

The USPTO’s “settled expectations” rule is a rule. It applies generally and prospectively to any IPR petition, and it implements and prescribes a concrete limit on IPR.

The rule is substantive many times over. To begin, it “change[s] existing law and policy,” *id.*, by introducing a never-seen-before IPR precondition. Indeed, the agency has been open about a new policy approach. Appx697 (announcing that the USPTO, under current leadership, “has focused on liberally permitting early challenges to patent validity” but believes “the longer a patent has been in force, the stronger and more settled the patent owner’s expectations should be”).

Moreover, the “settled expectations” rule affects patent challengers’ rights by creating a new ground for depriving opportunities to seek patent cancellation through IPR. The USPTO’s substantive judgment here that the patents engendered “settled expectations” worth preserving was its only reason for denying IPR. Appx2. Such a rule, which “affects the substantive . . . standards by which the [agency] examines a party’s application” is a substantive rule. *In re Chestek PLLC*, 92 F.4th 1105, 1109 (Fed. Cir. 2024); *see also Am. Hosp. Ass’n v. Bowen*, 834 F.2d 1037, 1046 (D.C. Cir. 1987) (establishing “factors for determining . . . eligibility” for relief is

“the classic example” of a substantive rule); *Pickus v. U.S. Bd. of Parole*, 507 F.2d 1107, 1112-13 (D.C. Cir. 1974); *AFL-CIO v. NLRB*, 57 F.4th 1023, 1041 (D.C. Cir. 2023); *Gen. Elec. Co. v. EPA*, 290 F.3d 377, 382-83 (D.C. Cir. 2002); *Reeder v. FCC*, 865 F.2d 1298, 1305 (D.C. Cir. 1989).

The rule’s substantive impact goes further still. It substantively affects patent owners and the public by establishing a category of “old” patents that are protected against IPR. It also overrides Congress’s substantive decisions not to impose a patent-age cap for IPR eligibility or a presumption of validity for older patents. And it affects challengers’ rights and obligations by requiring premature IPR challenges early in a patent’s life, or forfeiture of IPR rights.

On top of all that, the rule operated substantively especially because the USPTO imposed it retroactively. Notice and comment is required “[w]hen a rule prescribes a timetable for asserting substantive rights,” and “the time allotted is so short as to foreclose effective opportunity to make one’s case on the merits.” *Lamoille Valley R.R. Co. v. I.C.C.*, 711 F.2d 295, 328 (D.C. Cir. 1983). The rule here had the same effect. By creating a retroactive deadline to challenge patents that was impossible for IPR petitioners to meet, the USPTO foreclosed IPR petitioners’ opportunity to make their case on the merits. That is another substantive effect that required fair and thorough consideration via notice and comment. *Id.*

Finally, the AIA itself separately requires notice and comment in this specific context. The AIA commands that in “setting forth the standards for the showing of sufficient grounds to institute” IPR, the agency “shall prescribe regulations.” §316(a)(2); *see also* §312(a)(4) (requiring that requirements for IPR petitions, beyond those already enumerated in §312(a), be established “by regulation”). That means notice-and-comment rulemaking. “[W]hen a statute defines a duty in terms of agency regulations, those regulations are considered legislative rules,” which must be issued “pursuant to the [APA’s] notice-and-comment requirements.” *U.S. Telecom Ass’n v. FCC*, 400 F.3d 29, 38, 40 (D.C. Cir. 2005); *see MST Exp. v. Dep’t of Transp.*, 108 F.3d 401, 402 (D.C. Cir. 1997) (agency conceded that statute requiring prescribing standard “by regulation” requires notice-and-comment rulemaking). This was the backdrop against which Congress enacted §316(a). *Cf. Facebook, Inc. v. Windy City Innovations, LLC*, 973 F.3d 1321, 1350 (Fed. Cir. 2020) (“There is no indication in the [IPR] statute that Congress . . . intended [the Director] to engage in any rulemaking other than through the mechanism of prescribing regulations.”); *Aqua Prods., Inc. v. Matal*, 872 F.3d 1290, 1332 (Fed. Cir. 2017) (en banc) (Moore, J., concurring) (noting agreement among “majority” of en banc Court that where §316 “delegates to the Director the authority *to prescribe regulations* adopting standards, only notice and comment rulemaking by regulation

will be given *Chevron* deference”). The USPTO has no excuse for failing to follow this basic procedure.

The resulting chaos underscores the need for notice-and-comment rulemaking. Nobody knows whether “settled expectations” attach at year five or six; whether an IPR petition’s strength on the merits will matter; or whether today’s rules will apply tomorrow. The law demands more. The USPTO, like all agencies, must follow notice-and-comment procedures to ensure “fairness and mature consideration.” *Wyman-Gordon Co.*, 394 U.S. at 764.

D. The USPTO exceeded its authority—in violation of the APA and the Constitution—by inventing an IPR institution criterion untethered to the AIA.

The “settled expectations” rule’s most fundamental defect is that the USPTO lacks authority to create it at all. The AIA does not authorize the Director to invent institution criteria unmoored from the statute; and it certainly does not authorize a maximum-patent-age cap on IPR. In imposing the “settled expectations” rule, the USPTO exceeded its statutory authority and usurped Congress’s legislative power. 5 U.S.C. §706(2).

1. Congress did not empower the Director to create extra-statutory institution criteria.

Contrary to the USPTO’s belief, the Director does not have unfettered discretion at the institution stage. Congress outlined specific institution criteria for

the Director to consider. *E.g.*, §§314(a), 315(d), 325(d). It granted discretion in applying some of *those* criteria, as well as limited authority to promulgate “regulations” implementing *those* criteria, which the agency has failed to do (§316(a)(2)). But the USPTO instead believes the Director may invent *any* criteria she wishes—even with no basis in the AIA. *See* AD’s Resp., *In re Motorola Solutions*, No. 25-134, ECF No. 28 at 8 (Fed. Cir. Aug. 4, 2025) (institution “criteria” is “entirely within the Director’s discretion”). This is lawless. Congress did not legislate a reticulated framework for the USPTO to simply disregard. While this Court has occasionally assumed the Director has broad institution discretion, it has not squarely decided the bounds of that authority in the face of the arguments presented here. *E.g.*, *Mylan*, 989 F.3d at 1382; *Saint Regis Mohawk Tribe v. Mylan Pharms. Inc.*, 896 F.3d 1322, 1327 (Fed. Cir. 2018). This fundamental question needs a considered answer. This Court should confirm the Director’s power is limited by Congress’s design.

In the AIA, Congress instructed the agency to *apply* statutory requirements, not create new ones. It specified the core merits threshold in §314(a); it instructed parties to address the “requirement[s] *of this chapter*” (§313 (emphasis added)); and it set forth other reticulated considerations. Some are firm bars (§315(b)’s time limit and §315(e)’s estoppel). Some are discretionary considerations (§315(d)’s docket-

management authority and §325(d)’s anti-duplication authority). Congress did not do that work so the USPTO could rewrite the scheme on the Director’s whim.

To be sure, the Director has broad “discretion” within the AIA’s statutory markers. *Cuozzo*, 579 U.S. at 273. But discretion *within* markers is not discretion to fashion new boundaries. And the AIA nowhere grants the USPTO power to ignore Congress’s framework and invent *new* criteria. “Administrative agencies are creatures of statute”; they “possess only the authority that Congress has provided.” *Nat’l Fed’n of Indep. Bus. v. Dep’t of Lab., Occupational Safety & Health Admin.*, 595 U.S. 109, 117 (2022).

And Congress carefully specified when the Director may exercise discretion in IPR institution. Take §325(d). There, Congress provided that, in instituting any “proceeding under this chapter” (including IPRs), the Director “may” consider whether “the same or substantially the same prior art or arguments previously were presented to the Office.” §325(d). Congress granted the Director discretion in applying that criterion (the Director “may” reject a petition). And it authorized accompanying regulations to flesh out the standard. §316(a)(2). Those regulations must consider effects on “the patent system” (by avoiding inconsistent outcomes on the same prior art or arguments) and “efficient [agency] administration” (by avoiding redundant proceedings). §316(b). But none of this matters under the

USPTO’s current position. If the USPTO already has unfettered discretion to consider anything it chooses at institution, it does not need §325(d)’s *redundant* authority to do the same thing. That express section should not be read as a mere suggestion (at best) or superfluous (at worst). *See Gustafson v. Alloyd Co.*, 513 U.S. 561, 574 (1995) (avoiding such “redundan[cy]”).

Or take §315(d).⁹ There, Congress authorized the USPTO to “stay, transfer, consolidat[e], or terminat[e]” related proceedings. §315(d). This expressly authorizes the Director to manage the agency’s docket when overlapping proceedings are pending before the agency. Again, Congress granted discretion in applying that criterion (the Director “*may* determine” how such proceedings “may proceed” (emphasis added)), and authorized implementing regulations. §§316(a)(2), (b). Yet none of this is necessary under the USPTO’s unbounded approach.

The USPTO invokes §314(a) as the source of the Director’s discretion. *See* AD’s Resp., *In re SAP Am., Inc.*, No. 25-132, ECF No. 39 at 12 (Fed. Cir. July 18, 2025); *see also* Appx2 (denying petitions under §314(a)); Appx61 (Stewart Memo) (identifying §314(a) as authority for Director’s “discretion”); *Fintiv*, 2020 WL

⁹ Section 325(d) includes nearly identical language for PGRs.

2126495, at *2. But that subsection grants no such authority. Section 314(a) textually imposes a direct requirement for institution: “a reasonable likelihood that the petitioner would prevail.” This sets the critical threshold. *See* §314(a). It does not grant the Director freestanding authority to impose *any* criteria the Director wishes—much less to abridge the universal “scope” of IPR (§311(b)). A provision that speaks in the negative and limits the Director’s discretion cannot be construed as a sweeping, affirmative grant of power to deny IPR based on *any* criteria the Director chooses.

Nor does it help the USPTO that §314(a) does not *mandate* institution when the merits threshold is met. Even for petitions meeting that threshold, Congress supplied other criteria *outside* §314(a) that could still defeat institution. *E.g.*, §§315(b), (e), 315(d), 325(d). But it was *Congress* that chose these additional criteria. It nowhere empowered the USPTO to make different choices.

Congress’s express grant of discretion in two accompanying AIA sections confirms it did not grant broader discretion here. For derivation proceedings, Congress provided “the Director *may* institute” if the requisite “standards . . . are met.” §135(a)(1) (emphasis added). Similarly, for joinder petitions, “the Director, *in his or her discretion, may* join” parties otherwise satisfying §314. §315(c) (emphasis added). No comparable authority exists for IPR institution. “When Congress

includes particular language in one section of a statute but omits it from a neighbor, we normally understand that difference in language to convey a difference in meaning.” *Bittner v. United States*, 598 U.S. 85, 94 (2023); *see also Gallo v. Dep’t of Transp.*, 725 F.3d 1306, 1310 (Fed. Cir. 2013) (*expressio unius*). Congress expressly conferred discretion elsewhere in the AIA, but not for instituting IPRs; the Court should enforce that congressional choice.

2. Congress did not authorize the Director to deny institution because a patent is “old.”

The USPTO’s new “settled expectations” rule falls outside the AIA’s institution criteria and thus fails. Indeed, the rule conflicts with express congressional judgments in the AIA.

The AIA contains no cap on how “old” a patent may be to remain IPR-eligible. That was a deliberate design decision, confirmed by several additional congressional choices.

For one, Congress used a patent-age cutoff for IPR’s predecessor (*inter partes* reexamination) and IPR’s AIA counterpart (PGR), but not IPR. Under the prior scheme, Congress had excluded certain old patents from *inter partes* reexamination. It limited eligibility to patents issued on applications “filed . . . on or after” November 29, 1999, the act’s effective date. American Inventors Protection Act of 1999, Pub. L. No. 106–113, §4608, 113 Stat. at 1501A–572. But when Congress

replaced *inter partes* reexamination with IPR, it imposed no such age cutoff. Yet Congress chose differently for PGR, imposing an age cutoff there. *See* AIA §3(n)(1) (limiting PGR to patents with an effective filing date on or after March 16, 2013). Thus, for IPRs, Congress expressly *rejected* the same sort of categorical “old-patent” exclusion the Director has now implemented.

For another, Congress imposed a continuing patent-age cap for PGR but not IPR. PGR is available only until the patent is 9 months old. §321(c). IPR has no such maximum. The USPTO has no license to recalibrate that deliberate balance.

In addition, Congress chose a uniform, weaker presumption of validity in IPR. §§316(e), 282; *see Cuozzo*, 579 U.S. at 279. All patent claims, no matter their age, face cancellation in IPR under a lower preponderance-of-the-evidence threshold. *Id.* Congress created no extra presumption of validity for older patents.

The agency cannot invent its own rules to frustrate this intentional congressional scheme. 5 U.S.C. §706(2)(A), (C). The USPTO’s new “settled expectations” rule adds a patent-age cap to IPR and an artificial presumption of validity for “old” patents. Appx2. That rule flouts Congress’s choices, violates the separation of powers, and is an illegitimate basis for denying IPR.

II. The remaining mandamus criteria are satisfied.

A. The USPTO's errors are reviewable in mandamus.

When the USPTO exceeds legal constraints in denying institution, this Court applies mandamus review. *Mylan*, 989 F.3d at 1380. “In fact, when the Board denies institution, our mandamus jurisdiction is especially important.” *Id.* Although “the appeal bar in §314(d) prevents any direct appeal,” it does not “divest[] [this Court] of mandamus jurisdiction.” *Id.* Section 314(d) therefore does not bar mandamus review of Petitioners’ claims.

First, the USPTO’s violations of constitutional constraints (due process and separation of powers) are subject to mandamus review. *Mylan*, 989 F.3d at 1382-83.

Second, its APA violations in regulating retroactively are reviewable. Despite §314(d), “judicial review remains available consistent with the [APA], which directs courts to set aside agency action ‘not in accordance with law’ or ‘in excess of statutory jurisdiction, authority, or limitations.’” *SAS Inst., Inc. v. Iancu*, 584 U.S. 357, 371 (2018) (quoting 5 U.S.C. §706(2)(A), (C)). Section I.B, *supra*, rests on *the APA’s* requirements that the agency not exceed delegated authority and consider relevant factors. This is not a challenge “where the invoked provisions of law directly govern institution.” *Apple Inc. v. Vidal*, 63 F.4th 1, 11-14 (Fed. Cir. 2023).

Third, the agency’s notice-and-comment obligations are reviewable. As this Court already explained, §314(d) does not reach “the Director’s choice of whether to use notice-and-comment rulemaking.” *Id.* at 14-15.

While *Mylan* rejected a notice-and-comment challenge to a USPTO decision, it did so on the merits: the mandamus petitioner had not established “a clear and indisputable right to relief.” 989 F.3d at 1382; *id.* (not “explor[ing] the outer contours of possibility” for mandamus); *Apple*, 63 F.4th at 12 n.5 (characterizing *Mylan* as “holding mandamus standard not met for challenge to denial based on *Fintiv* instructions”). Indeed, that petitioner only offered a few relevant sentences in the introduction and background sections of its briefing. *See* Opp. to Mot. to Dismiss, *Mylan Labs. Ltd. v. Janssen Pharma., N.V.*, No. 21-1071, ECF No. 16 at 1, 5-6 (Fed. Cir. Dec. 7, 2020). That petitioner’s case-specific failure does not insulate the USPTO from review here.

Fourth, this Court can stop the agency from creating institution criteria beyond its power. Judicial review is available for “shenanigans” like these, where the USPTO has “exceeded [its] statutory authority.” *SAS*, 584 U.S. at 371; *see also Cuozzo*, 579 U.S. at 275; 5 U.S.C. §706(2). The “shenanigans” here are obvious. The Acting Director has been open about her disagreement with Congress’s IPR system—“the low preponderance of evidence standard” and the lack of any

“window of time that closes to stop these challenges.” Appx696 (article). Those are *features* of the statutory design. Yet the Acting Director has wielded institution power to *frustrate* them.

The agency-power challenge here therefore falls outside §314(d), which bars review of “‘an ordinary dispute about the application of’ an institution-related statute.” *Thryv, Inc v. Click-To-Call Techs., LP*, 590 U.S. 45, 54 (2020) (quoting *Cuozzo*, 579 U.S. at 271); *see, e.g., id.* (§315(b)); *Cuozzo*, 579 U.S. at 271 (§312(a)(3)); *ESIP Series 2, LLC v. Puzhen Life USA, LLC*, 958 F.3d 1378, 1385-86 (Fed. Cir. 2020) (§312(a)(2)). The issue here goes well beyond case-specific interpretation or application of institution criteria.

Instead, this Court retains the ability to answer the more fundamental question of the agency’s authority to create institution standards in the first place. “§314(d) does not ‘enable the agency to act outside its statutory limits.’” *SAS*, 584 U.S. at 371 (quoting *Cuozzo*, 579 U.S. at 275); *see* 5 U.S.C. §706(2). This reflects a deeply rooted principle: “courts have recognized that an implicit and narrow exception to [a] bar on judicial review exists for claims that the agency exceeded the scope of its delegated authority or violated a clear statutory mandate.” *Hanauer v. Reich*, 82 F.3d 1304, 1307 (4th Cir. 1996); *see Leedom v. Kyne*, 358 U.S. 184 (1958). This case fits squarely within that preservation of judicial review. The Acting

Director’s creation of new, extra-statutory criteria is a “blatant violation[] of [a] legal constraint[]” that activates judicial review. *See IGT v. Zynga Inc.*, 144 F.4th 1357, 1367 (Fed. Cir. 2025).

Nor are any of this Court’s decisions to the contrary. *Apple* preserved mandamus review. 63 F.4th at 12 n.5 (reserving “‘whether mandamus might be available in an extraordinary case,’” since *Apple* was “not a mandamus case” (quoting *Thryv*, 590 U.S. at 54 n.6)). And regardless, *Apple* did not address a challenge to underlying agency power. The Court and parties assumed the Director *could* establish extra-statutory criteria. *Apple* held only that §314(d) barred a claim that the Director’s criteria misapprehended §315(b)’s time bar. That does not address the antecedent question whether Congress granted the Director unilateral authority to create institution criteria outside the AIA’s statutory framework—a materially different question. *Taylor Energy Co. v. Dep’t of the Interior*, 990 F.3d 1303, 1310, n.1 (Fed. Cir. 2021) (“[W]hen an issue is not argued or is ignored in a decision, such decision is not precedent to be followed in a subsequent case in which the issue arises.” (citation omitted)).

Nor does *Mylan* bar review of that question. As discussed, *Mylan* merely rejected the particular contentions there under the mandamus standard. *Supra* 33. And *Mylan* had no need to scrutinize the Director’s institution authority because all

involved *presumed* the Director was “free” to refuse institution based on “reasons of administrative efficiency.” 989 F.3d at 1382 (citing *Heckler v. Chaney*, 470 U.S. 821, 830-32 (1985)). Petitioners here, by contrast, have squarely raised whether the agency in fact has that discretion. And it is well-settled that “Congress may limit an agency’s exercise of enforcement power” “by setting substantive priorities” or “by otherwise circumscribing an agency’s power to discriminate among . . . cases it will pursue.” *Heckler*, 470 U.S. at 833. Here, Congress set boundaries that the agency has repeatedly exceeded, making this case a prototypical mandamus candidate.

* * *

If, however, the Court believes these fundamental questions are somehow unreviewable under existing circuit law, the Court should revisit those decisions en banc—initially or otherwise. And Petitioners reserve the right to seek such review.

B. Petitioners have no other adequate means of relief.

Mandamus is the proper mechanism for “judicial review” of “decisions denying institution,” “[g]iven that there is no adequate remedy by way of direct appeal,” which this Court holds is barred by §314(d). *In re Palo Alto Networks, Inc.*, 44 F.4th 1369, 1374 (Fed. Cir. 2022) (citation omitted).¹⁰

¹⁰ For similar reasons mandamus is available, Petitioners believe §314(d) should not be read to foreclose appeals challenging policies exceeding agency authority and

C. Mandamus is appropriate under the circumstances.

Mandamus is a critical check on unlawful agency action. It is appropriate “to decide ‘basic’ and ‘undecided’ questions” and “to further supervisory or instructional goals where issues are unsettled and important.” *In re BigCommerce, Inc.*, 890 F.3d 978, 981 (Fed. Cir. 2018) (quoting *Schlagenhauf v. Holder*, 379 U.S. 104, 110 (1964) and *In re Queen’s Univ. at Kingston*, 820 F.3d 1287, 1291 (Fed. Cir. 2016)). Mandamus is also warranted when “important to ‘proper judicial administration.’” *In re Cray Inc.*, 871 F.3d 1355, 1358-59 (Fed. Cir. 2017) (quoting *Schlagenhauf*, 379 U.S. at 110 and *In BP Lubricants USA Inc.*, 637 F.3d 1307, 1313 (Fed. Cir. 2011)).

This case is a prime mandamus candidate. It presents basic, undecided questions regarding the USPTO’s authority to rewrite Congress’s institution standards and impose, post-hoc, an extra-statutory “settled expectations” rule. *See BigCommerce*, 890 F.3d at 981. Those questions implicate the core functioning of Congress’s patent system and IPR scheme. *See Cray*, 871 F.3d at 1358-59. These actions have sweeping consequences for an overwhelming number of stakeholders.

violating statutory and constitutional mandates. But Petitioners acknowledge that under this Court’s existing precedent, no direct appeal from IPR institution denials is available—and no such appeal is necessary given the availability of mandamus.

The USPTO has unwound Congress’s work and categorically excluded an entire body of patents from review—immunizing “old” patents less than a third of the way into their lifespan. The USPTO’s refusal to stay within statutory bounds and follow notice-and-comment procedures has produced turmoil; the agency unleashes a constantly shifting landscape of confusion and uncertainty in a process Congress designed to be controlled by statute and regulation. Anything the USPTO says today could be reversed via website post tomorrow (at the whim of a current or future Director). This makes informed decisions impossible for IPR petitioners, patent owners, and investors—with serious effects on patent transactions, licensing, and litigation.

The agency’s erratic conduct exceeds lawful bounds. Mandamus exists to constrain unlawful action and force agencies to act within their lawful authority. This Court is ideally situated to enforce Congress’s scheme and hold the USPTO to its statutory and constitutional obligations.

CONCLUSION

The Court should grant the petition and vacate the three non-institution decisions. The Court should direct the USPTO to reconsider institution solely under the statutory criteria, not the agency’s extra-statutory framework. At a minimum, the Court should direct the USPTO to reconsider institution without the USPTO’s

new “settled expectations” rule and solely under the guidance in place when the petitions were filed.

Dated: September 17, 2025

Respectfully Submitted,

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CERTIFICATE OF COMPLIANCE

1. This petition complies with the type-volume limitation of Fed. R. App. P. 21(d) because:

■ this petition contains 7,793 words, excluding the parts of the brief exempted by Fed. R. App. P. 32(f) and Fed. Cir. R. 32(b)(2).

2. This brief complies with the typeface and type style requirements of Fed. R. App. P. 32(a)(5) and 32(a)(6) because:

■ this brief has been prepared in a proportionally spaced typeface using Word for Microsoft 365 in 14-point Equity A font.

/s/ Debra J. McComas

Debra J. McComas

PROOF OF SERVICE

I certify that on September 17, 2025, I caused a paper copy of this document (and the attached appendix, entries of appearance, certificates of interest, and notices of related cases) to be sent by express carrier to lead counsel for respondent Polaris PowerLED Technologies, LLC at the following address:

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I further certify that I caused courtesy electronic copies of this document (and the attached appendix, entries of appearance, certificates of interest, and notices of related cases) to be sent to David Alberti at dalberti@krameralberti.com and to the following additional counsel of record for respondent:

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I declare under penalty of perjury under the laws of the United States that the foregoing is true and correct.

Dated: September 17, 2025

/s/ Debra J. McComas

Debra J. McComas

No. 25-_____

**IN THE UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT**

**IN RE SANDISK TECHNOLOGIES INC. and
WESTERN DIGITAL TECHNOLOGIES, INC.,**
Petitioners.

APPENDIX TO PETITION FOR WRIT OF MANDAMUS

**On Petition for a Writ of Mandamus to the Director of the United States
Patent and Trademark Office, Patent Trial and Appeal Board
Nos. IPR2025-00515, IPR2025-00516 and IPR2025 -00517**

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4	IPR2025-00517	n/a	n/a	Docket of IPR2025-00517	Appx13
Administrative Materials¹					
5	n/a	n/a	6/21/2022	Memorandum from Director Vidal to Board, <i>Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation</i> (now rescinded)	Appx17

¹ These administrative documents were published by the USPTO, but were not filed as exhibits or papers in these IPRs. Accordingly, they do not have docket numbers.

6	n/a	n/a	4/21/2023	Advance Notice of Proposed Rulemaking, <i>Changes Under Consideration to Discretionary Institution Practices</i> , 88 Fed. Reg. 24,503	Appx26
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29	IPR2025-00517	14		Petitioner's Sur-Reply Brief on Discretionary Denial	Appx687
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30	n/a	n/a	9/8/2025	Ryan Davis, <i>Stewart Says New Patent Policies Aim to Bring Stability</i> , Law360 (Sept. 8, 2025)	Appx696
31	n/a	n/a	8/29/2025	Jonathan DeFosse et al., <i>Data Undermines USPTO's 'Settled Expectations' Doctrine</i> , Law360 (Aug. 29, 2025)	Appx699

² These documents were not filed in these three IPRs. Accordingly, they do not have docket numbers from the IPRs.

[Director Discretionary Decision@uspto.gov](mailto:Director_Discretionary_Decision@uspto.gov)

571-272-7822

Paper 15

Date: July 16, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE OFFICE OF THE UNDER SECRETARY OF COMMERCE
FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE
UNITED STATES PATENT AND TRADEMARK OFFICE

SANDISK TECHNOLOGIES INC. and
WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner.

IPR2025-00515 (Patent 9,183,085 B2)
IPR2025-00516 (Patent 8,601,346 B2)
IPR2025-00517 (Patent 8,554,968 B2)

Before COKE MORGAN STEWART, *Acting Under Secretary of
Commerce for Intellectual Property and Acting Director of the United States
Patent and Trademark Office.*

DECISION
Denying Institution of *Inter Partes* Review

IPR2025-00515 (Patent 9,183,085 B2)
IPR2025-00516 (Patent 8,601,346 B2)
IPR2025-00517 (Patent 8,554,968 B2)

Polaris PowerLED Technologies, LLC (“Patent Owner”) filed a request for discretionary denial (Paper 9, “DD Req.”) in the above-captioned cases, and Sandisk Technologies, Inc. and Western Digital Technologies, Inc. (“Petitioner”) filed an opposition (Paper 12, “DD Opp.”).¹

After considering the parties’ arguments and the record, and in view of all relevant considerations, discretionary denial of institution is appropriate in these proceedings. This determination is based on the totality of the evidence and arguments the parties have presented.

Some considerations counsel against discretionary denial. For example, the parallel district court litigation involving Patent Owner and Petitioner has been stayed. However, other considerations favor discretionary denial. For example, the challenged patents have been in force for approximately nine, twelve, and twelve years, creating strong settled expectations, and Petitioner does not provide any persuasive reasoning why an *inter partes* review is an appropriate use of Board resources. *Dabico Airport Sols. Inc. v. AXA Power ApS*, IPR2025-00408, Paper 21 at 2–3 (Director June 18, 2025). In the absence of any such information, the Office is disinclined to disturb the settled expectations of Patent Owner.

Although certain arguments are highlighted above, the determination to exercise discretion to deny institution is based on a holistic assessment of all of the evidence and arguments presented. Accordingly, the Petitions are denied under 35 U.S.C. § 314(a).

In consideration of the foregoing, it is:

¹ Citations are to papers in IPR2025-00515. The parties filed similar papers in IPR2025-00516 and IPR2025-00517.

IPR2025-00515 (Patent 9,183,085 B2)

IPR2025-00516 (Patent 8,601,346 B2)

IPR2025-00517 (Patent 8,554,968 B2)

ORDERED that Patent Owner's request for discretionary denial is *granted*; and

FURTHER ORDERED that the Petitions are *denied*, and no trial is instituted.

IPR2025-00515 (Patent 9,183,085 B2)
IPR2025-00516 (Patent 8,601,346 B2)
IPR2025-00517 (Patent 8,554,968 B2)

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DOCKET
(IPR2025-00515)

Case # IPR2025-00515 DISCRETIONARY DENIAL

Patent # 9183085

Parties Sandisk Technologies, Inc. et al. v. Polaris PowerLED Technologies, LLC

Tech center 2100 Art unit 2112

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Exhibits

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✓	1009	01/29/2025	Ex.1009-SSD Requirements & Endurance Test. JESD218	32	Petitioner	Public
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✓	1007	01/29/2025	Ex.1007-US8176360-Frost et al	38	Petitioner	Public
✓	1006	01/29/2025	Ex.1006-US9037951-Cirdecivan et al	22	Petitioner	Public
✓	1005	01/29/2025	Ex.1005-US Pub. 20140136927-Li et al	15	Petitioner	Public
✓	1004	01/29/2025	Ex.1004-CV of Dr. Lara Dolecek	26	Petitioner	Public
✓	1003	01/29/2025	Ex.1003-Declaration of Dr. Lara Dolecek (Polaris 085 patent)	113	Petitioner	Public
✓	1002	01/29/2025	Ex.1002-Prosecution History of U.S. App. No. 13-477600	744	Petitioner	Public
✓	1001	01/29/2025	Ex.1001-US9183085-May 12 2012	51	Petitioner	Public

▼ Real party

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Petitioner side

Name	Individual or Organization	Address	Email	Phone number	Fax number
Sandisk Technologies, Inc.	Organization	951 Sandisk Drive, Milpitas, CA, 95035, US			
Western Digital Technologies, Inc.	Organization	5601 Great Oaks Parkway, San Jose, CA, 95119, US			

Patent Owner / Respondent side

Appx7

Name	Individual or Organization	Address	Email	Phone number	Fax number
Polaris PowerLED Technologies, LLC	Organization	CA, US			

▼ Counsel

Petitioner side

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Counsel Type	Name	Email	USPTO Reg #	Phone number	Fax number
Lead Counsel	David O'Dell	david.odell.ipr@haynesboone.com	42044	972-739-8635	214-200-0853
Back-up Counsel	Hong Shi	hong.shi.ipr@haynesboone.com	69009	512-867-8440	214-200-0853
Back-up Counsel	Calmann Clements	calmann.clements.ipr@haynesboone.com	66910	972-739-8638	214-200-0853

Patent Owner / Respondent side

Counsel Type	Name	Email	USPTO Reg #	Phone number	Fax number
Lead Counsel	David Alberti	dalberti@krameralberti.com	43465	650-384-9869	
Back-up Counsel	sal lim	slim@feinday.com	45706	650-269-3543	
Back-up Counsel	Jason Fitzsimmons	jfitzsimmons-ptab@sternekessler.com	65367	202-772-8701	
Back-up Counsel	Richard Bemben	rbemben-ptab@sternekessler.com	68658	202-772-8549	
Back-up Counsel	Michael Specht	mspecht-ptab@sternekessler.com	54463	202-772-8756	

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Party	Transaction date (mm/dd/yyyy)	Payment method	Description	Fee code	Quantity	Fee amount	Fee total
PETITIONER	01/29/2025	Deposit Account	Inter Partes Review Post-Institution Fee - Up To 20 Claims	1414	1	\$28,125.00	\$28,125.00
PETITIONER	01/29/2025	Deposit Account	Inter Partes Review Request Fee - Up To 20 Claims	1406	1	\$23,750.00	\$23,750.00

DOCKET
(IPR2025-00516)

Case # IPR2025-00516 DISCRETIONARY DENIAL

Patent # 8601346

Parties Sandisk Technologies, Inc. et al. v. Polaris PowerLED Technologies, LLC

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✓	14	07/03/2025	Other: other	Petitioner's Sur-Reply Brief on Discretionary Denial	8	Petitioner	Public
✓	13	06/30/2025	Other: other	Patent Owner's Discretionary Denial Reply Brief	9	Patent Owner	Public
✓	12	06/24/2025	PET Opposition to Discretionary Denial Brief	Petitioner's Opposition to Patent Owner's Request for Discretionary Denial	31	Petitioner	Public
✓	11	05/27/2025	POPR: filed	Patent Owner's Preliminary Response	23	Patent Owner	Public
✓	10	04/25/2025	Notice: Updated Mandatory Notice	Patent Owner's Updated Mandatory Notices	5	Patent Owner	Public
✓	9	04/25/2025	PO Discretionary Denial Brief	Patent Owner's Brief on Discretionary Denial	40	Patent Owner	Public
✓	8	04/24/2025	Notice: Other	Notice: Extending Deadline for Discretion Briefing	4	Board	Public
✓	7	02/26/2025	Notice: Updated Mandatory Notice	Patent Owner's Updated Mandatory Notices	3	Patent Owner	Public
✓	6	02/26/2025	Notice: Notice filing date accorded	Notice: Notice filing date accorded	10	Board	Public
✓	5	02/13/2025	Notice: Mandatory Notice	Patent Owner's Mandatory Notices	6	Patent Owner	Public
✓	4	02/13/2025	Notice: Power of Attorney	Patent Owner's Power of Attorney	4	Patent Owner	Public
✓	3	01/23/2025	Petition: as filed	IPR Petition '346	83	Petitioner	Public
✓	2	01/23/2025	Notice: Power of Attorney	Petitioner's Power of Attorney- '346-Western Digital	2	Petitioner	Public
✓	1	01/23/2025	Notice: Power of Attorney	Petitioner's Power of Attorney- '346-Sandisk Technologies	2	Petitioner	Public

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✓	Exhibit # ↓	Filing date	Document name	Pages	Filing party	Availability
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✓	3101	06/26/2025	Ex. 3101	2	Board	Public
✓	3100	05/27/2025	E-mail regarding due dates	6	Board	Public
✓	2015	04/25/2025	EX2015-2025-04-18-WP-Proposed Claim Terms for Construction18	5	Patent Owner	Public
✓	2014	04/25/2025	EX2014-Sandisk Celebrates Nasdaq Listing After Completing Separation Sandisk	3	Patent Owner	Public
✓	2013	04/25/2025	EX2013-Patent Trial and Appeal Board (PTAB) Dashboard USPTO	5	Patent Owner	Public
✓	2012	04/25/2025	EX2012-fv25_ptab_appeal_statistics_2025march	9	Patent Owner	Public
✓	2011	04/25/2025	EX2011-Reply for Motion to Stay-CDCA-2-24-cv-02864-62	12	Patent Owner	Public
✓	2010	04/25/2025	EX2010-Protective Order-CDCA-2-24-cv-02864-61	31	Patent Owner	Public

✓	Exhibit # ↓	Filing date	Document name	Pages	Filing party	Availability
✓	2009	04/25/2025	EX2009-Exhibit C-Terms for Construction-CDCA-2-24-cv-02864-60-4	7	Patent Owner	Public
✓	2008	04/25/2025	EX2008-Exhibit B-Initial Invalidity Contentions-CDCA-2-24-cv-02864-60-3	108	Patent Owner	Public
✓	2007	04/25/2025	EX2007-Opposition to Motion to Stay-CDCA-2-24-cv-02864-60	27	Patent Owner	Public
✓	2006	04/25/2025	EX2006-Minute Order for Contentions-CDCA-2-24-cv-02864-59	1	Patent Owner	Public
✓	2005	04/25/2025	EX2005-Motion to Stay-CDCA-2-24-cv-02864-58	22	Patent Owner	Public
✓	2004	04/25/2025	EX2004-Scheduling Order-CDCA-2-24-cv-02864-54	26	Patent Owner	Public
✓	2003	04/25/2025	EX2003-List of Docket Entries, Micron v. Polaris, 1-25-cv-00073 (D. Idaho)	3	Patent Owner	Public
✓	2002	04/25/2025	EX2002-List of Docket Entries, Polaris v. WDC, 2-24-cv-02864 (C.D. Cal.)	10	Patent Owner	Public
✓	2001	04/25/2025	EX2001-List of Docket Entries, Polaris v. WDC, 1-24-cv-00101 (W.D. Tex.)	3	Patent Owner	Public
✓	1037	06/24/2025	Ex.1037-Perryman Inter Partes Review Impact 1 27 2021	15	Petitioner	Public
✓	1036	06/24/2025	Ex.1036-Judge Wright Markman Hearings and Orders	125	Petitioner	Public
✓	1035	06/24/2025	Ex.1035-Western Digital Form 10-K	209	Petitioner	Public
✓	1033	06/24/2025	Ex.1033-PTAB Judges Told To Get Ready For Layoffs-Law360	2	Petitioner	Public
✓	1032	06/24/2025	Ex.1032-Chief Patent Board Judge Waves Off Workforce Attrition Concerns	1	Petitioner	Public
✓	1031	06/24/2025	Ex.1031-Order Granting WD's Motion to Stay (06-23-25)	9	Petitioner	Public
✓	1022	06/24/2025	Ex.1022-Polaris Infringement Contentions Cover Pleading-10-02-2024	10	Petitioner	Public
✓	1021	06/24/2025	Ex.1021-Patent Assignment Recordation	2	Petitioner	Public
✓	1020	06/24/2025	Ex.1020-FAQs for Interim Processes (captured 5.13.25)	10	Petitioner	Public
✓	1018	06/24/2025	Ex.1018-2025-04-28-WD-Notice of Sotera Stipulations	5	Petitioner	Public
✓	1017	01/23/2025	Ex.1017-Interim Proc for Discretionary Denials in AIA Parallel Dist Ct Lit	9	Petitioner	Public
✓	1016	01/23/2025	Ex.1016-District Court Stats 9.30.2024	95	Petitioner	Public
✓	1015	01/23/2025	Ex.1015-Complaint	60	Petitioner	Public
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✓	1013	01/23/2025	Ex.1013-US8819699	10	Petitioner	Public
✓	1012	01/23/2025	Ex.1012-US8074149 Stolowitz	72	Petitioner	Public
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✓	1009	01/23/2025	Ex.1009-US6161165-Solomon	13	Petitioner	Public
✓	1008	01/23/2025	Ex.1008-US5787460 Yashiro	67	Petitioner	Public
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✓	1006	01/23/2025	Ex.1006-US5950225 Kleiman	12	Petitioner	Public
✓	1005	01/23/2025	Ex.1005-US20110078496A1 Jeddalah	16	Petitioner	Public
✓	1004	01/23/2025	Ex.1004-Paul Min CV	26	Petitioner	Public
✓	1003	01/23/2025	Ex.1003-Min Declaration	111	Petitioner	Public
✓	1002	01/23/2025	Ex.1002-346 File History	196	Petitioner	Public
✓	1001	01/23/2025	Ex.1001-US8601346	25	Petitioner	Public

▼ Real party

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Petitioner side

Name	Individual or Organization	Address	Email	Phone number	Fax number
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Western Digital Technologies, Inc.	Organization	5601 Great Oaks Parkway, San Jose, CA, 95119, US			

Patent Owner / Respondent side

Name	Individual or Organization	Address	Email	Phone number	Fax number
Polaris PowerLED Technologies, LLC	Organization	CA, US			

▼ Counsel

Petitioner side

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Back-up Counsel	Hong Shi	hong.shi.ipr@haynesboone.com	69009	512-867-8440	214-200-0853

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Back-up Counsel	sal lim	slim@feinday.com	45706	650-269-3543	650-460-8443
Back-up Counsel	Jason Fitzsimmons	jfitzsimmons-ptab@sternekessler.com	65367	202-772-8701	202-371-2540
Back-up Counsel	Richard Bembien	rbembien-ptab@sternekessler.com	68658	202-772-8549	202-371-2540
Back-up Counsel	Michael Specht	mspecht-ptab@sternekessler.com	54463	202-772-8756	202-371-2540

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PETITIONER	01/23/2025	Deposit Account	Inter Partes Review Request Fee - Up To 20 Claims	1406	1	\$23,750.00	\$23,750.00

DOCKET
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Case # IPR2025-00517 DISCRETIONARY DENIAL

Patent # 8554968

Parties Sandisk Technologies, Inc. et al. v. Polaris PowerLED Technologies, LLC

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✓	13	06/30/2025	Other: other	Patent Owner's Discretionary Denial Reply Brief	9	Patent Owner	Public
✓	12	06/24/2025	PET Opposition to Discretionary Denial Brief	Petitioner's Opposition to Patent Owner's Request for Discretionary Denial	36	Petitioner	Public
✓	11	05/27/2025	POPR: filed	Patent Owner's Preliminary Response	54	Patent Owner	Public
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✓	9	04/25/2025	PO Discretionary Denial Brief	Patent Owner's Brief on Discretionary Denial	54	Patent Owner	Public
✓	8	04/24/2025	Notice: Other	Notice: Extending Deadline for Discretionary Briefing	4	Board	Public
✓	7	02/26/2025	Notice: Updated Mandatory Notice	Patent Owner's Updated Mandatory Notices	3	Patent Owner	Public
✓	6	02/26/2025	Notice: Notice filing date accorded	Notice: Notice filing date accorded	10	Board	Public
✓	5	02/14/2025	Notice: Mandatory Notice	Patent Owner's Mandatory Notices	6	Patent Owner	Public
✓	4	02/14/2025	Notice: Power of Attorney	Patent Owner's Power of Attorney	4	Patent Owner	Public
✓	3	01/24/2025	Petition: as filed	IPR Petition '968	95	Petitioner	Public
✓	2	01/24/2025	Notice: Power of Attorney	Petitioner's Power of Attorney - '968 - Western Digital	1	Petitioner	Public
✓	1	01/24/2025	Notice: Power of Attorney	Petitioner's Power of Attorney - '968 - Sandisk Technologies	1	Petitioner	Public

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✓	Exhibit # ↓	Filing date	Document name	Pages	Filing party	Availability
✓	3103	07/09/2025	Ex. 3103	6	Board	Public
✓	3102	07/02/2025	Ex. 3102	4	Board	Public
✓	3101	06/26/2025	Ex. 3101	2	Board	Public
✓	3100	05/27/2025	E-mail regarding due dates	6	Board	Public
✓	2026	05/27/2025	EX2026-Specifications - PCI-SIG	7	Patent Owner	Public
✓	2025	05/27/2025	EX2025-Proposed Claim Constructions and Intrinsic and Extrinsic Evidence	11	Patent Owner	Public
✓	2024	04/25/2025	EX2024-2025-04-18-WD-Proposed Claim Terms for Construction18	5	Patent Owner	Public
✓	2023	04/25/2025	EX2023-US20100185808A1	67	Patent Owner	Public
✓	2022	04/25/2025	EX2022-US20080320214A1	48	Patent Owner	Public
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✓	2020	04/25/2025	EX2020-US7620784	13	Patent Owner	Public
✓	2019	04/25/2025	EX2019-NVM_Express_1.0_Gold	122	Patent Owner	Public
✓	2018	04/25/2025	EX2018-67813_15585808	10	Patent Owner	Public
✓	2017	04/25/2025	EX2017-US10296249	25	Patent Owner	Public
✓	2016	04/25/2025	EX2016-Redline Comparison of 12537733 and 12756477	137	Patent Owner	Public
✓	2015	04/25/2025	EX2015-61374242	367	Patent Owner	Public
✓	2014	04/25/2025	EX2014-Sandisk Celebrates Nasdaq Listing After Completing Separation Sandisk	3	Patent Owner	Public
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✓	1037	06/24/2025	Ex.1037-Western Digital Form 10-K	209	Petitioner	Public
✓	1035	06/24/2025	Ex.1035-2024-12-16-WD Cover Pleading-Invalidity Contentions	73	Petitioner	Public
✓	1034	06/24/2025	Ex.1034-PTAB Judges Told To Get Ready For Layoffs-Law360	2	Petitioner	Public
✓	1033	06/24/2025	Ex.1033-Chief Patent Board Judge Waves Off Workforce Attrition Concerns	1	Petitioner	Public
✓	1032	06/24/2025	Ex.1032-Order Granting WD's Motion to Stay (06-23-25)	9	Petitioner	Public
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✓	1018	01/24/2025	Ex.1018-US20100185719A1	41	Petitioner	Public
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✓	1014	01/24/2025	Ex.1014-Internet Archive-PCI Express Base 2.0 Specification	2	Petitioner	Public
✓	1013	01/24/2025	Ex.1013-Interim Proc for Discretionary Denials in AIA Parallel Dist Ct Lit	9	Petitioner	Public
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✓	1011	01/24/2025	Ex.1011-Complaint	60	Petitioner	Public
✓	1010	01/24/2025	Ex.1010-IEEE Dictionary	3	Petitioner	Public
✓	1009	01/24/2025	Ex.1009-Serebrin Provisional (61301937)	67	Petitioner	Public
✓	1008	01/24/2025	Ex.1008-US20110197003A1 Serebrin	27	Petitioner	Public
✓	1007	01/24/2025	Ex.1007-PCI Express Base Specification v20	632	Petitioner	Public
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✓	1002	01/24/2025	Ex.1002-968 File History	179	Petitioner	Public
✓	1001	01/24/2025	Ex.1001-US8554968	34	Petitioner	Public

▼ Real party

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Petitioner side

Name	Individual or Organization	Address	Email	Phone number	Fax number
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Western Digital Technologies, Inc.	Organization	5601 Great Oaks Parkway, San Jose, CA, 95119, US			

Patent Owner / Respondent side

Name	Individual or Organization	Address	Email	Phone number	Fax number
Polaris PowerLED Technologies, LLC	Organization	CA, US			

▼ Counsel

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Petitioner side

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Lead Counsel	David O'Dell	david.odell.ipr@haynesboone.com	42044	972-739-8635	214-200-0853
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Back-up Counsel	Hong Shi	hong.shi.ipr@haynesboone.com	69009	512-867-8440	214-200-0853

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Back-up Counsel	Jason Fitzsimmons	jfitzsimmons-ptab@sternekessler.com	65367	202-772-8701	202-371-2540
Back-up Counsel	Richard Bemben	rbemben-ptab@sternekessler.com	68658	202-772-8549	202-371-2540
Back-up Counsel	Michael Specht	mspecht-ptab@sternekessler.com	54463	202-772-8756	202-371-2540

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Party	Transaction date (mm/dd/yyyy)	Payment method	Description	Fee code	Quantity	Fee amount	Fee total
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PETITIONER	01/24/2025	Deposit Account	Inter Partes Review Request Fee - Up To 20 Claims	1406	1	\$23,750.00	\$23,750.00



Patent Trial and Appeal Board
Rescinded: February 28, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND
DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE

MEMORANDUM

DATE: June 21, 2022

TO: Members of the Patent Trial and Appeal Board

FROM: Katherine K. Vidal *Katherine Kelly Vidal*
Under Secretary of Commerce for Intellectual Property and
Director of the United States Patent and Trademark Office (USPTO or the Office)

SUBJECT: INTERIM PROCEDURE FOR DISCRETIONARY DENIALS IN AIA POST-
GRANT PROCEEDINGS WITH PARALLEL DISTRICT COURT
LITIGATION

Introduction

Congress designed the America Invents Act (AIA) post-grant proceedings “to establish a more efficient and streamlined patent system that will improve patent quality and limit unnecessary and counterproductive litigation costs.” H.R. Rep. No. 112–98, pt. 1, at 40 (2011), 2011 U.S.C.C.A.N. 67, 69; *see* S. Rep. No. 110–259, at 20 (2008). Parallel district court and AIA proceedings involving the same parties and invalidity challenges can increase, rather than limit, litigation costs. Based on the USPTO’s experience with administering the AIA, the agency has recognized the potential for inefficiency and gamesmanship in AIA proceedings, given the existence of parallel proceedings between the Office and district courts. To minimize potential conflict between the Patent Trial and Appeal Board (PTAB) and district court proceedings, the Office designated as precedential *Apple Inc. v. Fintiv, Inc.*¹ This precedential decision articulates

¹ *See Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) (designated precedential May 5, 2020).

the following set of nonexclusive factors (the *Fintiv* factors) that the PTAB considers on a case-specific basis in determining whether to institute an AIA post-grant proceeding where there is parallel district court litigation:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

The Office issued a Request for Comments (RFC)² on the PTAB's current approaches to exercising discretion on whether to institute an AIA proceeding, including situations involving parallel district court litigation. The Office received 822 comments from a wide range of stakeholders. In light of the feedback received, the Office is planning to soon explore potential rulemaking on proposed approaches through an Advanced Notice of Proposed Rulemaking. In the meantime, I have determined that several clarifications need to be made to the PTAB's current application of *Fintiv* to discretionary institution where there is parallel litigation.

As explained below, to benefit the patent system and the public good, the PTAB will not rely on the *Fintiv* factors to discretionarily deny institution in view of parallel district court litigation where a petition presents compelling evidence of unpatentability. This memorandum also confirms that the precedential import of *Fintiv* is limited to facts of that case. Namely, *Fintiv* involved institution of an AIA proceeding with a parallel district court litigation. The

² Discretion to Institute Trials Before the Patent Trial and Appeal Board, 85 FR 66502 (Oct. 20, 2020); Discretion to Institute Trials Before the Patent Trial and Appeal Board; Extension of Comment Period, 85 FR 73437 (Nov. 18, 2020).

plain language of the *Fintiv* factors is directed to district court litigation and does not apply to parallel U.S. International Trade Commission (ITC) proceedings, as the ITC lacks authority to invalidate a patent and the ITC's invalidity rulings are not binding on the Office or on district courts.

Consistent with *Sotera Wireless, Inc.*,³ the PTAB will not discretionarily deny institution in view of parallel district court litigation where a petitioner presents a stipulation not to pursue in a parallel proceeding the same grounds or any grounds that could have reasonably been raised before the PTAB. Additionally, when considering the proximity of the district court's trial date to the date when the PTAB final written decision will be due, the PTAB will consider the median time from filing to disposition of the civil trial for the district in which the parallel litigation resides.⁴ This memorandum clarifies those practices.

This memorandum is issued under the Director's authority to issue binding agency guidance to govern the PTAB's implementation of various statutory provisions, including directions regarding how those statutory provisions will apply to sample fact patterns. *See, e.g.*, 35 U.S.C. 3(a)(2)(A); PTAB Standard Operating Procedure (SOP) 2 at 1–2.

Analysis

Compelling Merits

In the AIA, Congress established post-grant proceedings, including IPR, PGR, and covered business method (CBM) proceedings to improve and ensure patent quality by providing “quick and cost-effective alternatives to litigation” for challenging issued patents. H.R. Rep. No. 112–98, pt. 1, at 48; *see also* S. Rep. No. 110–259, at 20 (explaining that the “post-grant review

³ *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) (precedential as to § II.A).

⁴ <https://www.uscourts.gov/statistics-reports/analysis-reports/federal-court-management-statistics>

system . . . will give third parties a quick, inexpensive, and reliable alternative to district court litigation to resolve questions of patent validity”). Congress granted the Office “significant power to revisit and revise earlier patent grants” as a mechanism “to improve patent quality and restore confidence in the presumption of validity that comes with issued patents.” *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 272 (2016) (quoting H.R. Rep. No. 112-98, pt. 1, at 45, 48). Given those objectives, compelling, meritorious challenges will be allowed to proceed at the PTAB even where district court litigation is proceeding in parallel. Compelling, meritorious challenges are those in which the evidence, if unrebutted in trial, would plainly lead to a conclusion that one or more claims are unpatentable by a preponderance of the evidence. That said, the PTAB retains discretion to deny institution for proceedings where abuse has been demonstrated.

Fintiv factor six reflects that the PTAB considers the merits of a petitioner’s challenge when determining whether to institute a post-grant proceeding in view of parallel district court litigation. Where the information presented at the institution stage is merely sufficient to meet the statutory institution threshold,⁵ the PTAB has the authority, where warranted, to exercise discretion to deny institution in view of the other *Fintiv* factors. In contrast, where the PTAB determines that the information presented at the institution stage presents a compelling

⁵ Institution of an IPR is authorized by statute only when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). Similarly, institution of a PGR, including a CBM, is authorized only when “the information presented in the petition . . . , if such information is not rebutted, would demonstrate that it is more likely than not that at least 1 of the claims challenged in the petition is unpatentable” *Id.* § 324(a).

unpatentability challenge, that determination alone demonstrates that the PTAB should not discretionarily deny institution under *Fintiv*.⁶

This clarification strikes a balance among the competing concerns of avoiding potentially conflicting outcomes, avoiding overburdening patent owners, and strengthening the patent system by eliminating patents that are not robust and reliable. Consistent with Congress's giving the Office the authority to revisit issued patents, the PTAB will not deny institution based on *Fintiv* if there is compelling evidence of unpatentability. This approach "allows the proceeding to continue in the event that the parallel proceeding settles or fails to resolve the patentability question presented in the PTAB proceeding." *Fintiv*, Paper 11 at 15. The patent system and the public good benefit from instituting compelling unpatentability challenges.

ITC and *Fintiv*

In 2018, the PTAB issued a decision in *NHK Spring*.⁷ There, the PTAB held that the advanced state of a parallel district court litigation involving similar validity disputes could be a factor weighing in favor of denying institution of an IPR because of concerns over the inefficient

⁶ The compelling evidence test affirms the PTAB's current approach of declining to deny institution under *Fintiv* where the evidence of record so far in the case would plainly lead to a conclusion that one or more claims are unpatentable. See, e.g., *Illumina Inc. v. Trs. of Columbia Univ.*, IPR2020-00988, Paper 20 (PTAB Dec. 8, 2020) (declining to deny under *Fintiv* in light of strong evidence on the merits even though four factors weighed in favor of denial and remaining factor was neutral); *Synthego Corp. v. Agilent Techs., Inc.*, IPR2022-00402, Paper 11 (May 31, 2022) (granting institution as efficiency and integrity of the system would not be served by denying institution of petition with particularly strong evidence on the merits); *Samsung Elecs. Co. v. Scramoge Tech., Ltd.*, IPR2022-00241, Paper 10 (June 13, 2022) (*Fintiv* analysis concludes that "very strong" evidence on the merits outweigh concurrent litigation involving earlier scheduled trial date and significant overlap in proceedings).

⁷ *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 (PTAB Sept. 12, 2018) (precedential). This decision also based the denial of institution on Director discretion under 35 U.S.C. § 325(d).

use of PTAB's resources. *NHK Spring*, Paper 8 at 19–20. Later, in 2020, the PTAB announced the *Fintiv* factors, which the PTAB considers when a patent owner raises an argument for discretionary denial under *NHK Spring* due to an earlier trial date. *Fintiv*, Paper 11 at 5–6. The *Fintiv* factors focus on the interplay between IPRs and district court litigation. Through that focus, the *Fintiv* factors seek to avoid duplicative efforts between the PTAB and federal district courts. For example, *Fintiv* factor one asks whether the “court” has granted a stay or if one may be granted. Similarly, *Fintiv* factor two looks at the proximity of the “court” trial date. Likewise, *Fintiv* factor three concerns the amount of investment in the parallel proceeding by the “court” and the parties. *Fintiv* factors five and six refer to the same parallel proceeding described in factor three.

Although the *Fintiv* factors are directed to district court litigation and not ITC proceedings,⁸ the PTAB has, in the past, denied AIA reviews based on parallel ITC investigations.⁹ Important differences, however, distinguish ITC investigations from patent invalidity trials in federal district courts. Unlike district courts, the ITC lacks authority to invalidate a patent and its invalidity rulings are not binding on either the Office or a district court. See *Tandon Corp. v. U.S.I.T.C.*, 831 F.2d 1017, 1019 (Fed. Cir. 1987). Therefore, an ITC determination cannot conclusively resolve an assertion of patent invalidity, which instead requires either district court litigation or a PTAB proceeding to obtain patent cancellation. Thus, denying institution because of a parallel ITC investigation will not necessarily minimize

⁸ *Fintiv* refers to ITC proceedings in discussing factor one. *Fintiv*, Paper 11 at 8–9. Addressing the situation where district court litigation is stayed pending an ITC investigation, *Fintiv* states in *dicta* that “it is difficult to maintain a district court proceeding on patent claims determined to be invalid at the ITC.” *Id.* at 9.

⁹ See, e.g., *Philip Morris Prods. S.A. v. Rai Strategic Holdings, Inc.*, IPR2020-00919, Paper 9 (PTAB Nov. 16, 2020).

potential conflicts between PTAB proceedings and district court litigation. For the foregoing reasons, the PTAB no longer discretionarily denies petitions based on applying *Fintiv* to a parallel ITC proceeding. This memorandum memorializes that practice. The PTAB will not discretionarily deny petitions based on applying *Fintiv* to a parallel ITC proceeding.

***Sotera* Stipulations**

Fintiv factor four looks at the overlap between the issues raised in the IPR petition and in the parallel proceeding in order to evaluate “concerns of inefficiency and the possibility of conflicting decisions.” *Fintiv*, Paper 11 at 12. If the petition includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding, this fact has favored denial. *Id.* at 12. Conversely, if the petition includes materially different grounds, arguments, and/or evidence than those presented in the district court, this fact has tended to weigh against exercising discretion to deny institution. *Id.* at 12–13.

When a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition, it mitigates concerns of potentially conflicting decisions and duplicative efforts between the district court and the PTAB. *See Sotera*, Paper 12 at 18–19. With such a stipulation, if an IPR or PGR is instituted, the grounds the PTAB resolves will differ from those present in the parallel district court litigation. For these reasons, the PTAB will not discretionarily deny institution of an IPR or PGR in view of parallel district court litigation where a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition. This clarification avoids inconsistent outcomes

between the PTAB and the district court and allows the PTAB to review grounds that the parallel district court litigation will not resolve.

Trial Date

Fintiv factor two considers the proximity of the court's trial date to the Board's projected statutory deadline for a final written decision. When applying this factor, the PTAB has taken the "courts' trial schedules at face value absent some strong evidence to the contrary."¹⁰ Thus, the PTAB has generally weighed this factor in favor of exercising discretion to deny institution if the trial date is scheduled before the projected statutory deadline for a final written decision.

In response to the RFC, a number of commenters expressed concern with the use of trial dates as a factor.¹¹ Stakeholders correctly noted that scheduled trial dates are unreliable and often change. A court's scheduled trial date, therefore, is not by itself a good indicator of whether the district court trial will occur before the statutory deadline for a final written decision.

Accordingly, when analyzing the proximity of the court's trial date under factor two of *Fintiv*, when other relevant factors weigh against exercising discretion to deny institution or are neutral, the proximity to trial should not alone outweigh all of those other factors. *See In re Genentech, Inc.*, 566 F.3d 1338, 1347 (Fed Cir. 2009). Parties may present evidence regarding the most recent statistics on median time-to-trial for civil actions in the district court in which the

¹⁰ *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 13 (May 13, 2020) (informative) (applying the *Fintiv* factors articulated in the precedential *Fintiv* decision).

¹¹ *See USPTO Executive Summary of Public Views on Discretionary Institution of AIA Proceedings* (Jan. 2021) (available at <https://www.uspto.gov/sites/default/files/documents/USPTOExecutiveSummaryofPublicViewsonDiscretionaryInstitutiononAIAProceedingsJanuary2021.pdf>).

parallel litigation resides¹² for the PTAB's consideration. Where the parties rely on time-to-trial statistics, the PTAB will also consider additional supporting factors such as the number of cases before the judge in the parallel litigation and the speed and availability of other case dispositions. *See id.*; *In re Google LLC*, No. 2021-178, 2021 WL 5292267 at *3 (Fed. Cir. 2021).

Conclusion

In summary, the PTAB will not deny institution of an IPR or PGR under *Fintiv* (i) when a petition presents compelling evidence of unpatentability; (ii) when a request for denial under *Fintiv* is based on a parallel ITC proceeding; or (iii) where a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as in the petition or any grounds that could have reasonably been raised in the petition. Additionally, when the PTAB is applying *Fintiv* factor two, the PTAB will consider the speed with which the district court case may come to trial and be resolved. The PTAB will weigh this factor against exercising discretion to deny institution under *Fintiv* if the median time-to-trial is around the same time or after the projected statutory deadline for the PTAB's final written decision. That said, even if the PTAB does not deny institution under *Fintiv*, it retains the right to deny institution for other reasons under 35 U.S.C. §§ 314(a), 324(a), and 325(d). For example, the PTAB may deny institution if other pertinent circumstances are present, such as abuse of process by a petitioner.

This interim guidance applies to all proceedings pending before the Office. This interim guidance will remain in place until further notice. The Office expects to replace this interim guidance with rules after it has completed formal rulemaking.

¹² The most recent statistics are available at: <https://www.uscourts.gov/statistics/table/na/federal-court-management-statistics/2022/03/31-1>.



(for example, post-fire flooding, landslides, and reburns)?

iv. How might Forest Service land managers build on work with partners to implement adaptation practices on National Forest System lands and in the WUI that can support climate resilience across jurisdictional boundaries, including opportunities to build on and expand Tribal co-stewardship?

v. Eastern forests have not been subject to the dramatic wildfire events and severe droughts occurring in the west, but eastern forests are also experiencing extreme weather events and chronic stress, including from insects and disease, while continuing to rebound from historic management and land use changes. Are there changes or additions to policy and management specific to conservation and climate resilience for forests in the east that the Forest Service should consider?

3. Mature and Old Growth Forests. The inventory required by E.O. 14072 demonstrated that the Forest Service manages an extensive, ecologically diverse mature and old-growth forest estate. Older forests often exhibit structures and functions that contribute ecosystem resilience to climate change. Along with unique ecological values, these older forests reflect diverse Tribal, spiritual, cultural, and social values, many of which also translate into local economic benefits.

Per direction in E.O. 14072, this section builds on the RFI to seek public input on policy options to help the Forest Service manage for future resilience of old and mature forest characteristics. Today there are concerns about the durability, distribution, and redundancy of these systems, given changing climate, as well as past and current management practices, including ecologically inappropriate vegetation management and fire suppression practices. Recent science shows severe and increasing rates of ecosystem degradation and tree mortality from climate-amplified stressors. Older tree mortality due to wildfire, insects and disease is occurring in all management categories.

The Forest Service is analyzing threats to mature and old-growth forests to support policy development to reduce those threats and foster climate resilience. Today's challenge for the Forest Service is how to maintain and grow older forest conditions while improving and expanding their distribution and protecting them from the increasing threats posed by climate change and other stressors, in the context of its multiple-use mandate.

a. How might the Forest Service use the mature and old-growth forest

inventory (directed by E.O. 14072) together with analyzing threats and risks to determine and prioritize when, where, and how different types of management will best enable retention and expansion of mature and old-growth forests over time?

b. Given our current understanding of the threats to the amount and distribution of mature and old-growth forest conditions, what policy, management, or practices would enhance ecosystem resilience and distribution of these conditions under a changing climate?

4. Fostering Social and Economic Climate Resilience.

a. How might the Forest Service better identify and consider how the effects of climate change on National Forest System lands impact Tribes, communities, and rural economies?

b. How can the Forest Service better support adaptive capacity for underserved communities and ensure equitable investments in climate resilience, consistent with the Forest Service's Climate Adaptation Plan, Equity Action Plan and Tribal Action Plan?

c. How might the Forest Service better connect or leverage the contribution of State, Private and Tribal programs to conservation and climate resilience across multiple jurisdictions, including in urban areas and with Tribes, state, local and private landowners?

d. How might the Forest Service improve coordination with Tribes, communities, and other agencies to support complementary efforts across jurisdictional boundaries?

e. How might the Forest Service better support diversified forest economies to help make forest dependent communities more resilient to changing economic and ecological conditions?

Christopher French,

Deputy Chief, National Forest System, Forest Service.

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DEPARTMENT OF COMMERCE

Patent and Trademark Office

37 CFR Part 42

[Docket No. PTO-P-2020-0022]

RIN 0651-AD47

Changes Under Consideration to Discretionary Institution Practices, Petition Word-Count Limits, and Settlement Practices for America Invents Act Trial Proceedings Before the Patent Trial and Appeal Board

AGENCY: United States Patent and Trademark Office, Department of Commerce.

ACTION: Advance notice of proposed rulemaking.

SUMMARY: The United States Patent and Trademark Office (USPTO or Office) is considering modifications to the rules of practice for inter partes review (IPR) and post-grant review (PGR) proceedings before the Patent Trial and Appeal Board (PTAB or Board) to better align the practices with the USPTO's mission to promote and protect innovation and investment in the same, and with the congressional intent behind the American Invents Act (AIA) to provide a less-expensive alternative to district court litigation to resolve certain patentability issues while also protecting against patentee harassment. The USPTO is considering promulgating rules the Director, and by delegation the Board, will use to exercise the Director's discretion to institute IPRs and PGRs; to provide a procedure for separate briefing on discretionary denial that will allow parties to address relevant issues for discretionary denial without encroaching on the pages they are afforded to address the merits of a case; to provide petitioners the ability to pay additional fees for a higher word-count limit; and to clarify that all settlement agreements, including pre-institution settlement agreements, are required to be filed with the Board.

DATES: Comments must be received by June 20, 2023 to ensure consideration.

ADDRESSES: For reasons of Government efficiency, comments must be submitted through the Federal eRulemaking Portal at www.regulations.gov. To submit comments via the portal, one should enter docket number PTO-P-2020-0022 on the homepage and click "search." The site will provide search results listing all documents associated with this docket. Commenters can find a reference to this document and click on the "Comment" icon, complete the required fields, and enter or attach their

comments. Attachments to electronic comments will be accepted in Adobe® portable document format (PDF) or Microsoft Word® format. Because comments will be made available for public inspection, information that the submitter does not desire to make public, such as an address or phone number, should not be included in the comments.

Visit the Federal eRulemaking Portal for additional instructions on providing comments via the portal. If electronic submission of, or access to, comments is not feasible due to a lack of access to a computer and/or the internet, please contact the USPTO using the contact information below for special instructions.

FOR FURTHER INFORMATION CONTACT:

Michael Tierney, Vice Chief Administrative Patent Judge, and Amber Hagy, Lead Administrative Patent Judge, at 571–272–9797.

SUPPLEMENTARY INFORMATION:

Executive Summary

Purpose

The United States Patent and Trademark Office (USPTO or Office) is charged with promoting innovation through patent protection. U.S. Const., art. I, section 8. The patent system fosters technological innovation not only by encouraging the public disclosure of ideas, but also by providing limited time, exclusive rights to the patented innovation and incentivizing research and development and investment in the same, as well as the investment necessary to bring that research and development to market. The patent system is a catalyst for jobs, economic prosperity, and world problem-solving. It works most efficiently and effectively when the USPTO issues and maintains robust and reliable patents. Patents help protect the funds invested in research and development and bring ideas to market. Optimal benefits of the patent system are achieved when inventors and assignees granted patent rights can efficiently engage in technology transfer and licensing (including cross-licensing), obtain funding to bring ideas to market, and/or enforce their rights. The patent system works best when any disputes as to the validity or infringement of patents are addressed efficiently and effectively, and when appropriate steps are taken to curb abusive actions that contravene the Office's mission to promote innovation. Congress recognized those dynamics when it designed the Leahy-Smith America Invents Act (AIA) post-grant proceedings “to establish a more

efficient and streamlined patent system that will improve patent quality and limit unnecessary and counterproductive litigation costs.” H.R. Rep. No. 112–98, part 1, at 40 (2011), 2011 U.S.C.C.A.N. 67, 69; *see* S. Rep. No. 110–259, at 20 (2008).

In designing the AIA, Congress empowered the Director of the USPTO to prescribe regulations related to the implementation of the AIA. Under 35 U.S.C. 316(a) and 326(a), the Director shall prescribe regulations for certain enumerated aspects of AIA proceedings, and under 35 U.S.C. 2(b)(2)(A), the Director may establish regulations that “shall govern the conduct of proceedings in the Office.” 35 U.S.C. 316 and 326. The Director's discretion is informed by 35 U.S.C. 316(b) and 326(b), which require that “the Director shall consider the effect of any such regulation on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted under” 35 U.S.C. 316 and 326. Sections 314(a) and 324(a) of 35 U.S.C. provide the Director with discretion to deny a petition, even when meritorious. *See, e.g.*, 35 U.S.C. 314(a) (stating “[t]he Director may not authorize an *inter partes* review to be instituted unless . . .”); *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 273 (2016) (“[T]he agency's decision to deny a petition is a matter committed to the Patent Office's discretion.”). Congress also provided that in “determining whether to institute [an AIA post-grant proceeding], the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.” 35 U.S.C. 325(d).

The changes under consideration would amend the rules of practice for IPR and PGR proceedings under the AIA. In proposing these changes, the Director has considered the comments received from stakeholders and the public, including in response to the Request for Comments on Discretion to Institute Trials Before the Patent Trial and Appeal Board (85 FR 66502 (Oct. 20, 2020)) (RFC), as well as “the effect of any such regulation on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted under” 35 U.S.C. 316 and 326.

The changes under consideration build on and codify existing precedent and guidance on Director's discretion to determine whether to institute an IPR or PGR. In considering possible changes, it important to keep in mind that, as the

Supreme Court explained in *Cuozzo*, “the purpose of the proceeding is not quite the same as the purpose of district court litigation.” *Cuozzo*, 579 U.S. at 279. As the Court stated, “one important congressional objective” in establishing IPR review is “giving the Patent Office significant power to revisit and revise earlier patent grants.” *Id.* at 272. The “basic purpose[]” of the review is “to reexamine an earlier agency decision”; it “offers a second look at an earlier administrative grant of a patent.” *Id.* at 279. The Court further noted that, under the AIA, “any third party can ask the agency to initiate inter partes review of a patent claim”; “[p]arties that initiate the proceeding need not have a concrete stake in the outcome; indeed, they may lack constitutional standing.” *Id.* at 268, 279. “Thus, in addition to helping resolve concrete patent-related disputes among parties, inter partes review helps protect the public's ‘paramount interest in seeing that patent monopolies . . . are kept within their legitimate scope.’” *Id.* at 279–280 (quoting *Precision Instrument Mfg. Co. v. Automotive Maintenance Machinery Co.*, 324 U.S. 806, 816 (1945)).

The changes under consideration provide that, in certain circumstances in which specific elements are met (and applicable exceptions do not apply), the Director, and by delegation the Board,¹ will exercise the Director's discretion and will deny institution of an IPR or PGR. The USPTO is also considering broadening the types of relationships between petitioners and other entities the Office will consider when evaluating discretionary denial in order to ensure that entities related to a party in an AIA proceeding are fully evaluated with regard to conflicts, estoppel provisions, and other aspects of the proceedings. The Office is also considering whether, in certain circumstances, challenges presenting “compelling merits” will be allowed to proceed at the Board even where the petition would otherwise be a candidate for discretionary denial (as is the current practice under the Director's Memorandum Regarding Interim Procedure for Discretionary Denials in AIA Post-grant Proceedings with Parallel District Court Litigation of June 21, 2022 (discussed below)). In addition, the Office is considering whether to promulgate discretionary denial rules to ensure that certain for-profit entities do not use the IPR and PGR processes in ways that do not advance the mission and vision of the Office to promote

¹ Any reference to the “Board” refers to actions the Board takes by delegation from the Director. Such actions are reviewable by the Director.

innovation or the intent behind the AIA to improve patent quality and limit unnecessary and counterproductive litigation costs.

Recognizing the important role the USPTO plays in encouraging and protecting innovation by individual inventors, startups, and under-resourced innovators who are working to bring their ideas to market, the Office is considering limiting the impact of AIA post-grant proceedings on such entities by denying institution when certain conditions are met. The Office is seeking input on how it can protect those working to bring their ideas to market either directly or indirectly, while not emboldening or supporting economic business models that do not advance innovation. For example, the Office seeks input on to whether to require identification of anyone having an ownership interest in the patent owner or petitioner. The USPTO welcomes thoughts on any additional disclosure requirements needed and how the Board should consider that information when exercising Director discretion.

The Office is also considering additional measures to address the concerns raised by repeated validity challenges to patent claims (potentially resulting in conflicting outcomes and overburdening patent owners). The USPTO is considering further modifying and clarifying circumstances in which the Board will deny review of serial and parallel petitions. As to parallel petitions, the Office is also considering changes to provide that, as an alternative to filing multiple petitions, a petitioner may pay additional fees for a higher word-count limit.

Furthermore, the Office is considering rules related to the framework the Board will use to conduct an analysis under 35 U.S.C. 325(d), which provides that in “determining whether to institute [an AIA post-grant proceeding], the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.”

In addition, the USPTO is considering a rule clarifying that if institution of an IPR is not discretionarily denied in view of any other criteria, the Board shall consider whether to deny institution if there is a pending district court action involving claims challenged in the IPR. In the case of a parallel district court action in which a trial adjudicating the patentability of challenged claims has not already concluded at the time of an IPR institution decision, the USPTO is proposing rules to install *Apple v. Fintiv* and related guidance, with additional

proposed reforms. *See Apple Inc. v. Fintiv, Inc.*, IPR2020–00019, Paper 11, 2020 WL 2126495 (PTAB Mar. 20, 2020) (designated precedential May 5, 2020); Director’s Memorandum Regarding Interim Procedure for Discretionary Denials in AIA Post-grant Proceedings with Parallel District Court Litigation (June 21, 2022) (Guidance Memorandum).² The USPTO is considering separate rules for instances in which a trial adjudicating the validity of challenged claims—in district court or during post-grant proceedings—has already concluded at the time of an IPR institution decision.

The USPTO is also considering a separate briefing process for addressing discretionary denial considerations under 35 U.S.C. 314(a), 324(a), and 325(d) so that briefing on discretionary denial does not encroach on the parties’ word-count limits for briefing on the merits.

Lastly, the USPTO is considering aligning the requirements for terminating proceedings pre- and post-institution by requiring that pre-institution settlement agreements be filed with the Board to support the termination of a proceeding pre-institution.

Background

Development of the Changes Under Consideration

On September 16, 2011, the AIA was enacted into law (Pub. L. 112–29, 125 Stat. 284 (2011)), and in 2012, the USPTO implemented rules to govern Office trial practice for AIA trials, including IPR, PGR, covered business method (CBM), and derivation proceedings pursuant to 35 U.S.C. 135, 316, and 326 and AIA 18(d)(2). *See* Rules of Practice for Trials Before the Patent Trial and Appeal Board and Judicial Review of Patent Trial and Appeal Board Decisions, 77 FR 48612 (Aug. 14, 2012); Changes to Implement Inter Partes Review Proceedings, Post-Grant Review Proceedings, and Transitional Program for Covered Business Method Patents, 77 FR 48680 (Aug. 14, 2012); Transitional Program for Covered Business Method Patents—Definitions of Covered Business Method Patent and Technological Invention, 77 FR 48734 (Aug. 14, 2012). Additionally, the USPTO published a Patent Trial Practice Guide for the rules to advise the public on the general framework of the regulations, including the structure and times for taking action in each of the

new proceedings. *See* Office Patent Trial Practice Guide, 77 FR 48756 (Aug. 14, 2012). Since then, the USPTO has designated numerous decisions in such proceedings as precedential or informative, has issued several updates to the Trial Practice Guide, and has issued guidance including the June 2022 Guidance Memorandum.

Prior Request for Comments Regarding Discretionary Institution

On October 20, 2020, the USPTO published an RFC to obtain feedback from stakeholders on case-specific approaches by the PTAB for exercising discretion on whether to institute an AIA proceeding and whether the USPTO should promulgate rules based on these approaches. *See* Request for Comments on Discretion to Institute Trials Before the Patent Trial and Appeal Board, 85 FR 66502 (Oct. 20, 2020). The USPTO published an Executive Summary in January 2021, encapsulating stakeholder feedback received from the RFC.³ The USPTO received 822 comments from a wide range of stakeholders, including individuals, associations, law firms, companies, and three United States Senators. In view of the comments in response to the RFC and the USPTO’s further experience with AIA proceedings, the USPTO intends to make policy changes through notice-and-comment rulemaking. Such rulemaking is consistent with comments received from stakeholders, made in response to the RFC as well as in other contexts, expressing a preference that key policy changes be made and formalized through rulemaking.

Director’s Discretionary Institution Authority in General

By way of background, the Board institutes an AIA trial on behalf of the Director. 37 CFR 42.4(a). In deciding whether to institute an AIA trial, the Board considers, at a minimum, whether a petitioner has satisfied the relevant statutory institution standard. Sections 314(a) and 324(a) of 35 U.S.C. provide the Director with discretion to deny a petition, even when meritorious. *See, e.g.*, 35 U.S.C. 314(a) (stating “[t]he Director may not authorize an *inter partes* review to be instituted unless . . .”); *Cuozzo*, 579 U.S. at 273 (“[T]he agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.”). In addition, 35

² https://www.uspto.gov/sites/default/files/documents/interim_proc_discretionary_denials_aia_parallel_district_court_litigation_memo_20220621_.pdf.

³ USPTO, Executive Summary: Public Views on Discretionary Institution of AIA Proceedings (Jan. 2021). Available at www.uspto.gov/sites/default/files/documents/USPTOExecutiveSummaryofPublicViewsonDiscretionaryInstitutionofAIAProceedingsJanuary2021.pdf.

U.S.C. 325(d) provides that “[i]n determining whether to institute or order a proceeding . . . , the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.”

Under 35 U.S.C. 316(a) and 326(a), the Director shall prescribe regulations for certain enumerated aspects of AIA proceedings, and under 35 U.S.C. 2(b)(2)(A), the Director may establish regulations that “shall govern the conduct of proceedings in the Office.” The Director’s discretion to institute review of a patent is informed by 35 U.S.C. 316(b) and 326(b), which require the Director to “consider the effect of any such regulation [under this section] on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted under this chapter.”

Congress designed the AIA to improve and ensure patent quality by providing “quick and cost-effective alternatives to litigation” for challenging issued patents. H.R. Rep. No. 112–98, part 1, at 48 (2011), 2011 U.S.C.C.A.N. 67, 69; see S. Rep. No. 110–259, at 20 (2008) (explaining that the “post-grant review system . . . will give third parties a quick, inexpensive, and reliable alternative to district court litigation to resolve questions of patent validity”). In so doing, Congress granted the USPTO “significant power to revisit and revise earlier patent grants” as a mechanism “to improve patent quality and restore confidence in the presumption of validity that comes with issued patents.” *Cuozzo*, 579 U.S. at 272 (quoting H.R. Rep. No. 112–98, part 1, at 45, 48). At the same time, Congress instructed that “the changes made by [the AIA] are not to be used as tools for harassment or a means to prevent market entry through repeated litigation and administrative attacks on the validity of a patent,” and “[d]oing so would frustrate the purpose of the section as providing quick and cost effective alternatives to litigation.” H.R. Rep. No. 112–98, at 48 (2011).

To take into account the 35 U.S.C. 316(b) and 326(b) considerations of the economy, the integrity of the patent system, and the ability of the USPTO to provide timely and cost-effective PGRs, as outlined in the AIA, the USPTO has developed factors to consider when determining whether to institute an AIA review under several different circumstances, including when: (1) additional petitions are filed by the same petitioner or sufficiently related

parties challenging the same patent claims as a first petition after the patent owner has filed a preliminary response to the first petition (“serial” or “follow-on” petitions); (2) a petition relies on substantially the same prior art, and/or invokes the same or substantially the same arguments, previously addressed by the USPTO in connection with the challenged patent (implicating considerations under 35 U.S.C. 325(d)); (3) more than one petition is filed by the same petitioner (or privy or real party in interest with a petitioner) at the same time as the first filed petition or up until the filing of the preliminary response in the first filed proceeding (“parallel petitions”); and (4) a petition is filed in parallel with an ongoing district court proceeding (“parallel proceedings”).

As noted above, in late 2020, the USPTO received 822 comments in response to an RFC on certain discretionary institution considerations set forth in precedential Board decisions. Comments from stakeholders generally supported discretionary institution rulemaking, although the comments differed as to the specifics. The substance of the public comments is discussed below in connection with the proposed changes.

Discussion of Changes Under Consideration

The following is a discussion of the amendments under consideration for 37 CFR part 42.

Overview

In order to create clear, predictable rules where possible, as opposed to balancing tests that decrease certainty, the USPTO is considering changes that would provide for discretionary denials of petitions in the following categories, subject to certain conditions and circumstances (and exceptions) as discussed further below:

1. Petitions filed by certain for-profit entities;
2. Petitions challenging under-resourced patent owner patents where the patentee has or is attempting to bring products to market;
3. Petitions challenging patent claims previously subject to a final adjudication upholding the patent claims against patentability challenges in district court or in post-grant proceedings before the USPTO;
4. Serial petitions;
5. Petitions raising previously addressed prior art or arguments (subject to the 35 U.S.C. 325(d) framework);
6. Parallel petitions; and

7. Petitions challenging patents subject to ongoing parallel litigation in district court.

The changes under consideration also provide for several threshold definitions that apply to one or more of these categories of petitions subject to discretionary denials. Those definitions set forth the criteria used to determine: (1) what constitutes a “substantial relationship” between entities sufficient to trigger or avoid discretionary denial, (2) when claim sets are deemed to have “substantial overlap” with challenged claims, and (3) what constitutes “compelling merits” sufficient to trigger an exception to discretionary denial.

Finally, five additional changes are being considered: (1) absent exceptional circumstances, requiring petitioners to file a stipulation that neither they nor their privy or real parties have filed prior post-grant proceedings (PGRs, IPRs, CBMs or ex parte reexaminations) on the challenged claims; and that if their post-grant proceeding is instituted, neither they nor their privy or real parties in interest, will challenge any of the challenged claims in a subsequent post-grant proceeding (including PGRs, IPRs and ex parte reexamination); (2) requiring petitioners to file a separate paper justifying multiple parallel petitions; (3) allowing a potential payment of a fee to enhance the word-count limits for a petition to avoid multiple parallel petitions; (4) providing for separate briefing on discretionary denial issues; and (5) requiring filing of all settlement papers when the dismissal of AIA proceedings is sought, whether pre- or post-institution.

The USPTO welcomes public comments and feedback on all changes under consideration, which are discussed in detail below. The USPTO further welcomes any responses that address the effect any of the proposals herein would have on “the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted under” 35 U.S.C. 316 and 326. Some of the changes under consideration are set forth as alternative proposals. The USPTO appreciates feedback on the relative benefits and drawbacks, if any, of the alternatives proposed. The USPTO also invites suggestions on what, if any, additional disclosures the USPTO should require and any other considerations the USPTO should take into account that would weigh in favor of or against discretionary denial.

*Threshold Definitions**“Substantial Relationship” of Entities*

The USPTO currently applies the common law formulations of “real party in interest” and “privity” to ensure that entities related to a party in an AIA proceeding are considered when evaluating conflicts and the effect of estoppel provisions. *See* Consolidated Trial Practice Guide, 12–18 (Nov. 2019). For example, relationships based on corporate structure, contract, or financial interest are often considered in identifying real parties in interest or those in privity with a party to the proceedings.

The USPTO has adopted similar considerations in the discretionary denial context. For example, in *Valve Corp. v. Electronic Scripting Products, Inc.*, IPR2019–00062, –00063, –00084, 2019 WL 1490575 (PTAB Apr. 2, 2019) (precedential) (*Valve I*), the Board denied institution when a party, Valve, filed multiple petitions for IPR after the denial of an IPR request of the same claims filed by the party’s co-defendant in district court, whose accused products incorporated technology licensed from Valve. *Valve I*, 2019 WL 1490575, at *4–5. The Board held that when different petitioners challenge the same patent, the Board considers the relationship, if any, between those petitioners in weighing the factors in *General Plastic Co. v. Canon Kabushiki Kaisha*, IPR2016–01357, Paper 19 (PTAB Sept. 6, 2017) (precedential) (*General Plastic*). *Id.* The USPTO also explained, in *Valve Corp. v. Electronic Scripting Products, Inc.*, IPR2019–00064, –00065, –00085, 2019 WL 1965688 (PTAB May 1, 2019) (*Valve II*), that the first *General Plastic* factor applies to a later petitioner when that petitioner previously joined an instituted IPR proceeding and, therefore, was considered to have previously filed a petition directed to the same claims of the same patent. *Valve II*, 2019 WL 1965688, at *4–5.

However, the current party relationship concepts applied in the discretionary denial context are arguably too limited in certain circumstances. Accordingly, the USPTO is considering adopting a “substantial relationship” test to evaluate whether certain entities are sufficiently related to a party in an AIA proceeding such that discretionary denial is warranted under the criteria set forth in the changes under consideration. The substantial relationship test would be broadly construed and would encompass, but not be limited to, real parties in interest or privies of the party to the AIA proceeding, and would also include

others that are significantly related to that party, including at least those entities as discussed in *Valve I* and *Valve II*.

The USPTO is also considering other proposals for deeming entities to be substantially related for purposes of discretionary denials. For example, one proposal is to consider those involved in a membership organization, where the organization files IPRs or PGRs, as having a substantial relationship with the organization. There may be instances in which entities may pool their resources to challenge a patent. For example, where multiple entities are defending infringement claims in district court litigation, or have related interests in challenging the patentability of patent claims, they may join together to file a single challenge to the subject patent claims before the PTAB. Such activities may advance the Office’s mission and vision and the congressional intent behind the AIA where the entities are in privity with a party or are, themselves, real parties in interest, and where their involvement in the proceeding is consistent with the statutory provisions or the Office’s rules, including those related to estoppel or multiple challenges to a patent. In the interests of transparency, the Office would require disclosure of any such relationships by a party upon filing its first paper in an IPR or PGR and would require parties to promptly file a supplemental statement if the information changes.

Another proposal under consideration is requiring a patent owner and petitioner to disclose anyone with an ownership interest in the patent owner or petitioner, any government funding related to the patent, any third-party litigation funding support (including funding for some or all of the patent owner’s or petitioner’s attorney fees or expenses before the PTAB or district court), and any stake any party has in the outcome of the AIA proceeding or any parallel proceedings on the challenged claims. For example, the Office could require parties to disclose beneficial ownership interests similar to what the Securities and Exchange Commission requires.

“Substantial Overlap” Between Claim Sets

As discussed further below, for certain discretionary denial decisions the USPTO would consider whether there is “substantial overlap” between claim sets (for example, those previously adjudicated to not be invalid) and the challenged claims. Under the proposed changes, the Office is considering a clear, predictable

definition in which claim sets are deemed to “substantially overlap” the challenged claims when at least one challenged claim is “substantially the same” as a claim in a set to which the claim is being compared. For purposes of this comparison, claims will be deemed to be “substantially the same” when any differences between the claims are not material to patentability. Alternatively, the Office is open to considering a more subjective test in which substantial overlap between claim sets is determined on a case-by-case basis.

The Office requests comments on other possible tests for determining when claim sets will be considered to “substantially overlap” the challenged claims including what degree of overlap (*i.e.*, number of claims) would amount to “substantial overlap” and whether one overlapping claim should be sufficient.

Effect of “Compelling Merits” on Discretionary Denials

The changes under consideration would provide that, in certain circumstances, when a challenge presents compelling merits the proceeding will be allowed to proceed at the Board even where the petition would otherwise potentially be a candidate for discretionary denial. A challenge presents “compelling merits” when the evidence of record before the Board at the institution stage is highly likely to lead to a conclusion that one or more claims are unpatentable by a preponderance of the evidence. *See OpenSky Indus., LLC v. VLSI Tech. LLC*, IPR2021–01064, Paper 102 at 49 (PTAB Oct. 4, 2022) (Director decision, precedential) (describing compelling merits as those that “plainly lead to a conclusion that one or more claims are unpatentable,” and noting that such standard can be met only “if it is highly likely that the petitioner would prevail with respect to at least one challenged claim”). Under this test, the petitioner has the burden of presenting evidence at the institution stage that leaves the Board with a firm belief or conviction that it is highly likely that the petitioner would prevail with respect to at least one challenged claim. Consistent with the intent of the AIA and our mission, it is only this high certainty that would compel the Board to review claims for the public benefit when other considerations favor discretionary denial.

A compelling merits standard is a higher standard than the reasonable likelihood required for the institution of an IPR under 35 U.S.C. 314(a), and higher than more likely than not

required for institution of a PGR under 35 U.S.C. 324(a). The compelling merits standard is also higher than the preponderance of the evidence standard (more likely than not) that applies to final determinations of patentability at the close of trial. But because all relevant evidence likely will not have been adduced at the point of institution, a determination of “compelling merits” at the institution stage should not be taken as a signal to the ultimate conclusion after trial. *See OpenSky Indus.*, IPR2021–01064, Paper 102 at 49. The Board would provide its reasoning in determining whether the merits of a petition are compelling. Further, the Board would not reach any issue regarding “compelling merits” until all other discretionary denial issues have been evaluated and the petition is a candidate for discretionary denial.

The compelling merits test seeks to strike a balance among the competing concerns of avoiding potentially conflicting outcomes, avoiding wasteful parallel proceedings, protecting against patent owner harassment, and strengthening the patent system by allowing the review of patents challenged with a sufficiently strong initial merits showing of unpatentability. The patent system and the public could benefit from instituting challenges with a showing of unpatentability by compelling merits. The USPTO is also considering whether the compelling merits standard is the most appropriate standard for the Board to apply at the institution stage when determining if the merits of a petition are sufficiently strong to avoid discretionary denial.

The Office also requests comments on how the compelling merits standard would apply if the patent owner raises a factual question that cannot be resolved at institution (e.g., presenting evidence of secondary considerations of nonobviousness). In particular, the Office seeks feedback on what presumptions should apply and whether pre-institution discovery would be appropriate. The Office is considering whether, in assessing compelling merits, the Office should adopt a test whereby (1) the record will be viewed in the light most favorable to the patent owner and (2) the Board will draw all reasonable inferences in favor of patent owner.

Lastly, the Office is considering whether the compelling merits standard should apply as an exception to all of the bases for discretionary denial discussed below and, if not, which ones it should and should not apply to. Under current USPTO guidance, the compelling merits test does not apply

when certain entities are attempting to challenge a patent after a final adjudication of patentability in post-grant proceedings or in district court or when serial challenges are being made by the same party or a real party in interest or privy.

Discretionary Denials Under 35 U.S.C. 314(a), 324(a), and 325(d)

In the AIA, Congress established post-grant proceedings, including IPR, PGR, and CBM proceedings,⁴ to improve and ensure patent quality by providing “quick and cost-effective alternatives to litigation” for challenging issued patents. H.R. Rep. No. 112–98, part 1, at 48; *see also* S. Rep. No. 110–259, at 20 (explaining that the “post-grant review system . . . will give third parties a quick, inexpensive, and reliable alternative to district court litigation to resolve questions of patent validity”). Congress granted the Office “significant power to revisit and revise earlier patent grants” as a mechanism “to improve patent quality and restore confidence in the presumption of validity that comes with issued patents.” *Cuozzo*, 579 U.S. at 272 (quoting H.R. Rep. No. 112–98, part 1, at 45, 48). Given those objectives, the changes under consideration, in addition to providing clear rules for when the Board would exercise its discretion to deny institution, would also clarify that the Office always retains discretion to deny institution as a sanction or in response to improper conduct or gamesmanship.

Limitations on Nonmarket Competitors—Petitions Filed by Certain For-Profit Entities

The Office received feedback in the comments responsive to the RFC expressing concerns that some petitions are filed by for-profit entities who had not been sued for infringement and may not have an apparent reason for challenging validity of patent claims. The USPTO is likewise concerned that certain for-profit entities may use the IPR and PGR processes not to advance the mission and vision of the Office to promote innovation or the intent behind the AIA to provide a less-expensive alternative to district court litigation, but instead to advance other interests. To curb the potential for abusive filings, the USPTO is considering changes that would limit institution on filings by for-profit, non-competitive entities that in essence seek to shield the actual real

parties in interest and privies from statutory estoppel provisions. The changes under consideration would make clear that the Board would discretionarily deny any petition for IPR or PGR filed by an entity that: (1) is a for-profit entity; (2) has not been sued on the challenged patent or has not been threatened with infringement of the challenged patent in a manner sufficient to give rise to declaratory judgment standing; (3) is not otherwise an entity that is practicing, or could be alleged to practice, in the field of the challenged patent with a product or service on the market or with a product or service in which the party has invested to bring to market; and (4) does not have a substantial relationship with an entity that falls outside the scope of elements (1)–(3). The Office contemplates defining “for-profit entities” as entities that do not qualify for tax-exempt status with the Internal Revenue Service.

The USPTO is considering defining “for-profit” entities to include any entity that is a real party in interest with, or in privy with, a for-profit entity. The Office is alternatively considering “for-profit” entities to additionally include any parties with a substantial relationship with a for-profit entity.

The USPTO is seeking feedback on whether it should discretionarily deny an IPR or PGR if the patent owner provides a covenant not to sue to a for-profit petitioner and its customers prior to initiating litigation against those entities. In addition, the USPTO requests comments on whether it should consider any other covenant or stipulation in determining whether to exercise discretion to deny institution.

As to the second element, “has not been sued on the challenged patent,” the Office is considering whether the element should be further defined such that the Board will not discretionarily deny petitions filed by entities that have been threatened with infringement of the challenged patent in a manner sufficient to give rise to declaratory judgment standing. Alternatively, the Office is open to considering whether a petition should be denied where a petitioner lacks declaratory judgment standing, but the petitioner has a reasonable apprehension of suit based on the prior litigation conduct of the patentee asserting the patent or related patents against similarly situated companies.

Regarding the third element, under this proposal the Board is considering the metes and bounds of prior attempts to commercialize and how to define the term so that it encompasses efforts to bring products to market. The Office requests comments on whether and

⁴ The transitional covered business method patent review program expired on September 16, 2020, in accordance with AIA 18(a)(3). Although the program has sunset, existing CBM proceedings based on petitions filed before September 16, 2020, are still pending.

when activity by another should inure to the benefit of a petitioner. The Office is proposing the language “field of the challenged patent” to avoid a dispute about whether the petitioner practices the challenged claims or patent.

Regarding the fourth element, the USPTO understands there may be instances in which entities may pool resources to challenge a patent. For example, where multiple entities are defending infringement claims in district court litigation, or have related interests in challenging the patentability of patent claims, they may join together to challenge the subject patent claims before the PTAB. Such activity may advance the Office’s mission and vision and the congressional intent behind the AIA so long as the entities are real parties in interest or in privy, such that the activity does not work to avoid the effect of statutory provisions or the Office’s rules, including those related to estoppel and/or multiple challenges to a patent.

The USPTO is also considering whether, even if the petitioner is an entity satisfying the four elements discussed above, the Office should institute petitions where the petitioner satisfies a heightened standard of demonstrating compelling merits.

Micro and Small Entities: Protecting Under-Resourced Inventors and Petitioners

The USPTO recognizes that the contributions of startups, small businesses, and independent inventors are vital to the development of a variety of important American industries. They are the engines that, in many cases, drive innovation. The Office also recognizes that such entities may have limited resources that are necessarily devoted to crucial activities such as research, development, and manufacturing.

Such limited resources may impact the perceived fairness of post-grant reviews. For example, some stakeholders in response to the RFC expressed concern that under-resourced inventors are unable to afford the costs involved in defending patents in post-grant review. Some stakeholders advocating for small businesses and individual inventors urged the Office to take into account the financial resources of a patent owner, and to limit reviews of patents owned by under-resourced entities who lack funding to defend challenges to their patents but who have sought to bring their inventions to market either themselves or through a licensee.

Because providing support for startups, small businesses, and

independent inventors is one of the major priorities for the USPTO, the Office proposes to limit the impact of AIA post-grant proceedings on these patent owners by discretionarily denying petitions for an IPR or PGR when certain other conditions are met.

Specifically, under one proposal, absent compelling merits, the status of the patent owner would lead to a denial of institution when: (1) the patent owner had claimed micro entity or small entity status at issuance of the challenged patent and timely requested discretionary denial when presented with the opportunity; (2) during the calendar year preceding the filing of the petition, the patent owner did not exceed eight times the micro entity gross income level under 37 CFR 1.29(a)(3); and (3) at the time the petition was filed, the patent owner (or a licensee of the patent that started practicing the patent after becoming a licensee) was commercializing the subject matter of a challenged claim.

Under this proposal, to allow for growth between the time the patent issued and the filing of the petition, the changes under consideration would apply to entities that were micro or small entities at patent issuance but are under-resourced (as defined by a gross income requirement) at the time of filing the petition. The reduction to practice and commercialization requirement is intended to encourage the creation of new businesses and competition in the marketplace.

The USPTO welcomes any other proposals that will provide protections for startups, small businesses, and independent inventors, and recognizes it is not only those with limited resources that benefit our economy. At the same time, the Office wants to address competing concerns about spurious litigation and abusive practices. Due to the large variety of business models, it is difficult to draw widely applicable bright lines. The Office welcomes proposals to protect startups, small businesses, and independent inventors beyond those who are under-resourced to the extent the remainder of these proposed rules do not provide adequate protection. As an example, the Office is considering whether a multiplier of eight times the micro entity gross income level, or some other multiplier, would be appropriate to help the Office to ensure that it is reaching under-resourced individual inventors and start-ups (and not those funded or otherwise supported by an entity who is neither). The Office also is considering other possible approaches, including whether a limited-resource entity should be

required at the time of the petition to meet the micro or small entity provisions under 37 CFR 1.27 and 1.29. The Office welcomes comments on how the office should define “under-resourced” and whether the Office should include other criteria other than income. For example, the Office could consider a petitioner under-resourced if, at the time of petition filing, the petitioner is a small or micro entity not exceeding a specified gross income level and has been accused of making, using, selling or offering to sell in the United States, or importing into the United States the subject matter of a challenged claim. An accused petitioner is a petitioner having declaratory judgment standing under 28 U.S.C. 2201(a). *See MedImmune, Inc. v. Genentech, Inc.*, 549 U.S. 118 (2007).

To protect against government-owned or -funded entities using this section to attempt to insulate their patents, and/or to avoid abuse, for any measure that inures to the benefit of patent owners with limited resources, a consideration could include determining whether the small or micro entity has government funding. The Office could also consider third-party litigation funding support, including funding for some or all of the patent owner’s attorney fees or expenses before the PTAB or district court. The Board could also consider the resources of anyone with an ownership interest in the patent owner and anyone with any stake in the outcome of the AIA proceeding or any parallel proceedings on the challenged claims. For example, a small or micro entity requesting denial of institution based on limited resources could be required to disclose the identity of any third-party funders, including U.S. or foreign government funding; provide a brief description of the financial interest of the third-party funder; and state whether the funder’s approval is required for settlement or any positions taken before the PTAB. The PTAB could also inquire into all ownership interests to ensure this process is not abused. This information would not be used in any way other than to determine if an entity is truly under-resourced.

Other options the Office is considering include excluding from consideration the activities of licensees in certain circumstances. The Office welcomes comments on whether certain licenses activities should be excluded, keeping in mind that the USPTO wants to encourage bringing ideas to market whether directly or through technology transfer, licensing, or cross-licensing activities.

Additionally, the Office is considering how to proceed with discretionary

denials where a petitioner is under-resourced. The Office welcomes comments on whether the resource status of a petitioner should be a consideration when analyzing discretionary denials.

Prior Adjudications Upholding Validity

Comments by some stakeholders in response to the RFC emphasized that if a district court reaches a decision on patentability of a patent claim before a final decision can be reached in a parallel IPR proceeding, the benefits of the IPR (a cheaper, quicker, more efficient alternative to litigation) are not likely to be realized. According to these stakeholders, this point is even more salient in instances in which a patent claim has already been subject to an adjudication upholding the validity of the claim prior to the filing of a petition challenging that claim.

The changes under consideration would provide that prior final adjudications by a district court or by the Office in AIA post-grant proceedings upholding the validity of claims that substantially overlap the challenged claims will result in discretionary denial, except in cases in which the petitioner has standing to challenge the validity of the claims in district court or intends to pursue commercialization of a product or service in the field of the invention of a challenged claim, was not a real party in interest or privy to the party previously challenging one or more of the challenged claims (unless any earlier challenge was resolved for reasons not materially related to the merits of the petition, *e.g.*, a post-grant proceeding that was discretionarily denied or otherwise was not evaluated on the merits); and meets a heightened burden of compelling merits.

For clarity, the changes under consideration would also add a definition of “final adjudication” as a decision on the merits by a district court that is final within the meaning of 28 U.S.C. 1295(a)(1). This means that only prior adjudications of invalidity challenges in district court that are on the merits and are part of a final, appealable judgment would be within the scope of the changes under consideration. Similarly, a final adjudication at the Office would be a final, appealable decision of the Office. The Board should first determine whether a petitioner meets the first three criteria—standing, intent to commercialize and privy/real party in interest—before moving to the compelling merits analysis.

These considerations do not replace other limitations on serial petitions or other mechanisms for discretionary

denial, or the *Fintiv* analysis itself if there is, additionally, a parallel proceeding ongoing, but present an additional, independent basis for discretionary denial.

The Office is also considering whether to extend this proposal to including prior adjudications of validity through ex parte reexaminations requested by a third party other than the patent owner or the patent owner’s real party in interest or privy.

Serial Petitions

Serial petitioning occurs when additional petitions are filed challenging at least one claim previously challenged in a first petition: (1) after the filing of a preliminary response in a first petition challenging the same claims; or (2) if no preliminary response to the first petition is filed, after the expiration of the period for filing such a response under 37 CFR 42.107(b) or as otherwise ordered.⁵ In responding to the RFC, some stakeholders expressed concern that duplicative attacks on the same patent through the IPR process devalue the patent. The Office is considering revising the rules to address serial petitioning.

In *General Plastic Co. v. Canon Kabushiki Kaisha*, IPR2016–01357, 2017 WL 3917706, at *7 (PTAB Sept. 6, 2017) (precedential), the Board referred to the goals of the AIA but also “recognize[d] the potential for abuse of the review process by repeated attacks on patents.” 2017 WL 3917706, at *7 (citing H.R. Rep. No. 112–98, part 1, at 48 (2011)). To aid the Board’s assessment of “the potential impacts on both the efficiency of the *inter partes* review process and the fundamental fairness of the process for all parties,” *General Plastic* identified a number of non-exclusive factors that the Board will consider in exercising discretion in instituting an IPR, especially as to “follow-on” petitions challenging the same patent as challenged previously in an IPR, PGR, or CBM proceeding. *Id.* at *8. The *General Plastic* non-exclusive factors include: (1) whether the same petitioner previously filed a petition directed to the same claims of the same patent; (2) whether, at the time of filing of the first petition, the petitioner knew of the prior art asserted in the second petition or

should have known of it; (3) whether, at the time of filing of the second petition, the petitioner had already received a patent owner preliminary response (if filed) to the first petition or received the Board’s decision on whether to institute review in the first petition; (4) the length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition; and (5) whether the petitioner provides an adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent. *Id.* at *7. Additional factors include (6) the finite resources of the Board; and (7) the requirement to issue a final determination not later than 1 year after the date on which the Director notices institution of review. *Id.*

Since *General Plastic*, the Office has explained that the application of the first *General Plastic* factor is not limited to instances in which multiple petitions are filed by the same petitioner. For example, in *Valve I*, the Board denied institution when a party filed serial petitions for IPR after the denial of an IPR request of the same claims filed by the party’s co-defendant. *Valve I*, 2019 WL 1490575, at *4–5. The Board held that when different petitioners challenge the same patent, the Board considers the relationship, if any, between those petitioners when weighing the *General Plastic* factors. *Id.* The Office also explained, in *Valve II*, that the first *General Plastic* factor applies to a later petitioner when that petitioner previously joined an instituted IPR proceeding and, therefore, was considered to have previously filed a petition directed to the same claims of the same patent. *Valve II*, 2019 WL 1965688, at *4–5. The relationships between petitioners in serial petition scenarios depend on the circumstances. Additionally, “*General Plastic* factor 1 must be read in conjunction with factors 2 and 3.” *Code 200 v. Bright Data Ltd.*, IPR2022–00861, Paper 18 at 5 (PTAB Aug. 23, 2022) (Director decision, precedential). “Where the first-filed petition under factor 1 was discretionarily denied or otherwise was not evaluated on the merits, factors 1–3 only weigh in favor of discretionary denial when there are ‘road-mapping’ concerns under factor 3 or other concerns under factor 2.” *Id.*

The USPTO is considering replacing factors 1–7 with the following test, which incorporates the USPTO’s case law on factor 1. Under the proposal, the Board will discretionarily deny—subject to two exceptions—any serial IPR or PGR petition⁶ (with at least one

⁵ See Analysis of multiple petitions in AIA Proceedings (December 2020 update), www.uspto.gov/sites/default/files/documents/multiple_petition_mta_study_.pdf (noting that in fiscal year (FY) 2020, about 2% of AIA challenges (21 out of 938) were serial petitions, and a fraction of those (7) were successful); see also *id.* at slides 8 and 9 (describing what led to a successful serial petition in FY 2020).

challenged claim that is the same as a challenged claim in a previously filed IPR, PGR, or CBM petition) that is filed by one of the following: the same petitioner, a real party in interest or privy to that petitioner, a party with a significant relationship to that petitioner (as discussed in *Valve I*⁷), or a party who previously joined an instituted IPR or PGR filed by that petitioner (as discussed in *Valve I*⁸). The two exceptions are that the Board will not discretionarily deny such a petition when: (1) the earlier petition was resolved for reasons not materially related to the merits of the petition (e.g., was discretionarily denied or otherwise was not evaluated on the merits); or (2) exceptional circumstances are shown. Exceptional circumstances may, for example, include (a) situations in which a patentee changes the scope of the claims, for example, through amendment or a proposed claim construction; (b) situations where, at the time of filing of the first petition, the petitioner reasonably could not have known of or found the prior art asserted in the serial petition; or (c) situations in which the petitioner raises a new statutory challenge (35 U.S.C. 101, 112, or 102/103) that was not in the prior petition and has a justifiable explanation for why they did not raise the statutory challenge in the earlier petition.

This approach to serial petitions could simplify the process for analyzing such petitions and provide greater clarity and certainty to the parties regarding whether subsequent petitions will be instituted. The Office requests comments on this approach, including how it should define “exceptional circumstances” and whether it should use the “at least one overlapping claim” test or whether it should use the “substantial overlap” of claims test.

The Office is also considering whether to apply the substantial relationship test instead of limiting discretionary denial of serial petitions to those filed by the same petitioner, a real party in interest or privy to that petitioner, a party with a significant relationship to that petitioner, as discussed in *Valve I*, or a party who previously joined an instituted IPR or PGR filed by that petitioner, as discussed in *Valve II*. The Office also welcomes thoughts on whether the Office should discretionarily deny any serial petition, regardless of the relationship to the first petitioner, unless the petition meets the compelling merits test. The Office also welcomes comments on how the Office should define exceptional circumstances.

35 U.S.C. 325(d) Framework

Under 35 U.S.C. 325(d), in “determining whether to institute [an AIA post-grant proceeding] the Director⁶ may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.”

In evaluating the exercise of discretion to deny institution under 35 U.S.C. 325(d), the Board applies the two-part framework set forth in the precedential *Advanced Bionics* decision, which entails: (1) determining whether the same or substantially the same art was previously presented to the Office or whether the same or substantially the same arguments were previously presented to the Office; and (2) if either condition of the first part of the framework is satisfied, determining whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims. *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019–01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential).

In applying the two-part framework, the Board has also considered several non-exclusive factors set forth in the precedential *Becton, Dickinson* decision, including (a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; (d) the extent of the overlap between the arguments made during examination and the manner in which the petitioner relies on the prior art or the patent owner distinguishes the prior art; (e) whether the petitioner has pointed out sufficiently how the examiner erred in its evaluation of the asserted prior art; and (f) the extent to which additional evidence and facts presented in the petition warrant reconsideration of the prior art or arguments. *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017–01586, Paper 8 at 17–18 (PTAB Dec. 15, 2017) (precedential as to section III.C.5, first paragraph).

Factors (a), (b), and (d) of *Becton, Dickinson* relate to whether the art or arguments presented in the petition are the same or substantially the same as those previously presented to the Office. *Advanced Bionics*, Paper 6 at 10.

⁶ The Board institutes trial on behalf of the Director. 37 CFR 42.4(a).

Factors (c), (e), and (f) “relate to whether the petitioner has demonstrated a material error by the Office” in its prior consideration of that art or arguments. *Id.* Under *Advanced Bionics*, only if the same or substantially the same art or arguments were previously presented to the USPTO does the Office then consider whether the petitioner has demonstrated a material error by the Office. *Id.*

Although 35 U.S.C. 325(d) was not the specific focus of the RFC, in response to a general question about the Board’s use of discretion some stakeholders suggested that the Office promulgate rules for evaluating whether to proceed with an AIA review in view of 35 U.S.C. 325(d) based on the framework set forth in *Advanced Bionics* and *Becton, Dickinson*.⁷ To promote more consistency, clarity, and efficiency, the USPTO is proposing to promulgate rules directed at how the Board will conduct an analysis under 35 U.S.C. 325(d). While the considered changes reflect many of the underlying principles of *Advanced Bionics* and *Becton, Dickinson*, the Office intends to further clarify the application of 35 U.S.C. 325(d) to supersede the guidance provided in these cases in order to implement the intent of the AIA—to improve patent robustness and reliability—while providing appropriate deference to USPTO decisions on art or arguments previously before the Office.

The USPTO is considering limiting the application of 35 U.S.C. 325(d) to situations in which the Office previously addressed the prior art or arguments. Art or arguments would be deemed to have been previously addressed where the Office evaluated the art or arguments and articulated its consideration of the art or arguments in the record. For example, for the art to be deemed “previously addressed,” the claims must have been distinguished over the art in the record where the art was the basis of a rejection where the rejection was withdrawn or overcome by an amendment, was distinguished in a notice of allowance, or was discussed during an examiner interview. The mere citation of a reference on an Information Disclosure Statement (whether or not checked off by an examiner), in a Notice of References Cited (PTO–892) during prosecution of the challenged patent, or in search results would not be considered sufficient to be deemed “previously addressed” for purposes of 35 U.S.C. 325(d). Requiring that the art

⁷ Response from the American Intellectual Property Law Association at 10–11; response from the Intellectual Property Owners Association at 6–7.

be previously addressed increases efficiency and lowers the cost of proceedings for parties and the Board by providing a clear test that reduces unnecessary briefing.

The Office seeks to clarify that 35 U.S.C. 325(d) applies to art or arguments that were previously addressed during proceedings pertaining to: (1) the challenged patent; or (2) any parent application or other family member application of a challenged patent, but only if the claims of the parent application or other family member application contain or contained substantially the same limitations as those at issue in the challenged claims. If a patent owner makes an argument under 35 U.S.C. 325(d) based on art or arguments presented in a related application, the patent owner should identify how the claims of the related application and the challenged patent are substantially the same. For example, the patent owner may show that the challenged claims received an obviousness-type double patenting rejection over the claims of the parent and a terminal disclaimer was filed to overcome the rejection.

In the current proposal, 35 U.S.C. 325(d) would apply to art or arguments from related applications (if the claims are substantially the same) but would not apply to art or arguments that were addressed in any non-related applications. However, the Office is soliciting comments on whether there are benefits to limiting the application of 35 U.S.C. 325(d) to art or arguments that were previously addressed during proceedings pertaining only to the challenged patent (and not to any parent or related application, including child applications) or, alternatively, expanding the application of 35 U.S.C. 325(d) to non-related applications that were before the Office prior to the issuance of the challenged patent.

Further, under the proposal, prior art will be considered to be “substantially the same” only if the disclosure in the prior art previously addressed contains the same teaching relied upon in the petition and that teaching was addressed by the Office, whether it be a patent or a printed publication in an IPR or another type of prior art available in a PGR. For example, a U.S. national stage filing of a Patent Cooperation Treaty (PCT) application under 35 U.S.C. 371 could be considered to be “substantially the same” art as the PCT application if it has the same disclosure that was previously addressed in the PCT application. Similarly, two non-patent references could be considered to be “substantially the same” if they both

teach the same claim limitation in the same way as the challenged claim.

The Office also seeks to clarify that 35 U.S.C. 325(d) will apply to any proceedings in which the art or arguments were previously addressed, including prosecution, reissue, ex parte reexamination, inter partes reexamination, and AIA post-grant proceedings, and appeals of the same, involving the challenged patent or a related patent or application.

The proposals under consideration provide that if the patent owner meets its burden in showing that the same or substantially the same art or arguments were previously addressed by the Office, then the Board will not institute a trial unless the petitioner establishes material error by the Office. Examples of a material error may include misapprehending or overlooking specific teachings of the relevant prior art where those teachings impact patentability of the challenged claims, including experimental evidence demonstrating an inherent feature of the prior art or rebutting a showing of unexpected results. Another example may include an error of law, such as misconstruing a claim term, where the construction impacts the patentability of the challenged claims. It will not be considered material error if reasonable minds can disagree regarding the purported treatment of the art or arguments.

Parallel Petitions

With regard to parallel petitions filed against the same patent by the same petitioner or by a petitioner who has a substantial relationship with another petitioner challenging the same patent, the changes under consideration would provide that, when determining whether to institute an IPR or PGR, the Board will not institute parallel petitions unless the petitioner has made a showing of good cause as to why parallel petitions are necessary.

Based on the USPTO’s experience with administering the AIA, the Office finds it unlikely that circumstances will arise in which three or more petitions filed by a petitioner with respect to a particular patent will be appropriate. For example, the Office observed that for FY 2021 1,087 out of 1,136 patents challenged (96%) were subject to only one or two petitions, and that 49 out of 1,136 patents challenged (4%) were subject to three or more petitions. See also Analysis of multiple petitions in AIA Proceedings (December 2020 update), www.uspto.gov/sites/default/files/documents/multiple_petition_mta_study.pdf (noting that in FY 2020, 15% of AIA challenges (145 out of 938)

were parallel petitions, and only 30% of those (43) were successful). Further, two or more petitions filed against the same patent at or about the same time may place a substantial and unnecessary burden on the patent owner and could raise fairness, timing, and efficiency concerns. See 35 U.S.C. 316(b), 326(b).

Nevertheless, the Office recognizes that there may be circumstances in which more than one petition may be necessary, including, for example, when there is a dispute about a priority date or two different claim constructions, requiring arguments under multiple prior art references or mutually exclusive unpatentability theories. See Consolidated Trial Practice Guide, 59 (Nov. 2019). In such circumstances, one potential outcome of separating the alternative theories into different petitions, which would benefit patentees as well as petitioners, is that it would allow the Board to deny petitions with non-meritorious theories, such that the instituted AIA trial and related appeal to the Federal Circuit and the Supreme Court, if any, will be focused only on the meritorious theories, thereby eliminating the cost and burden of an AIA trial and appeal on rejected theories. If all of the theories were presented in only one petition, the Board would be required to either institute on all grounds raised in the petition or deny the petition in its entirety. *SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348, 1359–60 (2018); *PGS Geophysical AS v. Iancu*, 891 F.3d 1354, 1359–62 (Fed. Cir. 2018); *Adidas AG v. Nike, Inc.*, 894 F.3d 1256, 1258 (Fed. Cir. 2018).

In responding to the RFC, many stakeholders supported rulemaking to provide additional clarity and predictability that would set forth specific circumstances in which the Director would consider institution of parallel petitions, including, for example, those considerations set forth in the 2019 Consolidated Trial Practice Guide, alternative claim constructions, a large number of claims asserted in related litigation, the complexity of technology, numerous limitations in claims, a large number of different claimed embodiments, and a large number of grounds per challenged claim(s). Some stakeholders recommended that, given the Office’s restrictive word-count limits, additional parallel petitions are needed, and suggested requiring the petitioner to separately justify any second or subsequent parallel petition.

Additionally, some stakeholders encouraged the Office to distinguish parallel-petition situations from serial-petition situations to promote consistent

treatment. Some stakeholders recommended defining parallel petitions as two or more petitions filed before a preliminary response is filed regarding the earlier petition on the same patent.

Further, some stakeholders advocated that, with respect to the restrictive word-count limit, the Office should allow the petitioner to pay additional fees for a higher word-count limit or create a good cause exception to the word-count limit. Some stakeholders also suggested excluding sections of the petition and the preliminary response that address discretionary denial issues from the word-count limit.

The USPTO is considering changes to provide that, instead of filing multiple petitions, a petitioner may pay additional fees for a higher word-count limit. In particular, the Office could allow, for additional fees (e.g., an additional 50% or 100%), higher word-count limits (e.g., an additional 50% or 100%) for the petition. If a petitioner pays the fees for filing a petition with a higher word-count limit (e.g., an additional 50%), the patent owner preliminary response, patent owner response, reply to patent owner response, and sur-reply may be filed with proportionally higher word-count limits (e.g., an additional 50%) at no additional charge to either party. Under this change, a petitioner may file effectively two petitions as one long petition equal in length to two current petitions. Filing more than one petition with a higher word-count limit (i.e., two or more long parallel petitions) challenging the same patent by the same petitioner, however, would not be permitted.

The Office also is considering an additional option to provide that, when determining whether to institute an IPR or PGR, the Board will not institute parallel petitions unless the petitioner has made a showing of good cause as to why parallel petitions are necessary. To aid the Board in determining whether more than one petition (i.e., a parallel petition) is necessary (e.g., whether a showing of good cause exists), a petitioner that files two or more petitions challenging the same patent would, in a separate five-page paper filed with the petitions, identify: (1) a ranking of the petitions in the order in which it wishes the Board to consider the merits, if the Board uses its discretion to institute any of the petitions; and (2) a succinct explanation of the differences between the petitions, why the issues addressed by the differences in the petitions are material, and why the Board should exercise its discretion to institute additional

petitions if it identifies one petition that satisfies the petitioner's burden under 35 U.S.C. 314(a) or 324(a). The patent owner may file a response to the ranking in a separate five-page paper filed with each preliminary response.

The Office also is considering changes that would allow the Board, when evaluating the petitioner's good cause showing as to why more than one petition is necessary, to consider the following factors: (1) whether the patent owner has asserted a large number of claims in the parallel litigation; (2) whether the petitioner is challenging a large number of claims; (3) whether there is a dispute about a priority date requiring arguments under multiple prior art references; (4) whether there are alternative claim constructions that require different prior art references or mutually exclusive grounds; (5) whether the petitioner lacks sufficient information at the time of filing the petition, e.g., the patent owner has not construed the claims or provided specific information as to the allegedly infringed claims; (6) whether there are a large number of claimed embodiments challenged, e.g., composition claims, method of making claims, and method of use claims; (7) the complexity of the technology in the case; and (8) the strength of the merits of the petition.

Also under consideration are changes to provide that "parallel petitions" means two or more petitions that: (1) challenge the same patent by the petitioner or by a petitioner who has a substantial relationship with another petitioner challenging the same patent; and (2) are filed on or before (a) the filing date of a preliminary response to the first of two or more petitions, or (b) the due date set forth in 42.107(b) for filing a preliminary response to the first petition, if no preliminary response to the first petition is filed.

The Office requests feedback as to whether one petition for challenging a patent would be sufficient in most situations, including those suggested by the stakeholders in response to the RFC, if the petitioner is allowed to purchase higher word-count limits and also allowed to submit a separate paper to address discretionary denial issues, as discussed below, preserving word count for the merits. The Office also seeks feedback on whether the same requirements should or should not apply to both IPRs and PGRs. Additionally, the Office requests input on any modifications or alternative definitions for "parallel petitions" that would provide further clarity.

Parallel Litigation

In the case of a parallel district court action in which a trial adjudicating the patentability of the challenged claims has not already concluded at the time of an IPR institution decision, the USPTO is proposing rules to install *Apple v. Fintiv* and related guidance, with additional proposed reforms.

The AIA contains several provisions that function to minimize overlap between district court litigation and AIA proceedings in the Office. For example, the AIA provides that a petitioner may not file a civil action in district court challenging the validity of a patent claim prior to filing a petition asking the Office to institute an IPR or PGR of the same patent. See 35 U.S.C. 315(a)(1), 325(a)(1). Similarly, an IPR may not be instituted on a petition filed more than one year after the date on which the petitioner, a real party in interest, or a privy of the petitioner is served with a complaint alleging infringement of the patent, except under limited circumstances, which the Office is separately reconsidering, where the petition is accompanied by a request for joinder. 35 U.S.C. 315(b). Further, if a petitioner or real party in interest files a civil action challenging the validity of a patent claim after an IPR or PGR is instituted, the civil action will be stayed under most circumstances. See 35 U.S.C. 315(a)(2), 325(a)(2). In situations in which the petitioner is not barred by statute from pursuing an AIA proceeding in parallel with district court litigation, district courts have discretion to stay the parallel litigation in order to minimize duplicative efforts.

In contrast, the statutory deadlines governing the issuance of decisions on institution and final written decisions oftentimes make stays of AIA proceedings impractical. See 35 U.S.C. 314(b), 316(a)(11), 324(c), 326(a)(11). The Office, however, retains discretion under 35 U.S.C. 314(a) and 324(a) to deny institution of an IPR or PGR in circumstances in which parallel proceedings would result in significant inefficiency or in which there is gamesmanship or harassment. The Office has exercised that discretion to reduce overlap with parallel proceedings, particularly when trial in a parallel court proceeding would precede a final written decision from the Office. See, e.g., *Fintiv*, 2020 WL 2126495, at *2–7 (summarizing the factors the Office has considered when a patent owner argues for discretionary denial due to an earlier court trial date).

As noted, the Office received 822 comments in response to the RFC on the *Fintiv* factors and other aspects of AIA

proceedings. Comments from stakeholders in response to the RFC generally supported rulemaking with respect to discretionary denial, although the comments differed as to the specifics. In general, proponents of the *Fintiv* approach argued that petitioners should be required to choose a venue to avoid the expense for patent owners, especially independent inventors and small businesses, of participating in two proceedings addressing the same issues at the same time. They also argued that allowing multiple challenges destabilizes the patent system and violates the intent of Congress for AIA proceedings to be an alternative to district court litigation. These proponents favored litigation in district courts because district courts use a higher burden of proof, including the presumption of patent validity, and provide access to a jury.

In contrast, those opposed to the *Fintiv* approach argued that *Fintiv* incentivizes district court forum shopping by encouraging the filing of lawsuits in venues in which judges are quicker to schedule trials, even if those trial dates may not hold. They also argued that *Fintiv* is contrary to the explicit statutory one-year time frame permitted for a petitioner to file a petition after being served with a complaint charging infringement. *Fintiv* opponents further argued that the Office should not exercise discretion to deny institution of a timely filed, meritorious petition. They favored resolving patentability disputes before the PTAB, noting that it is a less expensive, more expert forum with legally and technically trained judges, and has a lower burden of proof.

On June 21, 2022, as the Office considered rulemaking on discretionary denials, the Director issued the Guidance Memorandum, which contains “several clarifications . . . to the PTAB’s current application of *Fintiv* to discretionary institution where there is parallel litigation.” As outlined in the Guidance Memorandum, the Board’s current practice is not to deny institution of an IPR under *Fintiv*: (1) when a petition presents compelling merits of unpatentability; (2) when a request for denial under *Fintiv* is based on a parallel International Trade Commission (ITC) proceeding; or (3) when a petitioner stipulates not to pursue in a parallel district court proceeding the same grounds as those in the petition or any grounds that could have reasonably been raised in the petition. Additionally, when the Board applies *Fintiv* factor 2, concerning the proximity of the district court trial date, the Board currently weighs this factor

against exercising discretion to deny institution if the projected district court trial date, based on median time-to-trial data, is around the same time as or after the projected statutory deadline for the Board’s final written decision.

Even if the Board does not deny institution under *Fintiv*, it retains discretion to deny institution for other reasons under 35 U.S.C. 314(a), 324(a), and 325(d). For example, the Guidance Memorandum makes clear that the Board may deny institution if other pertinent circumstances are present, such as abuse of process by a petitioner. The Office contemplates that the Board would retain the authority to deny institution in such circumstances.

Parallel Proceedings—Denial Unavailable

(1) Parallel PGR and District Court Proceedings

Congress expressed a premium on the value of PGRs, given the ability of those proceedings to explore more patentability issues early in patent life. More specifically, PGRs, unlike IPRs, may only be filed within nine months from the grant of the patent. 35 U.S.C. 321(c). This short-term window for filing a PGR reflects Congress’s desire to create “a new, early-stage process for challenging patent validity.” H.R. Rep. No. 112–98, part 1, at 48. By setting forth a strict time limit with respect to the filing of PGRs, Congress sought to ensure review of patents “early in their life, before they disrupt an entire industry or result in expensive litigation.” 157 Cong. Rec. S1326 (daily ed. Mar. 7, 2011) (statement of Sen. Sessions). Congress also sought to incentivize the filing of PGRs by allowing petitioners to raise any ground related to invalidity under section 282(b) of the Patent Act, in contrast to IPRs, in which petitioners are permitted only to raise challenges on a ground that could be raised under section 102 or 103 and only on the basis of prior art consisting of patents or printed publications. 35 U.S.C. 311(b), 321(b). As a result, the statutory estoppel ensuing from a PGR proceeding is broader than the statutory estoppel from an IPR proceeding, lessening the risks of conflicting decisions arising between the PTAB and district courts. *See* 35 U.S.C. 315(e)(2), 325(e)(2). Additionally, the threshold standard for institution of a PGR is higher than that for an IPR, as it requires a showing that at least one claim is more likely than not unpatentable rather than merely a reasonable likelihood of prevailing. *Compare* 35 U.S.C. 324(a) with 35 U.S.C. 314(a).

Given the clear differences in their statutory requirements, which serve to reduce the likelihood of potentially conflicting outcomes in parallel PGR and district court litigation, the Office is exploring whether different criteria should apply to discretionary denial of PGRs versus IPRs. One possibility is a rule providing that the Board will not invoke its discretion to deny institution of a PGR based on parallel district court litigation. The Office welcomes thoughts on whether PGRs should be treated differently than IPRs and, if so, how.

(2) IPR or PGR Proceedings and Parallel ITC Investigations

Consistent with current USPTO practice, the Office is contemplating a rule providing that the Board will not invoke its discretion under 35 U.S.C. 314(a) or 324(a) to deny institution of an IPR or PGR based on the existence or status of parallel ITC proceedings.

The Office recognizes that important differences distinguish ITC investigations from patent invalidity trials in federal district courts. Unlike district courts, the ITC lacks authority to invalidate a patent, and its invalidity rulings are not binding on either the Office or a district court. *See Tandon Corp. v. U.S.I.T.C.*, 831 F.2d 1017, 1019 (Fed. Cir. 1987). Therefore, an ITC determination cannot conclusively resolve an assertion of patent invalidity, which instead requires either district court litigation or a PTAB proceeding to obtain claim cancellation. Thus, denying institution because of a parallel ITC investigation will not necessarily minimize potential conflicts between PTAB proceedings and district court litigation. For this reason, it is the current practice of the USPTO not to deny institution of an IPR or PGR petition based on parallel proceedings in the ITC.

Parallel Proceedings—Denial Available

If neither situation outlined above, if adopted, precludes discretionary denial, the Board would then proceed to consider discretionary denial of an IPR in view of a parallel district court action. The Office is considering two alternatives for applying the Director’s discretion here: one in which discretionary denial determinations are governed solely by a clear, predictable rule, and another governed by that clear, predictable rule working, where appropriate, in conjunction with a streamlined version of the current *Fintiv* factors. In either option, a set of safe harbor exceptions to discretionary denial applies.

(1) Parallel IPR and District Court Proceedings—Clear, Predictable Rules

The Office notes that concerns regarding overlapping issues and duplicative efforts are greatly mitigated when a district court trial will not take place until after the Board issues a final written decision. Absent unusual circumstances, the Board is required to issue a final written decision not more than one year after an IPR is instituted. See 35 U.S.C. 316(a)(11). Thus, when a district court trial takes place more than one year after the deadline to institute an IPR, the estoppel of 35 U.S.C. 315(e)(2) will minimize or eliminate any potential overlap. See *id.* (providing that the issuance of a final written decision bars the petitioner from raising in district court “any ground that the petitioner raised or reasonably could have raised during that inter partes review”). District courts, which are not bound by statutory deadlines, are also able to adjust case schedules or implement stays, and can thereby avoid expending significant pre-trial efforts on issues that will be resolved in an IPR.

The Office is considering that, unless a safe harbor exception in the following section is met, the Board would apply a clear, predictable rule and deny institution of an IPR in view of pending parallel district court litigation involving at least one of the challenged claims if the Board determines a trial in the district court action is likely to occur before the projected statutory deadline for a final written decision. When analyzing when a district court trial is likely to occur, the Board may consider evidence regarding the most recent statistics on median time-to-trial for civil actions in the district court in which the parallel litigation resides as well as additional supporting factors, such as the number of cases before the judge in the parallel litigation and the speed and availability of other case dispositions.

As an alternative to determining if a trial in the district court action is likely to occur before the projected statutory deadline for a final written decision, and to ensure more clarity and certainty, the Office is considering whether to adopt a rule providing that the Board will not invoke its discretion to deny an IPR petition based on a parallel district court proceeding if the IPR petition is filed within 6 months after the date on which the petitioner, a real party in interest, or a privy thereof is served with a complaint alleging infringement of the patent, provided that the petitioner, real party in interest, or privy did not first file a civil action seeking declaratory judgment of noninfringement of any

claim of the patent before the date on which such complaint alleging infringement was filed. The Office recognizes that 35 U.S.C. 315(a)(1) bars institution of an IPR only if, before the date on which the petition for such review is filed, the petitioner or a real party in interest filed a civil action challenging the validity of a claim of the patent, and that 35 U.S.C. 315(b) permits a petition to be filed within one year of service of such a complaint. An early-filing exception would not, however, impose any earlier deadlines. It would instead merely offer an incentive for a petitioner to proceed promptly with any IPR petition. In the Office’s experience, such an incentive is desirable because prompt filing of a petition minimizes the potential for overlapping issues and duplicative efforts that can result from parallel proceedings. For example, prompt filing of an IPR petition could permit a district court to consider the possibility of a stay before it has invested significant resources into a lawsuit or could allow the court to tailor its case management deadlines so that it can take advantage of Board decisions on any overlapping issues.

(2) Exceptions—Safe Harbors Under Consideration

The USPTO recognizes that there are certain situations in which it may be inappropriate for the Board to deny institution in view of parallel district court litigation and is considering adopting changes to the rules that would govern such situations.

First, the Office is considering a rule providing that the Board will not deny institution under 35 U.S.C. 314(a) in view of parallel litigation when the petitioner files a stipulation agreeing not to pursue potentially overlapping grounds in district court. The Office is considering whether the petitioner must show that a stipulation has been filed in the district court action as well, and whether, if the petitioner is not a party to the district court litigation but a district court litigant is nonetheless a real party in interest or in privity with the petitioner, a stipulation filed by the party to the district court action would suffice under this exception.

The Office has recognized that when a petitioner stipulates not to pursue in a parallel district court proceeding grounds that were raised in the petition, the stipulation mitigates concerns related to overlapping issues and duplicative efforts. See *Sand Revolution, II, LLC v. Cont’l Intermodal Grp.—Trucking LLC*, IPR2019–01393, 2020 WL 3273334, at *5 (PTAB June 16, 2020) (applying *Fintiv* factors and

noting that the petitioner’s stipulation to forgo pursuing the “same” invalidity grounds in district court mitigated concerns regarding overlap) (*Sand Revolution* stipulation). The Office has also recognized that a broader stipulation, which also encompasses any ground that could have reasonably been raised in the petition, would weigh even more strongly against discretionary denial. See *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020–01019, 2020 WL 7049373, at *7 (PTAB Dec. 1, 2020) (applying *Fintiv* factors and determining that the petitioner’s stipulation to forgo pursuing in district court litigation “any ground raised or that could have been reasonably raised in an IPR” weighed “strongly” against exercising discretion to deny an IPR) (*Sotera* stipulation). In accordance with the Guidance Memorandum, the Board’s current practice is not to deny institution based on a parallel proceeding when the petitioner agrees to a broad *Sotera* stipulation that would prevent it from pursuing in a parallel district court proceeding “the same grounds as in the petition or any grounds that could have reasonably been raised in the petition.”

A significant advantage of a *Sotera* stipulation is that it effectively minimizes concerns related to the overlapping issues and duplicative efforts that may result from parallel district court litigation. A *Sand Revolution* stipulation, in contrast, does not necessarily prevent a petitioner from using a reference that was not raised, but reasonably could have been raised in an IPR, as part of an invalidity argument in district court. The estoppel provision of 35 U.S.C. 315(e)(2) will bar the petitioner from pursuing in district court any ground it raised, or reasonably could have raised, in the IPR, but only upon the issuance of a final written decision. Because this estoppel provision does not apply until the end of an AIA trial, it does not eliminate the concerns about overlapping issues and duplicative efforts that could arise from allowing petitioners to avoid discretionary denial of institution by agreeing merely to a narrower *Sand Revolution* stipulation.

However, the USPTO also recognizes that there are several potential disadvantages of adopting a rule that requires *Sotera* stipulations. For example, after an IPR petition has been filed, a patent owner may amend its district court infringement contentions to accuse a petitioner of infringing additional claims. In this situation, a *Sotera* stipulation might unfairly limit the defenses a petitioner could raise in district court against the newly asserted claims. Accordingly, such a rule could

incentivize petitioners to challenge more claims than necessary in an IPR in order to protect themselves in parallel litigation, thereby increasing the Office's workload and the parties' corresponding burden and expense. The USPTO recognizes that a narrower stipulation, such as a *Sand Revolution* stipulation, might avoid these undesirable consequences. The Office further understands that district courts have tools available to manage overlapping issues and minimize duplicative efforts, including the ability to limit certain defenses, to grant stays, and to provide flexible schedules. These tools arguably mitigate the concerns regarding overlapping issues and duplicative efforts that would result from a rule that allowed a petitioner to avoid discretionary denial of institution by filing a narrower stipulation.

Based on the foregoing considerations, the USPTO currently believes that—should it maintain this exception—the most appropriate approach is to maintain the current practice of permitting a petitioner to avoid a discretionary denial only by filing a *Sotera* stipulation. The Office would appreciate public comments regarding whether other, narrower types of stipulations should be sufficient to permit a petitioner to avoid discretionary denial of institution, such as a *Sotera* stipulation that is limited to the specific patent claims challenged in the petition, or a *Sand Revolution* stipulation. The Office would also appreciate comments on whether the *Sotera* stipulation can and should be limited to the claims asserted at the time the stipulation is filed.

The Office is additionally considering removing this exception and instead making a *Sotera* stipulation a necessary but not sufficient basis for institution. In other words, to survive a challenge under *Fintiv*, the Petitioner would necessarily need to file a *Sotera* stipulation. The Petitioner would still need to meet the other criteria for institution in view of a parallel litigation as expressed in this section.

As an alternative to all of the options discussed above, in the interest of creating a bright line test and to reduce uncertainty, the Office seeks feedback on whether *Fintiv* should be replaced entirely by a *Sotera* stipulation requirement where, when a parallel litigation is ongoing, the Office will not exercise discretion to deny institution if a *Sotera* stipulation is filed but would otherwise discretionarily deny institution without consideration of other circumstances or factors discussed above.

Second, the USPTO recognizes that stays of district court proceedings can minimize concerns related to parallel litigation. The Office, therefore, is considering a rule providing that the Board will not invoke its discretion to deny institution of an IPR based on a parallel district court proceeding if the parallel proceeding has been stayed and is reasonably expected to remain stayed at least until the deadline for the Board's decision regarding whether to institute an IPR. Such a rule would be consistent with Board precedent holding that a stay of parallel district court litigation “allays concerns about inefficiency and duplication of efforts” and “weighs strongly against exercising discretion to deny institution.” *Snap, Inc. v. SRK Tech. LLC*, IPR2020–00820, Paper 15, 2020 WL 6164354, at *4 (PTAB Oct. 21, 2020) (precedential as to section II.A). Where a district court has stayed proceedings and the Board institutes an IPR, the district court can avoid overlapping issues by continuing the stay until the Board issues a final written decision, at which time the petitioner will be barred from asserting in district court “any ground that the petitioner raised or reasonably could have raised during that inter partes review.” 35 U.S.C. 315(e)(2). Alternatively, the district court can adopt a schedule that allows it to avoid unnecessary rulings on potentially overlapping issues and to take advantage of Board rulings while still permitting litigation to move forward.

The USPTO is considering other exceptions as well. One potential exception in relation to parallel IPR or PGR and district court proceedings relates to strength of merits. In particular, the Office is contemplating that if the circumstances favor a discretionary denial of institution, the Board will analyze the merits of the petition, and will not discretionarily deny institution if the petition presents compelling merits. To further aid the USPTO's consideration of this proposal, the Office requests comments on whether a finding by the Board that the petition meets the compelling merits standard at institution increases or decreases the chance that a parallel district court action will be stayed.

(3) Parallel IPR and District Court Proceedings—Additional Factor-Based Test

The clear, predictable rule proposed above to govern discretionary denial decisions based on parallel district court proceedings is intended to provide clarity and certainty for the parties. Recognizing that the discretionary issues presented by parallel district

court litigation can be highly fact-variant, the Office is considering whether to additionally provide for a streamlined version of one or more of the other current *Fintiv* factors. The factor-based test would be available to the parties and the Board to consider, as appropriate and necessary, to avoid effecting an unduly harsh outcome under the clear, predictable rule. The Office expects that the clear, predictable rule will control the vast majority of discretionary issues in this space and make it unnecessary to engage any factor-based test.

For example, the Office is contemplating a factor-based test that would omit *Fintiv* factor 1 (the likelihood of a stay) because past experience has shown it to be difficult to predict a district court's future actions. The Office is also contemplating omitting *Fintiv* factor 5 (whether the petitioner and the defendant in the parallel proceeding are the same party) in favor of considering real parties in interest and privies, or alternatively parties that are substantially related.

The Office is considering three non-exclusive factors that, in addition to a clear, predictable rule, would be available, where appropriate, to guide the Board's discretion in situations in which the petitioner, its real party in interest, or a privy thereof is a party to ongoing district court litigation. The factors under consideration are:

- (1) Past and future expected investment in the parallel proceeding by the district court and the parties;
- (2) The degree of overlap between the issues in the petition and the parallel district court proceeding; and
- (3) Any other circumstances that the parties contend are relevant to the Board's exercise of discretion.

The first two factors are similar to *Fintiv* factors 3 and 4, respectively. The third factor above is similar to *Fintiv* factor 6. The exceptions/safe harbors from discretionary denial discussed above would apply equally to any discretionary decision rendered by the Board based on a factor-based test.

The Office welcomes thoughts on (1)–(3) above including the Office's current application of (3). The Office also welcomes comments on whether (1) or (2) are necessary.

Under the current guidelines, the PTAB weighs under the *Fintiv* analysis any additional circumstances that inform whether institution would advance or negatively impact the integrity of the patent system, including whether there is an abuse of the process such that the AIA proceeding is being used in a way that does not comport

with the purpose and legitimate goals of the AIA. *See OpenSky Indus., LLC v. VLSI Tech. LLC*, IPR2021–01064, Paper 102 at 44 (PTAB Oct. 4, 2022) (Director decision, precedential). A party may raise under *Fintiv* as an additional circumstance for denying a petition sought to be joined the fact that the party seeking to join would have been time-barred from filing the petition it seeks to join. Currently, any decision by the PTAB granting or denying institution based on this paragraph may be challenged on Director review.

The Office is also considering adopting a rule with regard to petitions accompanied by a motion for joinder. To help clarify the application of discretionary denial in view of a co-pending district court litigation, the joinder petition would be evaluated with respect to the timing of any underlying litigation of the earlier-filed petition. This means that when a party seeks to join an AIA proceeding, the PTAB would conduct the parallel proceeding analysis with respect to litigation involving the petitioner for the first-filed petition to which joinder is sought, in addition to exercising the Director's discretion on joinder consistent with operable rules, precedent, and practices.

Stipulation on No Multiple Challenges

To avoid patent owner harassment, the Office is considering, as a condition to not discretionarily denying institution under 35 U.S.C. 314(a), requiring petitioners to file a stipulation that neither they nor their privy or real parties have filed prior post-grant proceedings (PGRs, IPRs, CBMs or ex parte reexaminations requested by third parties, not by patent owner) as to any of the challenged claims; and that if their post-grant proceeding is instituted, neither they nor their privy or real parties in interest, will challenge any of the challenged claims in a subsequent post-grant proceeding (including PGRs, IPRs and ex parte reexaminations requested by third parties, not by patent owner). The Office is considering an exception to this rule where a petitioner can establish exceptional circumstances. Exceptional circumstances may include, for example, situations in which a patentee broadens the scope of the claims through a proposed claim construction.

Separate Briefing for Discretionary Denial

Many commenters who responded to the RFC suggested allowing the parties to brief discretionary denial considerations under 35 U.S.C. 314(a), 324(a), and 325(d) in separate papers

(i.e., separate from the petition or the patent owner preliminary response), to avoid encroaching on the parties' word-count limits for briefing on the merits. The Office has found the practice of allowing parties to file separate papers addressing the ranking of petitions helpful in evaluating parallel petitions while preserving the parties' word count to focus on the merits of the challenge. The Office believes a similar procedure to allow parties to address all relevant factors for discretionary denial in separate briefing would also be helpful.

The USPTO is considering amending the rules to provide a procedure for separate briefing on discretionary denial, in which the patent owner would file, prior to the deadline for a preliminary response, a separate request for discretionary denial to address any relevant factors regarding discretionary denial. This filing would trigger the opportunity for the petitioner to file an opposition and for the patent owner to file a reply. The page limits for such briefing would be 10 pages for the patent owner request, 10 pages for a petitioner opposition to the request, and 5 pages for a patent owner reply.

The Office is further considering amending the rules to provide that the Board may also, in the interest of justice, raise discretionary denial *sua sponte*, in which case the Board will provide the parties with the opportunity for briefing.

The USPTO also requests feedback on whether the Office should require patentees to provide (e.g., in a request for discretionary denial or as part of their mandatory disclosures, 37 CFR 42.8) additional information as to patent ownership as a precondition for the Board considering discretionary denial. For example, the Office requests feedback on whether, as a precondition to discretionary denial, patent owners should be required to disclose additional information relating to entities having a substantial relationship with the patent owner (e.g., anyone with an ownership interest in the patent owner; any government funding or third-party litigation funding support, including funding for some or all of the patent owner's attorney fees or expenses before the PTAB or district court; and any stake any party has in the outcome of the AIA proceeding or any parallel proceedings on the challenged claims).

Settlement Agreements

For consistency and predictability, the USPTO is considering changes to the rules to clarify that parties must file with the Office true copies of all settlement agreements, including pre-institution settlement agreements (or

understandings between the parties, including any collateral agreements referred to in such agreements or understandings), similar to post-institution settlement agreements. In addition, although the USPTO may grant a motion to terminate an AIA proceeding prior to or after institution based on a binding term sheet, the Office proposes to clarify that parties are required to file a true copy of any subsequent settlement agreements between the parties in connection with, or in contemplation of, the termination.

These considered changes align with the policy set forth in the Executive Order on Promoting Competition in the American Economy (E.O. 14036), which encourages Government agencies to cooperate on policing unfair, anticompetitive practices. Having a depository of all settlement agreements in connection with contested cases, including AIA proceedings, in the USPTO would assist the Federal Trade Commission (FTC) and the Department of Justice in determining whether antitrust laws were being violated. *See, e.g., Congressional Record, Senate, October 3, 1962, 22041, www.govinfo.gov/content/pkg/GPO-CRECB-1962-pt16/pdf/GPO-CRECB-1962-pt16-5.pdf* (explaining that the filing with the Patent Office of all agreements in connection with interference cases would assist the FTC and the Department of Justice in determining whether the antitrust laws were being violated).

Although 35 U.S.C. 135(e), 317(b), and 327(b) require filing of settlement agreements made in connection with, or in contemplation of, the termination of a proceeding that has been instituted, these statutory provisions do not expressly govern AIA pre-institution settlement. *See Rules of Practice for Trials Before the Patent Trial and Appeal Board and Judicial Review of Patent Trial and Appeal Board Decisions*, 77 FR 48612, 48625 (Aug. 14, 2012) (final rule) (stating that "35 U.S.C. 135(e) and 317, as amended, and 35 U.S.C. 327 will govern settlement of Board trial proceedings but do not expressly govern pre-institution settlement"). The Office is considering changes to clarify that 37 CFR 42.74(b) "provides that settlement agreements must be in writing and filed with the Board prior to termination of the proceeding."

Since the inception of AIA trials, the Board has been generally uniform in requiring the filing of a settlement agreement prior to terminating an AIA proceeding based on a joint motion by the parties, pre- or post-institution. Nevertheless, some petitioners have

recently filed motions to dismiss or withdraw the petition before institution, arguing that they should not be required to file a copy of the parties' settlement agreements, and some panels in those cases have granted the motions and terminated the proceedings without requiring the parties to file their settlement agreements. *See, e.g., Samsung Elecs. Co. v. Telefonaktiebolaget LM Ericsson*, IPR2021-00446, Paper 7 (PTAB Aug. 3, 2021) (Order—Dismissal Prior to Institution of Trial) (over the dissent of one Administrative Patent Judge (APJ)), granting the petitioner's motion to dismiss the petition and terminating the proceeding, without requiring the parties to file their settlement agreements); *Huawei Techs. Co. v. Verizon Patent & Licensing Inc.*, IPR2021-00616, -00617, Paper 9 (PTAB Sept. 9, 2021) (Order—Dismissal Prior to Institution of Trial) (same dispute among a panel of APJs); *AEP Generation Res. Inc. v. Midwest Energy Emissions Corp.*, IPR2020-01294, Paper 11 (PTAB Dec. 14, 2020).

For consistency and predictability, the considered changes would ensure that pre-institution settlement agreements, like post-institution settlement agreements, are filed with the Board. Under the considered changes, notwithstanding that an AIA proceeding is in a preliminary stage before institution, any agreement or understanding between the patent owner and a petitioner, including any collateral agreements referred to in such agreement or understanding, made in connection with, or in contemplation of, the termination of an AIA proceeding, would be required to be in writing, and a true copy of such agreement or understanding would be required to be filed in the Office. In short, all settlement agreements between the parties made in connection with, or in contemplation of, the termination of an AIA proceeding would need to be in writing and filed with the Board. Parties would not be able to circumvent this requirement by filing merely a motion to dismiss or withdraw the petition, as granting such a motion would effectively terminate the proceeding.

In addition, as noted above, although the USPTO may grant a motion to terminate an AIA proceeding prior to or after institution based on a binding term sheet, the Office could require the filing of a true copy of any subsequent settlement agreement between the parties in connection with, or in contemplation of, the termination. Under the current practice, some panels have accepted a binding term sheet as the settlement agreement, while other

panels have required a formal settlement agreement, not just a binding term sheet. For example, in several cases, panels granted a motion to terminate a proceeding based on a binding term sheet notwithstanding that a future settlement agreement was contemplated. *See, e.g., Allergan Inc. v. BTL Healthcare Techs. A.S.*, PGR2021-00022, Paper 17 (PTAB July 6, 2021); *Nalu Med., Inc. v. Nevro Corp.*, IPR2021-01023, Paper 14 (PTAB Nov. 24, 2021). In several other cases in which the parties filed or executed a binding term sheet while contemplating a settlement agreement, the panel held the motion to terminate in abeyance until the parties filed the settlement agreement, or granted a short extension of time, so the parties could avoid the expense of continued preparation of a preliminary response or other papers until the parties filed the settlement agreement. *See, e.g., Textron Inc. v. Nivel Parts & Mfg. Co.*, PGR2017-00035, Paper 15 (PTAB Feb. 2, 2018); *AT&T Corp. v. Kaiji LLC*, IPR2020-00889, Paper 9 (PTAB July 17, 2020).

The Office is considering changes to amend the rules to provide that the parties may file a binding term sheet with their motion to terminate a proceeding. Also, the Board may grant the motion to terminate based on the binding term sheet if the parties certify in their motion that: (1) there are no other agreements or understandings, including any collateral agreements, between the parties with respect to the termination of the proceeding; and (2) they will file a true copy of any subsequent settlement agreement between the parties, including collateral agreements, made in connection with the termination of the proceeding, within one month from the date that the settlement agreement is executed. A failure to timely file the subsequent settlement agreement could result in sanctions. *See* 37 CFR 42.11(a) and 42.12. The Board may maintain jurisdiction over the proceeding and the involved patent to resolve any misconduct issues or vacate its decision granting the motion to terminate.

The Office welcomes any comments on the anticipated benefits and costs to individual parties, and the economy as a whole, that may result from the proposed actions above on discretionary denial.

The Office welcomes any other additional comments or proposals on discretionary denial.

Executive Order 12866 (Regulatory Planning and Review): This rulemaking has been determined to be significant

for purposes of E.O. 12866 (Sept. 30, 1993).

Katherine K. Vidal,
Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office.

[FR Doc. 2023-08239 Filed 4-20-23; 8:45 am]

BILLING CODE 3510-16-P

ENVIRONMENTAL PROTECTION AGENCY

40 CFR Part 52

[EPA-R06-OAR-2022-0307; FRL-10892-01-R6]

Air Plan Approval; Texas; Updates to Public Notice and Procedural Rules and Removal of Obsolete Provisions

AGENCY: Environmental Protection Agency (EPA).

ACTION: Proposed rule.

SUMMARY: Pursuant to the Federal Clean Air Act (CAA or the Act), the Environmental Protection Agency (EPA) is proposing to approve portions of three revisions to the Texas State Implementation Plan (SIP) submitted by the Texas Commission on Environmental Quality (TCEQ) on July 9, 2021, and January 21, 2022. The first revision, adopted on April 22, 2020, submitted on January 21, 2022, updates internal cross-references and removes or replaces obsolete provisions identified during a routine review of the Texas permitting regulations. The second revision, adopted on June 9, 2021, submitted July 9, 2021, repeals obsolete permitting provisions, and makes necessary corresponding edits to other permitting provisions. The third revision, adopted on August 25, 2021, submitted January 21, 2022, enhances the public notice requirements of the air permitting program.

DATES: Written comments must be received on or before May 22, 2023.

ADDRESSES: Submit your comments, identified by Docket No. EPA-R06-OAR-2022-0307, at <https://www.regulations.gov> or via email to wiley.adina@epa.gov. Follow the online instructions for submitting comments. Once submitted, comments cannot be edited or removed from [Regulations.gov](https://www.regulations.gov). The EPA may publish any comment received to its public docket. Do not submit electronically any information you consider to be Confidential Business Information (CBI) or other information whose disclosure is restricted by statute. Multimedia submissions (audio, video, etc.) must be accompanied by a written comment.



designated representatives. Normally such actions are categorically excluded from further review under paragraph L61 of Appendix A, Table 1 of DHS Instruction Manual 023-01-001-01, Rev. 1. A preliminary Record of Environmental Consideration supporting this determination is available in the docket. For instructions on locating the docket, see the **ADDRESSES** section of this preamble. We seek any comments or information that may lead to the discovery of a significant environmental impact from this proposed rule.

G. Protest Activities

The Coast Guard respects the First Amendment rights of protesters. Protesters are asked to call or email the person listed in the **FOR FURTHER INFORMATION CONTACT** section to coordinate protest activities so that your message can be received without jeopardizing the safety or security of people, places, or vessels.

V. Public Participation and Request for Comments

We view public participation as essential to effective rulemaking and will consider all comments and material received during the comment period. Your comment can help shape the outcome of this rulemaking. If you submit a comment, please include the docket number for this rulemaking, indicate the specific section of this document to which each comment applies, and provide a reason for each suggestion or recommendation.

Submitting comments. We encourage you to submit comments through the Federal Decision-Making Portal at <https://www.regulations.gov>. To do so, go to <https://www.regulations.gov>, type USCG-2024-0169 in the search box and click "Search." Next, look for this document in the Search Results column, and click on it. Then click on the Comment option. If you cannot submit your material by using <https://www.regulations.gov>, call or email the person in the **FOR FURTHER INFORMATION CONTACT** section of this proposed rule for alternate instructions.

Viewing material in docket. To view documents mentioned in this proposed rule as being available in the docket, find the docket as described in the previous paragraph, and then select "Supporting & Related Material" in the Document Type column. Public comments will also be placed in our online docket and can be viewed by following instructions on the <https://www.regulations.gov> Frequently Asked Questions web page. Also, if you click on the Dockets tab and then the

proposed rule, you should see a "Subscribe" option for email alerts. The option will notify you when comments are posted, or a final rule is published.

We review all comments received, but we will only post comments that address the topic of the proposed rule. We may choose not to post off-topic, inappropriate, or duplicate comments that we receive.

Personal information. We accept anonymous comments. Comments we post to <https://www.regulations.gov> will include any personal information you have provided. For more about privacy and submissions to the docket in response to this document, see DHS's eRulemaking System of Records notice (85 FR 14226, March 11, 2020).

List of Subjects in 33 CFR Part 100

Harbors, Marine safety, Navigation (water), Reporting and recordkeeping requirements, Security measures, Waterways.

For the reasons discussed in the preamble, the Coast Guard is proposing to amend 33 CFR part 100 as follows:

PART 100—SAFETY OF LIFE ON NAVIGABLE WATERS

- 1. The authority citation for part 100 continues to read as follows:

Authority: 46 U.S.C. 70041; 33 CFR 1.05–1.

- 2. Add § 100.T01–0169 to read as follows:

§ 100.T01–0169 Sail Grand Prix 2024, Upper Bay New York Harbor, New York City, NY.

(a) *Regulated area.* The regulations in this section apply to the following area: All waters of the Upper Bay of New York Harbor, from surface to bottom, encompassed by a line connecting the following points beginning at 40°42'10.6" N, 74°01'48.5" W; thence to 40°41'50.0" N, 74°01'08.7" W; thence to 40°41'35.6" N 74°01'08.8" W; thence along the shore to 40°41'02.4" N 74°01'29.3" W; thence to 40°40'46.9" N 74°01'49.3" W; thence to 40°40'49.0" N 74°02'25.5" W; thence to 40°41'13.3" N 74°02'26.2" W; thence to 40°41'31.0" N 74°02'18.7" W; thence to 40°41'54.6" N 74°02'01.3" W; thence to 40°42'03.9" N 74°01'56.8" W and thence back to the point of origin. These coordinates are based on North American Datum 83 (NAD 83).

(b) *Definitions.* As used in this section—

Designated representative means a Coast Guard Patrol Commander, including a Coast Guard coxswain, petty officer, or other officer operating a Coast Guard vessel and a Federal, State, and

local officer designated by or assisting the Captain of the Port New York (COTP) in the enforcement of the regulations in this section.

Participant means all persons and vessels registered with the event sponsor as a participant in the race.

(c) *Regulations.* (1) All non-participants are prohibited from entering, transiting through, anchoring in, or remaining within the regulated area described in paragraph (a) of this section unless authorized by the Captain of the Port New York (COTP) or their designated representative.

(2) To seek permission to enter, contact the COTP or the COTP's representative by VHF–FM Channel 16. Those in the regulated area must comply with all lawful orders or directions given to them by the COTP or the designated representative.

(3) The COTP will provide notice of the regulated area through advanced notice via broadcast notice to mariners and by on-scene designated representatives.

(d) *Enforcement periods.* This section will be enforced from 1 p.m. to 4 p.m. on June 21, 2024, and from 3:30 p.m. to 6:30 p.m. on June 22, 2024, through June 23, 2024.

Zeita Merchant,

Captain, U.S. Coast Guard, Captain of the Port Sector New York.

[FR Doc. 2024–08433 Filed 4–18–24; 8:45 am]

BILLING CODE 9110–04–P

DEPARTMENT OF COMMERCE

Patent and Trademark Office

37 CFR Part 42

[Docket No. PTO–P–2023–0048]

RIN 0651–AD72

Patent Trial and Appeal Board Rules of Practice for Briefing Discretionary Denial Issues, and Rules for 325(d) Considerations, Instituting Parallel and Serial Petitions, and Termination Due to Settlement Agreement

AGENCY: United States Patent and Trademark Office, Department of Commerce.

ACTION: Notice of proposed rulemaking.

SUMMARY: The United States Patent and Trademark Office (USPTO or Office) proposes modifications to the rules of practice for inter partes review (IPR) and post-grant review (PGR) proceedings before the Patent Trial and Appeal Board (PTAB or Board) that the Director and, by delegation, the PTAB will use

in exercising discretion to institute IPRs and PGRs. The Office proposes these provisions in light of stakeholder feedback received in response to an October 2020 Request for Comments (RFC) and an April 2023 Advance Notice of Proposed Rulemaking (ANPRM). The proposals enhance and build on existing precedent and guidance regarding the exercise of the Director's discretion pursuant to the America Invents Act (AIA) to determine whether to institute an IPR or PGR proceeding with regard to serial petitions, parallel petitions, and petitions implicating the same or substantially the same art or arguments previously presented to the Office. The proposed rules also provide a separate briefing process for discretionary institution arguments and align the procedures for termination of proceedings pre- and post-institution.

DATES: Comments must be received by June 18, 2024 to ensure consideration.

ADDRESSES: For reasons of Government efficiency, comments must be submitted through the Federal eRulemaking Portal at <https://www.regulations.gov>. To submit comments via the portal, one should enter docket number PTO-P-2023-0048 on the homepage and click "search." The site will provide search results listing all documents associated with this docket. Commenters can find a reference to this notice and click on the "Comment" icon, complete the required fields, and enter or attach their comments. Attachments to electronic comments will be accepted in Adobe® portable document format (PDF) or Microsoft Word® format. Because comments will be made available for public inspection, information that the submitter does not desire to make public, such as an address or phone number, should not be included in the comments.

Visit the Federal eRulemaking Portal for additional instructions on providing comments via the portal. If electronic submission of, or access to, comments is not feasible due to a lack of access to a computer and/or the internet, please contact the USPTO using the contact information below for special instructions.

FOR FURTHER INFORMATION CONTACT:

Michael P. Tierney, Vice Chief Administrative Patent Judge; Amber L. Hagy, Lead Administrative Patent Judge; or

Jamie T. Wisz, Lead Administrative Patent Judge, at 571-272-9797.

SUPPLEMENTARY INFORMATION:

Background

The USPTO is charged with promoting innovation through patent protection. U.S. Const., art. I, section 8. The patent system is a catalyst for jobs, economic prosperity, and world problem-solving. It fosters innovation by encouraging the public disclosure of ideas and by providing inventors time-limited exclusive rights to their patented innovation, thereby incentivizing research and development and investment in the same, as well as the investment necessary to bring that research and development to market. The patent system works most efficiently and effectively when the USPTO issues and maintains robust and reliable patents upon which patent owners and the public can rely to engage in technology transfer and licensing (including cross-licensing), invest in innovations to bring them to market and commercialize ideas, and/or to enforce patent rights.

Congress granted the Office "significant power to revisit and revise earlier patent grants" as a mechanism to "improve patent quality and restore confidence in the presumption of validity that comes with issued patents." *Cuozzo Speed Techs., LLC v. Lee*, 579 U.S. 261, 272 (2016) (quoting H.R. Rep. No. 112-98, pt. 1, at 45, 48). Congress also sought to ensure that the proceedings provided "a quick, inexpensive, and reliable alternative to district court litigation to resolve questions of patent validity." S. Rep. No. 110-259, at 20. At the same time, Congress instructed that "the changes made by [the AIA] are not to be used as tools for harassment or a means to prevent market entry through repeated litigation and administrative attacks on the validity of a patent," as "[d]oing so would frustrate the purpose of the section as providing quick and cost-effective alternatives to litigation." H.R. Rep. No. 112-98, at 48 (2011).

Under 35 U.S.C. 316(a) and 326(a), the Director shall prescribe regulations for certain enumerated aspects of AIA proceedings and 35 U.S.C. 2(b)(2)(A) gives the Director authority to establish regulations that "shall govern the conduct of proceedings in the Office." The proposed rules are in furtherance of this statutory authority.

The AIA gives the Director discretion to institute an IPR or PGR proceeding that satisfies the relevant statutory institution standard. Sections 314(a) and 324(a) of 35 U.S.C. provide the Director with discretion to deny a petition, even when meritorious. *See, e.g.*, 35 U.S.C. 314(a) (stating "[t]he Director may not authorize an *inter partes* review to be

instituted unless . . ."); *Cuozzo*, 579 U.S. at 273 ("[T]he agency's decision to deny a petition is a matter committed to the Patent Office's discretion."). The Director's discretion to institute an AIA trial is informed by 35 U.S.C. 316(b) and 326(b), which require that "the Director shall consider the effect of any such regulation on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted under" 35 U.S.C. 316 and 326. In addition, 35 U.S.C. 325(d) provides that "[i]n determining whether to institute or order a proceeding . . . , the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office."

The powers and discretion granted to the Director to determine whether to institute an AIA proceeding have been delegated to the PTAB. 35 U.S.C. 6(a), 314, 324; 37 CFR 42.4(a). To promote the delegated authority being exercised consistent with how the Director would exercise their discretion and consistently across panels, and to promote more transparency and consistency for those appearing before the PTAB and the public, the Director and the PTAB have issued guidance and precedential decisions. In particular, to take into account the 35 U.S.C. 316(b) and 326(b) considerations of the economy, the integrity of the patent system, and the ability of the USPTO to provide timely and cost-effective post-grant proceedings, as outlined in the AIA, this guidance and precedential decisions have set forth factors to consider when determining whether to institute an AIA review, including whether: (1) more than one AIA petition challenging the same patent is filed by the same petitioner at the same time as the first petition or up until the filing of the preliminary response in the first filed proceeding ("parallel petitions"); (2) additional AIA petitions are filed by the same petitioner (or privy or real party in interest with a petitioner) challenging overlapping claims of the same patent as the first petition after the patent owner has filed a preliminary response to the first petition ("serial" or "follow-on" petitions); or (3) an AIA petition relies on the same or substantially the same prior art or arguments previously addressed by the USPTO in connection with the challenged patent (implicating considerations under 35 U.S.C. 325(d)).

The changes under consideration would amend the rules of practice for IPR and PGR proceedings to codify and

build on that guidance and those precedential decisions as well as formalize PTAB's current practices, while creating more uniformity across PTAB panels. In proposing these changes, the Director considered "the effect of any such regulation on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted under" 35 U.S.C. 316 and 326. The Director has also considered the comments received from stakeholders, including those in response to the "Request for Comments on Discretion To Institute Trials Before the Patent Trial and Appeal Board" (85 FR 66502 (Oct. 20, 2020)), and received in response to the ANPRM titled "Changes Under Consideration to Discretionary Institution Practices, Petition Word-Count Limits, and Settlement Practices for America Invents Act Trial Proceedings Before the Patent Trial and Appeal Board" (88 FR 24503 (Apr. 21, 2023)). In light of the robust, extensive feedback from diverse stakeholders, and the Board's experience in implementing the AIA for over a decade, the Office proposes rule revisions intended to help ensure fairness, transparency, and efficiency. This rulemaking is consistent with comments received from stakeholders in response to the RFC and the ANPRM, as well as those received in other contexts, expressing a preference that key policy changes be made and formalized through rulemaking.

The Office is now proposing rules addressing a subset of topics from the ANPRM. The Office continues to consider issuing proposed rules, with associated opportunities to comment, on other topics raised in the ANPRM.

The Office proposes to incorporate into the rules the factors the Board will consider in determining whether to institute an IPR or PGR for parallel petitions and serial petitions as well as set forth the framework the Board will use to conduct an analysis under 35 U.S.C. 325(d) when determining whether to institute an IPR or PGR. These proposed changes enhance and build on existing precedent and guidance regarding the exercise of the Director's discretion to determine whether to institute an AIA proceeding.

Another proposed change would provide a procedure in which a patent owner may, in a separate paper filed prior to a preliminary response, request discretionary denial of institution, in which case each of the parties will have the opportunity, in a separate responsive briefing, to address relevant factors for discretionary denial. This

separate briefing avoids encroaching on the parties' word-count limits for briefing on the merits.

An additional proposed change would amend the rules of practice for the termination of proceedings in view of settlement to align the requirements for terminating proceedings pre- and post-institution, requiring that pre-institution settlement agreements be filed timely with the Board to support termination of a proceeding pre-institution. This proposed change would also align with the "Executive Order on Promoting Competition in the American Economy" (E.O. 14036, 86 FR 36987 (July 9, 2021)) by facilitating a depository for all settlement agreements in connection with contested cases, including AIA proceedings, to assist the Federal Trade Commission (FTC) and the Department of Justice (DOJ) in ensuring compliance with antitrust laws.

Development of the Changes Under Consideration

On September 16, 2011, the AIA was enacted into law (Pub. L. 112–29, 125 Stat. 284 (2011)), and in 2012, the USPTO implemented rules to govern Office practice for AIA proceedings, including IPRs, PGRs, covered business method (CBM) patent reviews, and derivation proceedings pursuant to 35 U.S.C. 135, 316, and 326 and AIA 18(d)(2). *See* 37 CFR part 42; Rules of Practice for Trials Before the Patent Trial and Appeal Board and Judicial Review of Patent Trial and Appeal Board Decisions, 77 FR 48612 (Aug. 14, 2012); Changes to Implement Inter Partes Review Proceedings, Post-Grant Review Proceedings, and Transitional Program for Covered Business Method Patents, 77 FR 48680 (Aug. 14, 2012); Transitional Program for Covered Business Method Patents—Definitions of Covered Business Method Patent and Technological Invention, 77 FR 48734 (Aug. 14, 2012). Additionally, the USPTO published a "Patent Trial Practice Guide" to advise the public on the general framework of the regulations, including the structure and times for taking action in each of the new proceedings. *See* Office Patent Trial Practice Guide, 77 FR 48756 (Aug. 14, 2012). Since then, the USPTO has designated numerous decisions in such proceedings as precedential or informative, issued several Director memoranda providing agency guidance on the PTAB's implementation of various statutory provisions, and issued several updates to the "Trial Practice Guide."

Prior Request for Comments Regarding Discretionary Institution

On October 20, 2020, the USPTO published an RFC to obtain feedback from stakeholders on case-specific approaches by the PTAB for exercising discretion on whether to institute an AIA proceeding and whether the USPTO should promulgate rules based on these approaches. *See* Request for Comments on Discretion To Institute Trials Before the Patent Trial and Appeal Board, 85 FR 66502 (Oct. 20, 2020). The USPTO received 822 comments from a wide range of stakeholders, including individuals, associations, law firms, companies, and three United States Senators. In January 2021, the USPTO published an executive summary encapsulating stakeholder feedback received from the RFC.¹

Prior Advance Notice of Proposed Rulemaking

On April 20, 2023, as a follow-up to the RFC, the USPTO published an ANPRM to obtain feedback from stakeholders on a range of concepts relating to how the Director, and, by delegation, the PTAB, exercises discretion to institute IPRs and PGRs under 35 U.S.C. 314(a), 324(a), and 325(d). *See* Changes Under Consideration to Discretionary Institution Practices, Petition Word-Count Limits, and Settlement Practices for America Invents Act Trial Proceedings Before the Patent Trial and Appeal Board, 88 FR 24503 (Apr. 20, 2023). In the ANPRM, the USPTO also solicited comments regarding whether it should provide a separate briefing process for discretionary institution arguments, and/or clarify that parties that settle prior to institution must file copies of any settlement agreements that exist with the PTAB.

Engagement on the ANPRM was extensive. During the two-month comment period, which ended on June 20, 2023, diverse stakeholders submitted over 14,500 comments, reflecting the nation's deep interest in shaping the future of the patent system. The comments provided support for, opposition to, and diverse recommendations on the concepts discussed. The Office appreciates the thoughtful comments and has considered and analyzed them thoroughly.

¹ USPTO, Executive Summary: Public Views on Discretionary Institution of AIA Proceedings (Jan. 2021), available at <https://www.uspto.gov/sites/default/files/documents/USPTOExecutiveSummaryofPublicViewsonDiscretionaryInstitutiononAIAProceedingsJanuary2021.pdf>.

The vast majority of comments were from individuals, whose views generally fell on the opposite ends of the spectrum—stating either that AIA review is an important protection against unwarranted litigation and unpatentable claims and the Office should have fewer bases for discretionarily denying review of patents or that AIA review is being misused, for example, to the detriment of small inventors.

The USPTO also received many comments from trade and legal associations representing numerous members, many of which provided detailed, point-by-point comments on each concept discussed in the ANPRM. Individual companies also weighed in, from large, established corporations to small startups. These comments also spanned the spectrum, with some supporting or opposing all or most of the concepts discussed.

Discussion of Proposed Changes

In this section, the Office describes the proposed changes to specific sections in part 42 of Title 37 of the Code of Federal Regulations. Each subsection describes a related group of regulatory changes and discusses stakeholder comments relevant to the proposed changes. The Office solicits additional comments on the specific proposed changes.

Definitions: Section 42.2

Section 42.2: Adds definitions of “serial petition” and “parallel petitions” as follows:

A “serial petition” is a petition that (1) challenges overlapping claims of the same patent that have already been challenged by the petitioner, the petitioner’s real party in interest, or a privy of the petitioner; and (2) is filed after (a) the filing of a patent owner preliminary response to the first petition; or (b) the expiration of the period for filing such a response under § 42.107(a)(2) or § 42.207(a)(2), or as otherwise ordered, if no preliminary response to the first petition is filed.

Discussion: Comments were mixed as to whether the definition of a serial petition should apply to petitions filed by parties other than the original petitioner, and what degree of relationship between the parties is sufficient to bring a subsequent petition under the definition of a serial petition. Some comments expressed uncertainty as to the definition of “significant relationship” as set forth in *Valve Corp. v. Electronic Scripting Products, Inc.*, IPR2019–00062, Paper 11 (PTAB Apr. 2, 2019), and asked for clarity as to the degree of relationship that would be

considered sufficient. The Office has determined that applying the real party in interest and privity concepts in exercising discretion in the serial petition context carries out Congress’s desire that the Director balance concerns about harassment in exercising discretion. Further, adopting the established common-law concepts of real party in interest and privity (see *Taylor v. Sturgell*, 553 U.S. 880 (2008)) provides a body of case law from which the PTAB and the public can draw when assessing whether the relationship between the parties is sufficiently significant to warrant discretionary denial. The Office notes that though *Valve* used the term “significant relationship” to examine the relationship between the petitioners, the analysis was consistent with privity concepts.

“Parallel petitions” are two or more petitions that (1) challenge the same patent and (2) are filed by the same petitioner on or before: (a) the filing of a patent owner preliminary response to any of the petitions, or (b) the due date set forth in § 42.107(a)(2) or § 42.207(a)(2) for filing a patent owner preliminary response to the first petition (if no patent owner preliminary response to the petitions is filed).

Discussion: In response to the ANPRM, some commenters expressed concern that the definition of parallel petitions in the ANPRM was overly restrictive, as the definition focused on petitions challenging the same “patent” as opposed to petitions challenging overlapping “claims” of the patent. The Office is moving forward with the “same patent” definition as opposed to the “overlapping claims” definition at this time to provide a mechanism for the Board to review filing behaviors to assess whether there are any abuses or misuses of the post-grant procedures, including ones that may place unwarranted and unnecessary burdens on the patent owner (e.g., filing, without explanation, multiple petitions challenging a single patent where each petition challenges a single claim of the patent). That said, even if two petitions are considered parallel under this definition, if the petitions challenge different claims given a large claim set or different art relevant to the different claim sets, the Board may still exercise its discretion to institute both petitions under proposed §§ 42.108(d) and 42.208(e).

Some commenters requested more clarity regarding the difference in timing between petitions the Office deems to be filed in parallel and those it deems to be filed serially. To provide better clarity on this issue, the Office proposes to

define a parallel petition in the rule as one filed during the time period for filing a patent owner preliminary response in the first proceeding. This timing reflects current practice, as noted in the Board’s 2019 Consolidated Trial Practice Guide.

Briefing on Motions for Discretionary Denial: Sections 42.24, 42.107, 42.207, 42.108(c)(1), 42.208(c)(1)

Section 42.24: Provides page limits for briefing on requests for discretionary denial (which are provided for in §§ 42.107 and 42.207, and which further provide that a patent owner may file the request for discretionary denial without Board authorization under 37 CFR 42.20(b)). A patent owner request for discretionary denial is limited to 10 pages, a petitioner opposition is also limited to 10 pages, and a patent owner sur-reply is limited to 5 pages.

Sections 42.107 and 42.207: Amend the rules on preliminary responses to provide that the patent owner preliminary response shall not address discretionary denial unless authorized by the Board, and further provide that a patent owner may raise and address discretionary denial issues in a separate request for discretionary denial of the petition, which would be limited to addressing any applicable discretionary institution issues and factors. Issues and factors applicable to requests for discretionary institution include those provided for in proposed §§ 42.108 and 42.208, except §§ 42.108(d) and 42.208(e) governing parallel petitions, as well as any issue that the patent owner believes warrants discretionary denial of the petition in view of the Office’s rules, precedents, or guidance. The proposed amendment also provides the following due dates: (1) a request for discretionary denial must be filed no later than two months after the date of a notice indicating that the petition to institute an IPR has been granted a filing date; (2) the opposition to the request must be filed no later than one month after the filing of the request for discretionary denial; and (3) a reply in support of the request must be filed no later than two weeks after the filing of the opposition. The proposed amendment also provides that the Board may *sua sponte* raise discretionary denial, in which case the Board will provide the parties with the opportunity for briefing on the relevant factors set forth in this section. However, nothing in the rules prevents the Board, when the circumstances warrant, from exercising discretion and authorizing the patent owner to include discretionary denial issues in the patent owner preliminary response. Further, to the extent the merits are relevant to

discretionary denial, the parties may direct the Board's attention to the petition and patent owner preliminary response for discussion of the merits as contained in those documents.

Sections 42.108(c)(1) and 42.208(c)(1): Provide that the Board's decision on institution will take into account a patent owner's request for discretionary denial when such a request is filed, including any opposition and reply.

Discussion: The Office has found the practice of allowing parties to file separate papers ranking their petitions in the order in which petitioner desires the Board to consider the merits is helpful in evaluating parallel petitions while preserving the parties' word count to focus on the merits of the challenge. The Office solicited feedback in the ANRPM on a similar procedure to allow parties to address discretionary denial in separate briefing. In response, most commenters favored separate briefing to discuss discretionary denial issues, noting that it would free up space in the petitions and patent owner responses to address the merits and allow more fulsome discussion of discretionary denial issues. That response is consistent with the responses the USPTO received from the RFC.

In response to the ANPRM, some commenters expressed concern that allowing separate briefing on discretionary denial would only favor petitioners because it would give a petitioner an automatic right to respond to a patent owner preliminary response. The proposed rules address these concerns by limiting the petitioner's opposition to the patent owner's request for discretionary denial to the issues raised in that request, and then allowing a patent owner the opportunity to file a reply brief limited to responding to the petitioner's opposition.

The USPTO also recognizes that there may be instances in which it is appropriate for the Office to address discretionary denial even if the patent owner does not file a request. The Office is further proposing amendments to §§ 42.107 and 42.207 to provide that the Board may raise discretionary denial *sua sponte*, in which case the Board will provide the parties with the opportunity for briefing.

Termination and Settlement Agreements: 37 CFR 42.72 and 42.74

Section 42.72: Revises the provisions for termination of a proceeding in view of settlement, clarifying that the Board may terminate a proceeding on its own initiative before or after institution. Provides that the parties may jointly move for termination of a proceeding, before or after institution.

Section 42.74: Provides that a joint motion for termination of a proceeding, filed before or after institution, must be accompanied by any written settlement agreement.

Discussion: Since FY2020, the settlement rate for AIA proceedings has been approximately 30% per year, with pre-institution being over 50% of the settlements each year. See https://www.uspto.gov/sites/default/files/documents/ptab_aia_fy2023_roundup.pdf. For consistency and predictability, the USPTO is proposing changes to the rules to ensure that pre-institution settlement agreements are filed with the Office, similar to post-institution settlement agreements. Although 35 U.S.C. 135(e), 317(b), and 327(b) require filing of settlement agreements made in connection with, or in contemplation of, the termination of an AIA proceeding that has been instituted, by their own terms these statutory provisions do not expressly govern AIA pre-institution settlement. See Rules of Practice for Trials Before the Patent Trial and Appeal Board and Judicial Review of Patent Trial and Appeal Board Decisions, 77 FR 48612, 48625 (Aug. 14, 2012) (final rule) (stating that "35 U.S.C. 135(e) and 317, as amended, and 35 U.S.C. 327 will govern settlement of Board trial proceedings but do not expressly govern pre-institution settlement"). Pursuant to the Board's authority to establish procedural rules for post-grant proceedings, 35 U.S.C. 316(a)(4) and 326(a)(4), we propose to extend the same practice required by statute to encompass current practice and require filing of pre-institution settlement agreements.

This proposed rule aligns with the policy set forth in Executive Order 14036, which encourages government agencies to cooperate on policing unfair, anticompetitive practices. In addition, having a depository for all settlement agreements in connection with contested cases, including AIA proceedings, in the USPTO would assist the FTC and the DOJ in determining whether antitrust laws have been violated.

Since the inception of AIA proceedings, the Board has been generally uniform in requiring the filing of a settlement agreement prior to terminating an AIA proceeding based on a joint motion by the parties, pre- or post-institution. Nevertheless, some petitioners have filed motions to dismiss or withdraw the petition before institution, arguing that they should not be required to file a copy of the parties' settlement agreements, and panels in some of those cases have granted the

motions and terminated the proceedings without requiring the parties to file their settlement agreements. See, e.g., *Samsung Elecs. Co. v. Telefonaktiebolaget LM Ericsson*,

IPR2021–00446, Paper 7 (PTAB Aug. 3, 2021) (Order—Dismissal Prior to Institution of Trial) (over the dissent of one Administrative Patent Judge (APJ)), granting the petitioner's motion to dismiss the petition and terminating the proceeding without requiring the parties to file their settlement agreements); *Huawei Techs. Co. v. Verizon Patent & Licensing Inc.*, IPR2021–00616, Paper 9 and IPR2021–00617, Paper 9 (PTAB Sept. 9, 2021) (Order—Dismissal Prior to Institution of Trial) (same dispute among a panel of APJs); *AEP Generation Res. Inc. v. Midwest Energy Emissions Corp.*, IPR2020–01294, Paper 11 (PTAB Dec. 14, 2020).

Stakeholder comments in response to the ANPRM were divided on whether the filing of pre-institution settlement agreements should be required to terminate a proceeding pre-institution. A number of comments supported the filing of pre-institution settlement agreements to provide greater transparency and to curb the potential for abusive filings. The Office agrees. The proposed changes provide consistency and predictability by making clear that pre-institution settlement agreements must be filed with the Office. This approach provides the USPTO a greater ability to monitor and curb potential abusive filings and, consistent with Executive Order 14036, allows the USPTO to cooperate with other government agencies to police unfair, anticompetitive practices.

A few ANPRM comments opposed the proposed requirement to file pre-institution settlement agreements, taking the position that the statute only requires the filing of agreements post-institution. Some believed that parties should have the option to voluntarily file pre-institution settlement agreements. A few comments expressed concern that the Office lacks authority to require the filing of settlement agreements to terminate a proceeding before institution. As noted above, the statute requires the filing of settlement agreements made in connection with, or in contemplation of, the termination of a proceeding that has been instituted, and is silent on AIA pre-institution settlement. The proposed rule is promulgated within the Director's authority to prescribe regulations establishing and governing an IPR under the AIA provisions. See 35 U.S.C. 316(a)(4).

Further, as discussed above, the Board has been generally uniform in requiring

the filing of a settlement agreement prior to terminating an AIA proceeding both pre- and post-institution, pursuant to 37 CFR 42.74(b). The proposed rule ensures greater predictability and consistency.

Some ANPRM comments expressed concern that requiring the filing of settlement agreements would discourage or complicate pre-institution settlement negotiations. As noted above, the proposed rule is consistent with the prior general uniform practice of the Board of requiring the filing of settlement agreements if parties would like termination based on settlement prior to a decision on institution. Any concerns regarding possible disclosure to nonparties of settlement terms from such filings have not been borne out in practice, given the availability of filing such documents with the designation “Board and Parties Only.”

Factors for Discretionary Denial: 37 CFR 42.108 and 42.208

Sections 42.108 and 42.208: Revise the rules for institution of IPRs to include factors to be addressed in consideration of discretionary denial on the basis of parallel petitions (§§ 42.108(d), 42.208(e)) and serial petitions (§§ 42.108(e), 42.208(f)), and in accordance with 35 U.S.C. 325(d) (§§ 42.108(f), 42.208(g)).

Sections 42.108(c)(1) and 42.208(c)(1) provide that the factors set forth for discretionary denial shall not be construed to limit the Board’s discretion to deny institution or dismiss a proceeding as a sanction or in response to evidence of improper conduct or gamesmanship.

Sections 42.108(c)(2) and 42.208(c)(2) provide that, in reaching a decision on institution of a petition accompanied by a timely motion for joinder to a petition that was instituted, the Board will not consider arguments against initiating that petition on the basis of discretionary considerations under §§ 42.108(d) and 42.208(e) (parallel petitions) or §§ 42.108(f) and 42.208(g) (petitions implicating 35 U.S.C. 325(d)) where those considerations were available in the already-instituted petition. However, the Board may deny motions for joinder and the later-filed petition where a patent owner successfully identifies other bases for discretionary denial.

Sections 42.108(d) and 42.208(e) provide that the Board will not institute parallel petitions absent a threshold showing of good cause as to why more than one petition is necessary. The petitioner must provide information relevant to a good cause determination either in the petition or a separate filing,

and the patent owner may respond in a separate filing. Various factors relevant to the good cause determination may be considered by the Board, including: (1) a petitioner’s ranking of their parallel petitions in the order in which petitioner wishes the Board to consider the merits, (2) an explanation of the differences between parallel petitions, (3) the number of claims challenged by the petitioner and asserted by the patent owner, (4) whether the parties dispute the priority date of the challenged patent, (5) whether there are alternative claim constructions requiring different prior art, (6) whether the petitioner lacked information at the time of filing the petition; and (7) the complexity of the technology in the case, as well as any other information believed to be pertinent to the good cause determination.

Sections 42.108(e) and 42.208(f) provide that the Board may deny institution of any serial petition when it challenges claims of the same patent that overlap with claims challenged in a previously filed petition for IPR, PGR, or CBM patent review. The Board will consider various factors in determining whether to deny institution of a serial petition, including: (1) whether, at the time of filing of the first petition, the petitioner knew of the prior art asserted in the second petition or should have known of it; (2) whether, at the time of filing of the second petition, the petitioner had already received the patent owner preliminary response to the first petition or had received the Board’s institution decision for the earlier petition; (3) the length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition; and (4) whether the petitioner provided an adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent. (As discussed below, these are factors (2) through (5) from the 2017 *General Plastic* precedential decision. Factor (1) from *General Plastic* is incorporated into the proposed rule’s definition of a “serial petition,” and factors (6) and (7) are not included in the proposed rule.)

Sections 42.108(f) and 42.208(g) provide that the Board may deny a petition for IPR under 35 U.S.C. 325(d) if the same or substantially the same prior art or arguments previously presented were meaningfully addressed by the Office with respect to the challenged patent or a related patent or application, unless the petitioner establishes material error in the Office’s previous evaluation. The rule provides

an opportunity for a patent owner to file a request for discretionary denial under 35 U.S.C. 325(d), for the petitioner to file an opposition, and for the patent owner to file a reply. The Board may deny the petition if section 325(d) is sufficiently implicated such that instituting on all grounds of unpatentability would not promote the efficient administration of the Office or support the integrity of the patent system.

Discussion

Statutory Authority

Some comments assert generally that discretionary denials frustrate Congress’s intent by depriving parties of the ability to seek AIA review. Some comments express the view that the Director does not have the authority to preclude serial or parallel petitions.

Congress specifically granted the Director of the USPTO the authority to institute a review. 35 U.S.C. 314 and 324. The AIA statute does not require the Director to institute a review in any case, and gives the Director discretion not to institute even where the statutory requirements for institution are met. The Director’s discretion is informed by 35 U.S.C. 316 and 326, which require that “the Director shall consider the effect of any such regulation on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings instituted under this chapter.” 35 U.S.C. 316 and 326. Congress also empowered the Director to prescribe regulations related to the implementation of the AIA. *See* 35 U.S.C. 316(a) and 326(a) (stating that the Director shall prescribe regulations for certain enumerated aspects of AIA proceedings). Under 35 U.S.C. 2(b)(2)(A), the Director may establish regulations that “shall govern the conduct of proceedings in the Office.” The language and intent of the above statutes therefore support evaluating whether parallel or serial petitions advance the mission and vision of the Office to promote innovation or the intent behind the AIA to provide a less-expensive alternative to district court litigation when exercising the Director’s discretion to institute. 35 U.S.C. 316(b) and 326(b). Also, under 35 U.S.C. 325(d), “the Director may take into account whether, and reject the petition or request because, the same or substantially the same prior art or arguments previously were presented to the Office.”

Parallel Petitions

Comments pertaining to parallel petitions challenging the same patent, as defined in § 42.2, were mixed.

Many comments supported denying parallel petitions absent a showing of good cause. Some comments that supported the concept of requiring a showing of good cause for filing parallel petitions asserted that this practice is in line with the congressional intent to allow discretionary denials based on the volume of AIA petitions. In line with these comments, the proposed rule implements the current practice of requiring that petitioners demonstrate why parallel petitions should be allowed to proceed. This framework supports the Office's goal of reducing duplicative challenges to a patent and balances the interests of parties by preventing undue harassment of patent owners through the filing of multiple challenges to a patent, while allowing petitioners reasonable opportunities to seek review.

Many comments asserted that denials of meritorious challenges are an unnecessary restraint on review. Yet, some comments urged that the restrictions on parallel petitions do not go far enough. Some urged greater restrictions on parallel petitions, asserting that most, if not all, parallel petitions should be denied to prevent companies from harassing patent owners. The proposed rule strikes a balance between denying all parallel petitions and instituting all parallel petitions that meet the statutory threshold for institution in 35 U.S.C. 314(a) and 35 U.S.C. 324(a) by requiring a showing by the petitioner of good cause as to why more than one petition is necessary.

Some comments asserted that there are no justifications for limiting multiple petitions because there is little, if any, evidence of petitioners abusing the system by filing multiple petitions. A USPTO study of parallel petitions found that from fiscal year 2015 through fiscal year 2018, parallel petitions represented roughly 15–18% of all challenges. https://www.uspto.gov/sites/default/files/documents/executive_summary_ptab_multiple_petitions_study_fy2021-2022_update.pdf. In fiscal year 2019, parallel petitions represented roughly 20% of all challenges, but then in fiscal years 2020 through 2022, the percent of challenges involving parallel petitions steadily dropped, down to roughly 7% in fiscal year 2022 (the final year of the study). See *id.* The decrease in the number of parallel petition filings was influenced by USPTO guidance (see Consolidated Trial Practice Guide

(2019)), which the USPTO is now codifying and clarifying through the rulemaking process.

Serial Petitions

Comments on proposed discretionary denials of serial petitions, as defined in § 42.2, were sharply divided, with most comments favoring either fewer or greater restrictions.

Some comments supported the adoption of the *General Plastic* factors as a compromise between denying all serial petitions and instituting all serial petitions that meet the statutory threshold for institution in 35 U.S.C. 314(a) and 35 U.S.C. 324(a). In *General Plastic Co. v. Canon Kabushiki Kaisha*, IPR2016–01357, 2017 WL 3917706, at *7 (PTAB Sept. 6, 2017) (precedential), the PTAB referred to the AIA's goals “to improve patent quality and make the patent system more efficient by the use of post-grant review procedures” but also “recognize[d] the potential for abuse of the review process by repeated attacks on patents.” 2017 WL 3917706, at *7 (citing H.R. Rep. No. 112–98, part 1, at 48 (2011)). To aid the Board's assessment of “the potential impacts on both the efficiency of the inter partes review process and the fundamental fairness of the process for all parties,” *General Plastic* identified a number of non-exclusive factors that the Board will consider in exercising discretion in instituting an IPR, especially as to “follow-on” petitions challenging a patent that was challenged previously in an IPR, PGR, or CBM proceeding. *Id.* at *8. The *General Plastic* non-exclusive factors include: (1) whether the same petitioner previously filed a petition directed to the same claims of the same patent; (2) whether, at the time of the filing of the first petition, the petitioner knew of the prior art asserted in the second petition or should have known of it; (3) whether, at the time of the filing of the second petition, the petitioner had already received a patent owner preliminary response (if filed) to the first petition or received the Board's decision on whether to institute review in the first petition; (4) the length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition; and (5) whether the petitioner provided an adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent. *Id.* at *7. Additional factors include: (6) the finite resources of the Board, and (7) the requirement to issue a final determination not later than one year after the date on which

the Director notices institution of review. *Id.*

The proposed serial petition definition and rules generally adopt the *General Plastic* factors approach, striking a balance between denying all serial petitions versus removing all restrictions on serial petitions. Specifically, *General Plastic* factor (1) is included in the definition of “serial petition” in § 42.2, and factors (2) through (5) are included in the proposed rules at § 42.108(e) and § 42.208(f). The other two *General Plastic* factors—(6) and (7)—are not proposed for regulatory adoption in light of stakeholder feedback that parties lack sufficient information to opine on the finite resources of the Board and the Board's ability to issue a final determination within one year. While the parties need not address existing factors (6) and (7), the Board may still weigh the considerations reflected by those factors in rendering its decision on serial petition issues.

Comments that urged greater restrictions on serial petitions asserted that most, if not all, serial petitions should be presumptively denied to prevent companies from harassing patent owners or contesting the same patent repeatedly. Some of these comments offered limited exceptions to presumptive denials, including requiring the petitioner to demonstrate it could not reasonably have discovered earlier the prior art presented in the subsequent petition and requiring a heightened burden for subsequent petitions of demonstrating unpatentability by clear and convincing evidence.

As discussed, the proposed rule implements the current practice of applying substantially the same factors as those stated in *General Plastic*. This framework supports the Office's goal of reducing duplicative challenges to a patent and balances the interests of parties by preventing undue harassment of patent owners through serial challenges while allowing petitioners reasonable opportunities to seek review.

A USPTO study of serial petitions filed by the same petitioner found a notable decrease in the filing of serial petitions, as well as institution of AIA trials based on serial petitions, after the Office issued *General Plastic* in late 2017. See https://www.uspto.gov/sites/default/files/documents/executive_summary_ptab_multiple_petitions_study_fy2021-2022_update.pdf. This data showed that in fiscal year 2015, serial petitions represented roughly 9.0% of all challenges, and in fiscal years 2016 and 2017 serial petitions represented roughly 8% of all

challenges. After the issuance of *General Plastic* in late 2017, serial petition filings began immediately dropping, representing 5.6% of filings in fiscal year 2018, approximately 2% of filings fiscal years 2019 and 2020, 1.4% of filings in fiscal year 2021, and 1.7% of filings in fiscal year 2022. Additionally, of the 17 petitions involving a serial petition attempt by the same petitioner in fiscal year 2022, only 3 petitions resulted in institution (roughly 18%), as compared to 42 out of 99 serial petition filings that resulted in institution (roughly 42%) in fiscal year 2015. Although the data suggests that only small number of serial petition challenges continue to occur each year, in the wake of *General Plastic*, the USPTO believes that there is a public benefit to codifying and clarifying the existing practice related to serial petition challenges through the rulemaking process.

Some stakeholders commented that multiple filings are often the result of a patent owner's litigation tactics. The Office believes the articulated factors provide adequate means to strike the appropriate balance between denying and allowing all serial petitions because they allow the Board to weigh relevant and appropriate evidence and, for example, to identify instances of improper roadmapping, in which a petitioner engages in a litigation tactic to gain an advantage by tailoring a "follow on" petition based on information gleaned from a patent owner's preliminary response to an earlier petition. As the Board noted in *General Plastic*: "Multiple, staggered petitions challenging the same patent and same claims raise the potential for abuse. The absence of any restrictions on follow-on petitions would allow petitioners the opportunity to strategically stage their prior art and arguments in multiple petitions, using our decisions as a roadmap, until a ground is found that results in the grant of review." 2017 WL 3917706, at *7.

Previously Presented Art or Arguments

On March 24, 2020, the Office designated as precedential *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020). This precedent lays out a two-part framework for evaluating whether to exercise discretion under 325(d). The first part of the test relates to whether the same or substantially the same art or arguments were previously presented to the Office. The second part of the test looks to whether the petitioner has demonstrated that the Office erred in a

manner material to the patentability of the challenged claims.

The Office does not have any studies evaluating the impact of the *Advanced Bionics* precedent on the application of 325(d). Comments received in response to the ANPRM, however, generally expressed the view that *Advanced Bionics* provides the public with a simplified framework for evaluating 325(d) issues, even if application of the *Advanced Bionics* framework would not alter the outcome of the majority of cases where 325(d) issues arose.

Specific comments on the application of 35 U.S.C. 325(d) to deny petitions on the basis of previously presented prior art or arguments were split, primarily on the question of whether the Office should consider prior art that was made of record, but not applied or substantively discussed by the examiner, as having been "previously presented."

Some comments supported a proposed rule that would limit the application of discretionary denial under section 325(d) to situations in which the prior art was previously applied or substantively discussed during examination. One comment stated that applying discretionary denial in situations in which prior art was listed on an Information Disclosure Statement (IDS), without more involvement in examination, would encourage "dumping" of references on the Office during prosecution. Another comment agreed that a requirement that a prior art reference be previously addressed would increase efficiency by providing a clear test that reduces unnecessary briefing.

Section 325(d) provides discretion for the Director, when determining whether to institute a proceeding, to take into account whether the same (or substantially the same) art or arguments were previously presented to the Office. The USPTO agrees that the application of section 325(d) should be limited to situations in which the prior art or arguments were meaningfully addressed by the Office. The proposed rule provides that art or arguments are deemed to have been meaningfully addressed where the Office has evaluated the art or arguments and articulated its consideration of the art or arguments in the record of the application from which the patent issued or the record of a related application or patent with claims that are substantially the same. For purposes of this section, an application or patent is "related" to the challenged patent if it claims priority to a common application or is a parent application or parent patent of the challenged patent.

This definition of "related application or patent" only applies to part 42 and does not apply to other sections that discuss the term (e.g., 37 CFR 1.77(b)(2), 1.78(d)(5)).

Some comments favored the broader application of discretionary denial in circumstances in which prior art references were made of record during prosecution (such as on an IDS) but not applied or substantively discussed by the examiner. Comments expressed concern that requiring a patent owner to identify prior art or arguments that were meaningfully addressed by the Office is inconsistent with the text of 325(d). One comment noted patent applicants do not have control over what references an examiner chooses to cite in the record and believed that excluding art that was merely cited on an IDS may deter compliance with the duty of disclosure. Another comment expressed concern with a blanket rule that section 325(d) only applies to art and arguments previously evaluated by the Office. One comment suggested that if prior art and arguments are limited to art and arguments addressed by the Office, petitioners should face a higher "material error" burden. In response to the concern that patent applicants do not have control over what references an examiner chooses to address, the rule does not prevent patent applicants from drawing attention to specific references.

As noted above, 35 U.S.C. 325(d) gives the Director the authority to take into account whether the same or substantially the same prior art was previously presented to the Office, but does not require the Director to do so. After careful consideration of the comments, and to best support the integrity of the patent system, the USPTO proposes to limit the application of 325(d) to circumstances in which the same or substantially the same prior art or arguments previously presented to the Office were meaningfully addressed by the Office. Under these circumstances, the proposed rule installs the current Board practice of requiring petitioners to establish a "material error" by the Office. *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020) (precedential). A material error may include misapprehending or overlooking clear, specific evidence in the prior record, including teachings of the relevant prior art that impact the patentability of the challenged claims; evidence demonstrating an inherent feature of the prior art; or evidence rebutting a showing of unexpected results. A material error may also include a legal error, including an

erroneous claim construction that impacts the patentability of the challenged claims.

The proposed rule also seeks to carry out the purpose of 325(d), and give appropriate deference to prior findings made by the Office when meaningfully addressing prior art references, by focusing on instances in which a petitioner seeks to apply a reference in a manner that is directly contrary to prior Office findings. The proposed rule thus defines “the same prior art” as a reference that forms the basis of a challenge in a petition, where that reference was previously meaningfully addressed by the Office and the petition relies on the reference for a factual proposition that directly contradicts a finding made by the Office when the reference was previously meaningfully addressed. Therefore, if the “same prior art” was meaningfully addressed, the petition may be denied under 35 U.S.C. 325(d) unless the petitioner establishes material error by the Office.

The proposed rule ensures greater predictability and consistency in the application of 325(d) and focuses the application of 325(d) on circumstances in which the prior record is clear. The proposed rule further supports the Office’s goal of reducing duplicative challenges to a patent by considering whether the same or substantially the same challenge was meaningfully addressed by the Office previously. The proposed rule does not reduce or eliminate a patent applicant’s duty of disclosure under 37 CFR 1.56.

One comment suggested that where a patent owner asserts that the same or substantially the same prior art was previously presented in a related application, the requirement for the patent owner to identify how the claims are substantially the same as those in the challenged patent should only apply to related applications that are not direct ancestors.

Under the proposed rule, a patent owner must identify, in a request for discretionary denial under 35 U.S.C. 325(d), where the same or substantially the same prior art or arguments were meaningfully addressed by the Office. If the art or arguments were previously evaluated by the Office in the record of a related application, the patent owner must establish that the art or arguments were previously evaluated with respect to claims that are substantially the same as the claims in the challenged patent. Claims in a direct ancestor patent may not be substantially the same as those in the challenged patent, and therefore the requirement of establishing that the claims are substantially the same as those in the challenged patent to related

applications that are not direct ancestors is still necessary. Additionally, where the claims are substantially the same as those in a related application, a petitioner could identify inconsistent positions taken by an examiner in the related application as part of its burden of establishing material error.

Discretionary Denial Considerations for Joinder Petitions

Proposed rule § 42.208(c)(2) installs current Board practice regarding the analysis of 35 U.S.C. 325(d) and parallel petition issues in the joinder context. Joinder petitions may present the same discretionary denial considerations as the petition upon which the IPR sought to be joined was instituted. See *Facebook, Inc. v. Windy City Innovations, LLC*, 973 F.3d 1321, 1335–38 (Fed. Cir. 2020) (holding that 35 U.S.C. 315(c) prohibits a joined party from bringing new issues through its petition into the proceeding being joined). Additionally, section 325(d) or parallel petition issues implicated by the joinder petition were already implicated by the previously instituted petition. Issues raised by discretionary considerations under 35 U.S.C. 325(d) are directed to the prosecution history of the challenged patent and to whether the same or substantially the same prior art or arguments were previously presented to the Office. Arguments under section 325(d) were available to the patent owner in the context of the already instituted petition. Similarly, parallel petition issues require the showing of good cause for multiple petitions filed by the same petitioner based on particular considerations (e.g., the number of claims the petitioner is challenging, whether there is a priority date dispute, whether there are alternative claim constructions, the number of claims the patent owner is asserting in litigation, etc.). In the scenario in which a joinder petitioner seeks to join multiple instituted IPRs, the need to justify multiple IPR trials is implicated by the already instituted petitions.

Accordingly, under current practice, Board panels presented with 35 U.S.C. 325(d) or parallel petition issues for joinder petitions have declined to consider those issues in light of the decision to institute the previously instituted petition(s) to be joined. In order to maintain consistency with current practice, in reaching a decision on institution of a petition accompanied by a timely motion for joinder, Board panels will not consider arguments on discretionary considerations under § 42.108(d) (parallel petitions) or § 42.108(f) (35 U.S.C. 325(d)) where the

petition(s) sought to be joined was instituted and those discretionary considerations were available in the already instituted petition. The Board may, however, deny motions for joinder where the later-filed petition implicates other bases for discretionary denial.

Rulemaking Considerations

A. Administrative Procedure Act: The changes proposed by this rulemaking involve rules of agency practice and procedure, and/or interpretive rules, and do not require notice-and-comment rulemaking. See *Perez v. Mortg. Bankers Ass’n*, 575 U.S. 92, 97, 101 (2015) (explaining that interpretive rules “advise the public of the agency’s construction of the statutes and rules which it administers” and do not require notice and comment when issued or amended); *Cooper Techs. Co. v. Dudas*, 536 F.3d 1330, 1336–37 (Fed. Cir. 2008) (stating that 5 U.S.C. 553, and thus 35 U.S.C. 2(b)(2)(B), do not require notice-and-comment rulemaking for “interpretative rules, general statements of policy, or rules of agency organization, procedure, or practice”); and *JEM Broadcasting Co. v. F.C.C.*, 22 F.3d 320, 328 (D.C. Cir. 1994) (explaining that rules are not legislative because they do not “foreclose effective opportunity to make one’s case on the merits”).

Nevertheless, the USPTO is publishing this proposed rule for comment to seek the benefit of the public’s views on the Office’s proposed regulatory changes.

B. Regulatory Flexibility Act: For the reasons set forth in this notice, the Senior Counsel for Regulatory and Legislative Affairs, Office of General Law, USPTO, has certified to the Chief Counsel for Advocacy of the Small Business Administration that changes set forth in this notice of proposed rulemaking (NPRM) would not have a significant economic impact on a substantial number of small entities. See 5 U.S.C. 605(b).

The changes in this NPRM set forth express modifications to the rules of practice for IPR and PGR proceedings before the PTAB that the Director and, by delegation, the PTAB, will use in exercising discretion to institute IPRs and PGRs under 35 U.S.C. 314(a), 324(a), and 325(d). The changes pertaining to discretionary institution are largely formalizing existing Board practice, as set forth in precedential decisions and the Trial Practice Guide. Additionally, the changes allowing parties to separately brief discretionary institution issues and the filing of pre-existing settlement agreements prior to

institution would not cause any party to incur significant additional cost.

As a result, the Office estimates that any requirements resulting from these proposed changes would create little, if any, additional burden to those practicing before the Board. The Office proposes to formalize rules that, for the most part, implement current PTAB practices with regard to discretionary denial of serial and parallel petitions for review, petitions implicating considerations under 35 U.S.C. 325(d), procedures for separate briefing on discretionary denial, and practices regarding termination due to settlement. Accordingly, any economic impact would be minimal.

Regarding parallel petitions, the proposed rule providing that the Board will not institute parallel petitions absent a showing of good cause as to why more than one petition is necessary reflects current practice. The Board's Consolidated Trial Practice Guide (November 2019) already makes clear that one petition should be sufficient in most situations and requires petitioners to rank any parallel petitions. In response to stakeholder comments, the proposed rule articulates specific circumstances that may establish good cause and promotes greater efficiency and transparency in the Board's determination whether to go forward with parallel petitions. Accordingly, the proposed change is expected to have minimal economic impact.

With regard to serial petitions, the proposed rule adopts the factors set forth in the Board's precedential decision in *General Plastic*. Accordingly, the proposed rule generally reflects current practice, including practice based on binding precedent, to reduce duplicative proceedings, and is expected to have minimal economic impact.

With regard to petitions implicating considerations under 35 U.S.C. 325(d), the proposed rule clarifies that mere prior citation of prior art in an IDS will not automatically satisfy the first prong of the analytical framework in the Board's decision in *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 8 (PTAB Feb. 13, 2020) (precedential). The proposed rule resolves an issue that has caused confusion and resulted in unnecessary briefing and the consumption of significant time and effort in the past in the absence of credible evidence that the art or arguments were meaningfully addressed by the Office. Accordingly, the proposed change is expected to mitigate the need for parties and the Board to expend resources in trying to assess examiner

error where the examiner did not meaningfully address the art and arguments. As such, the proposed rule is expected to increase efficiency for the parties and the Board and therefore is not expected to have a significant economic impact.

The proposed rule regarding separate briefing on discretionary denial issues is likewise expected to increase efficiency for the parties and the Board. The parties already brief the same issues and provide the same information that would be presented in the separate briefing in any existing patent owner preliminary response and any petitioner sur-reply, but will merely do so in a different format going forward. The proposed rule will help highlight and focus attention on the key issues concerning discretionary denial. As such, the proposed rule will not substantially change existing practice and is unlikely to have any significant economic impact.

Finally, with respect to practices regarding termination, the proposed change aligns the requirements for terminating proceedings pre- and post-institution by clarifying that pre-institution settlement agreements must be filed with the Board for termination of a proceeding, which includes pre-institution terminations as well as post-institution terminations. This proposal aligns with already widespread practice, where most parties requesting termination pre-institution have provided such agreements. 35 U.S.C. 135(e), 317(b), and 327(b), concerning settlement, do not expressly address settlements pre-institution, but the Board has been generally uniform in requiring agreements to be filed prior to termination. As such, the proposed rule reflects existing practice and eliminates potential confusion. Under the proposed rule, parties will simply be filing existing documents, not creating any additional documents, and accordingly, any cost for compliance will be minimal.

For these reasons, the proposed changes in this NPRM would not have a significant economic impact on a substantial number of small entities.

C. Executive Order 12866 (Regulatory Planning and Review): This rulemaking is significant under Executive Order 12866 (Sept. 30, 1993), as amended by Executive Order 14094 (Apr. 6, 2023).

D. Executive Order 13563 (Improving Regulation and Regulatory Review): The Office has complied with Executive Order 13563 (Jan. 18, 2011).

Specifically, and as discussed above, the Office has, to the extent feasible and applicable: (1) made a reasoned determination that the benefits justify

the costs of the rule; (2) tailored the rule to impose the least burden on society consistent with obtaining the regulatory objectives; (3) selected a regulatory approach that maximizes net benefits; (4) specified performance objectives; (5) identified and assessed available alternatives; (6) involved the public in an open exchange of information and perspectives among experts in relevant disciplines, affected stakeholders in the private sector, and the public as a whole, and provided online access to the rulemaking docket; (7) attempted to promote coordination, simplification, and harmonization across Government agencies and identified goals designed to promote innovation; (8) considered approaches that reduce burdens and maintain flexibility and freedom of choice for the public; and (9) ensured the objectivity of scientific and technological information and processes.

E. Executive Order 13132 (Federalism): This rulemaking pertains strictly to federal agency procedures and does not contain policies with federalism implications sufficient to warrant preparation of a Federalism Assessment under Executive Order 13132 (Aug. 4, 1999).

F. Executive Order 13175 (Tribal Consultation): This rulemaking will not: (1) have substantial direct effects on one or more Indian tribes, (2) impose substantial direct compliance costs on Indian tribal governments, or (3) preempt tribal law. Therefore, a tribal summary impact statement is not required under Executive Order 13175 (Nov. 6, 2000).

G. Executive Order 13211 (Energy Effects): This rulemaking is not a significant energy action under Executive Order 13211 because this rulemaking is not likely to have a significant adverse effect on the supply, distribution, or use of energy. Therefore, a Statement of Energy Effects is not required under Executive Order 13211 (May 18, 2001).

H. Executive Order 12988 (Civil Justice Reform): This rulemaking meets applicable standards to minimize litigation, eliminate ambiguity, and reduce burden as set forth in sections 3(a) and 3(b)(2) of Executive Order 12988 (Feb. 5, 1996).

I. Executive Order 13045 (Protection of Children): This rulemaking does not concern an environmental risk to health or safety that may disproportionately affect children under Executive Order 13045 (Apr. 21, 1997).

J. Executive Order 12630 (Taking of Private Property): This rulemaking will not affect a taking of private property or otherwise have taking implications

under Executive Order 12630 (Mar. 15, 1988).

K. Congressional Review Act: Under the Congressional Review Act provisions of the Small Business Regulatory Enforcement Fairness Act of 1996 (5 U.S.C. 801 *et seq.*), prior to issuing any final rule, the USPTO will submit a report containing the rule and other required information to the United States Senate, the United States House of Representatives, and the Comptroller General of the Government Accountability Office. The changes in this NPRM are not expected to result in an annual effect on the economy of \$100 million or more; a major increase in costs or prices; or significant adverse effects on competition, employment, investment, productivity, innovation, or the ability of United States-based enterprises to compete with foreign-based enterprises in domestic and export markets. Therefore, this rulemaking is not a “major rule” as defined in 5 U.S.C. 804(2).

L. Unfunded Mandates Reform Act of 1995: The changes set forth in this NPRM do not involve a Federal intergovernmental mandate that will result in the expenditure by State, local, and tribal governments, in the aggregate, of \$100 million (as adjusted) or more in any one year, or a Federal private sector mandate that will result in the expenditure by the private sector of \$100 million (as adjusted) or more in any one year, and will not significantly or uniquely affect small governments. Therefore, no actions are necessary under the provisions of the Unfunded Mandates Reform Act of 1995. *See* 2 U.S.C. 1501 *et seq.*

M. National Environmental Policy Act of 1969: This rulemaking will not have any effect on the quality of the environment and is thus categorically excluded from review under the National Environmental Policy Act of 1969. *See* 42 U.S.C. 4321 *et seq.*

N. National Technology Transfer and Advancement Act of 1995: The requirements of section 12(d) of the National Technology Transfer and Advancement Act of 1995 (15 U.S.C. 272 note) are not applicable because this rulemaking does not contain provisions that involve the use of technical standards.

O. Paperwork Reduction Act of 1995: The Paperwork Reduction Act of 1995 (44 U.S.C. 3501 *et seq.*) requires that the Office consider the impact of paperwork and other information collection burdens imposed on the public. This NPRM involves information collection requirements that are subject to review by the Office of Management and Budget (OMB) under the Paperwork

Reduction Act of 1995 (44 U.S.C. 3501 *et seq.*). The collection of information involved in this rulemaking have been reviewed and previously approved by OMB under OMB control numbers 0651–0069. This rulemaking does not add any additional information requirements or fees for parties before the Board.

Notwithstanding any other provision of law, no person is required to respond to, nor shall any person be subject to, a penalty for failure to comply with a collection of information subject to the requirements of the Paperwork Reduction Act unless that collection of information displays a currently valid OMB control number.

P. E-Government Act Compliance: The USPTO is committed to compliance with the E-Government Act to promote the use of the internet and other information technologies, to provide increased opportunities for citizen access to Government information and services, and for other purposes.

List of Subjects in 37 CFR Part 42

Administrative practice and procedure, Inventions and patents, Lawyers.

For the reasons set forth in the preamble, the Office proposes to amend 37 CFR part 42 as follows:

PART 42—TRIAL PRACTICE BEFORE THE PATENT TRIAL AND APPEAL BOARD

■ 1. The authority citation for 37 CFR part 42 is revised to read as follows:

Authority: 35 U.S.C. 2(b)(2), 6, 21, 23, 41, 135, 311–319, 321–329; Pub. L. 112–129, 125 Stat. 284; and Pub. L. 112–274, 126 Stat. 2456.

■ 2. Amend § 42.2 by adding, in alphabetical order, the definitions for “parallel petitions” and “serial petition” to read as follows:

§ 42.2 Definitions.

* * * * *

Parallel petitions means two or more petitions that:

(1) Challenge the same patent by the petitioner; and

(2) Are filed on or before:

(i) The filing of the first patent owner preliminary response to any of the petitions; or

(ii) The due date set forth in § 42.107(a)(2) or § 42.207(a)(2) for filing a patent owner preliminary response to the first petition, if no patent owner preliminary response to the petitions is filed.

* * * * *

Serial petition means a petition that:

(1) Challenges same or overlapping claims of the same patent that have already been challenged by the petitioner, the petitioner’s real party in interest, or a privy of the petitioner; and

(2) Is filed after:

(a) The filing of a patent owner preliminary response to the first petition; or

(b) The expiration of the period for filing such a response under § 42.107(a)(2) or § 42.207(a)(2), or as otherwise ordered, if no preliminary response to the first petition is filed.

* * * * *

■ 3. Amend § 42.24 by adding paragraph (e) to read as follows:

§ 42.24 Type-volume or page limits for petitions, motions, oppositions, replies, and sur-replies.

* * * * *

(e) *Requests for discretionary denial.*

The following page limits apply to briefing in connection with a patent owner request for discretionary denial but do not include a table of contents; a table of authorities; a listing of facts that are admitted, denied, or cannot be admitted or denied; a certificate of service; or an appendix of exhibits:

(1) *Patent owner request:* 10 pages.

(2) *Petitioner opposition:* 10 pages.

(3) *Patent owner reply:* 5 pages.

■ 4. Revise § 42.72 to read as follows:

§ 42.72 Termination of proceeding.

(a) *The Board may terminate a proceeding.* The Board may terminate a proceeding, where appropriate, before institution or after institution, including where the proceeding is consolidated with another proceeding or pursuant to a joint request under 35 U.S.C. 317(a) or 327(a).

(b) *Motion for termination of a proceeding.* With prior authorization from the Board, parties may file a joint request for termination of a proceeding before institution, or after institution pursuant to 35 U.S.C. 317(a) or 327(a), by filing a joint motion accompanied by any written agreement or understanding, including any collateral agreements, between the parties as required by § 42.74.

■ 5. Amend § 42.74 by revising paragraph (b) to read as follows:

§ 42.74 Settlement.

* * * * *

(b) *Agreements in writing.* Any agreement or understanding between the parties made in connection with, or in contemplation of, the termination of a proceeding shall be in writing, and a true copy shall be filed with the Board before the termination of a proceeding.

* * * * *

■ 6. Amend § 42.107 by revising the section heading and paragraphs (a) and (b) to read as follows:

§ 42.107 Preliminary response to petition and request for discretionary denial.

(a) *Patent owner preliminary response.* (1) The patent owner may file a preliminary response to the petition. The response is limited to setting forth the reasons why no *inter partes* review should be instituted under 35 U.S.C. 314 based on issues other than discretionary denial, and can include supporting evidence. The preliminary response is subject to the word count under § 42.24. A patent owner preliminary response shall not address discretionary denial, which may only be raised pursuant to § 42.107(b), unless otherwise authorized by the Board.

(2) The preliminary response must be filed no later than three months after the date of a notice indicating that the petition to institute an *inter partes* review has been granted a filing date. A patent owner may expedite the proceeding by filing an election to waive the patent owner preliminary response.

(b) *Request for discretionary denial.*

(1) In addition to a preliminary response to the petition, the patent owner may file a single request for discretionary denial of the petition. 37 CFR 42.20(b) notwithstanding, no prior Board authorization is required to file the single request for discretionary denial. The request is limited to addressing any applicable discretionary institution issues and factors, other than those involving parallel petitions under § 42.108(d). Applicable discretionary institution issues include those enumerated in § 42.108(e) and (f), as well as any issue that the patent owner believes, based on Office rules, precedent, or guidance, warrants discretionary denial of the petition. If the patent owner files a request for discretionary denial, the petitioner may file an opposition limited to the issues raised in the request, and the patent owner may file a reply limited to the issues raised in the opposition. The request, opposition, and reply are subject to the page limits under § 42.24(e). The Board may also *sua sponte* raise any applicable discretionary denial issue, in which case the Board will provide an opportunity for briefing by the parties.

(2) A request for discretionary denial must be filed no later than two months after the date of a notice indicating that the petition to institute an *inter partes* review has been granted a filing date. An opposition to the request for discretionary denial must be filed no

later than one month after the filing of the request for discretionary denial. A reply in support of the request must be filed no later than two weeks after the filing of the opposition.

* * * * *

■ 7. Amend § 42.108 by revising paragraph (c) and adding paragraphs (d) through (f) to read as follows:

§ 42.108 Institution of inter partes review.

* * * * *

(c) *Institution considerations.* *Inter partes* review shall not be instituted unless the Board decides that the information presented in the petition demonstrates that there is a reasonable likelihood that at least one of the claims challenged in the petition is unpatentable. The Board's decision will take into account a patent owner preliminary response when such a response is filed, including any testimonial evidence. A petitioner may seek leave to file a reply to the preliminary response in accordance with §§ 42.23 and 42.24(c). Any such request must make a showing of good cause.

(1) *Consideration of discretionary denial.* The Board's decision will also take into account, when filed, a patent owner's request for discretionary denial, including any opposition and reply, and a petitioner's filing pursuant to § 42.108(d). To the extent the patent owner contends that there are substantive weaknesses in the petitioner's grounds of unpatentability that are relevant to the exercise of discretion under 35 U.S.C. 314(a), the patent owner may indicate in their request that they will address those substantive weaknesses in the preliminary response permitted by § 42.107(a). Nothing in § 42.108 shall be construed to limit the Board's discretion to deny institution or dismiss a proceeding as a sanction or for any other reason deemed warranted by the Board.

(2) *Discretionary considerations for joined petitions.* In reaching a decision on institution of a petition accompanied by a timely motion for joinder, the Board will not consider arguments on discretionary considerations under § 42.108(d) (parallel petitions) or § 42.108(f) (35 U.S.C. 325(d)) where the petition sought to be joined was instituted. However, the Board may deny the accompanying motion for joinder where the later-filed petition implicates other bases for discretionary denial.

(d) *Parallel petitions challenging the same patent.* The Board will not institute parallel petitions, as defined in § 42.2, absent a showing of good cause as to why more than one petition is

necessary. A petitioner filing a parallel petition may, either in the petition or in a separate paper filed concurrently with the petition and limited to no more than five pages, provide information relevant to the good cause determination. 37 CFR 42.20(b) notwithstanding, the patent owner is authorized, without prior Board authorization, to file a separate paper of no more than five pages, on or before the deadline for the preliminary response, limited to providing an explanation of why the Board should not institute more than one petition. Information relevant to the good cause determination may include:

(1) A petitioner's ranking of their petitions in the order in which petitioner desires the Board to consider the merits of their petitions relative to the other parallel petitions;

(2) An explanation of the differences between the petitions and why the issues addressed by the differences are material;

(3) The number of patent claims of the challenged patent that have been asserted by the patent owner in district court litigation;

(4) The number of claims the petitioner is challenging;

(5) Whether there is a dispute about the priority date of the challenged patent;

(6) Whether there are alternative claim constructions that require different prior art references on mutually exclusive grounds;

(7) Whether the petitioner lacked information, such as the identity of asserted claims, at the time they filed the petitions;

(8) The complexity of the technology in the case; and

(9) Any other information believed to be pertinent to the good cause determination.

(e) *Institution factors for serial petitions.* The Board, in its discretion, may deny institution of any serial petition, as defined in § 42.2, for *inter partes* review challenging claims of the same patent that overlap with claims challenged in a previously filed petition for *inter partes* review, post-grant review, or covered business method patent review. The Board will consider the following factors in determining whether to deny institution:

(1) Whether, at the time of filing of the first petition, the petitioner knew of the prior art asserted in the second petition or should have known of it;

(2) Whether, at the time of filing of the second petition, the petitioner had already received the patent owner preliminary response to the first petition or had received the Board's decision on

whether to institute review in the first petition;

(3) The length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition; and

(4) Whether the petitioner provided an adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent.

(f) *Discretion based on previously presented art or arguments.* A petition for *inter partes* review may be denied under 35 U.S.C. 325(d) if the same or substantially the same prior art was previously meaningfully addressed by the Office or the same or substantially the same arguments were previously meaningfully addressed by the Office with regard to the challenged patent or a related patent or application, unless the petitioner establishes material error by the Office. If some, but not all, of the grounds of unpatentability presented in a petition implicate considerations under 35 U.S.C. 325(d), the Board may deny the petition if section 325(d) is sufficiently implicated such that instituting on all grounds of unpatentability would not promote the efficient administration of the Office or support the integrity of the patent system.

(1) *Request to deny institution pursuant to discretion under 35 U.S.C. 325(d).* A patent owner may file a request for discretionary denial under 35 U.S.C. 325(d) under the provisions of § 42.107(b). Such request must identify whether the same or substantially the same prior art was previously meaningfully addressed by the Office and/or whether the same or substantially the same arguments were previously meaningfully addressed by the Office. A petitioner may file an opposition under the provisions of § 42.107(b) to argue that the same or substantially the same prior art or arguments were not previously meaningfully addressed by the Office and/or to argue that there was material error by the Office. The patent owner may file a reply to the opposition under the provisions of § 42.107(b).

(2) *The same prior art.* Prior art is deemed to be “the same prior art” if a reference that forms the basis of the challenges in the petition was previously meaningfully addressed by the Office and the petition relies on the reference for a factual proposition that directly contradicts a finding made by the Office when the reference was previously meaningfully addressed.

(3) *Substantially the same prior art.* Prior art is “substantially the same prior

art” if the disclosure in the prior art previously meaningfully addressed by the Office contains the same teaching as that relied upon in the petition.

(4) *Meaningfully addressed art or arguments.* Art or arguments are deemed to have been meaningfully addressed when the Office has evaluated the art or arguments and articulated its consideration of the art or arguments in the record of the patent or the application from which the patent issued or the record of a related application or patent with claims that are substantially the same. An initialed Information Disclosure Statement, without more, does not satisfy this standard. Art or arguments from a related application or patent will only be considered to be meaningfully addressed if they are addressed by the Office before the issuance of the challenged patent.

(5) *Related application or patent.* For purposes of this section, an application or patent is “related” to the challenged patent if it claims priority to a common application or is a parent application or parent patent of the challenged patent.

■ 8. Amend § 42.207 by revising the section heading and paragraphs (a) and (b) to read as follows:

§ 42.207 Preliminary response to petition and request for discretionary denial.

(a) *Patent owner preliminary response.* (1) The patent owner may file a preliminary response to the petition. The response is limited to setting forth the reasons why no post-grant review should be instituted under 35 U.S.C. 324 based on issues other than discretionary denial, and can include supporting evidence. The preliminary response is subject to the word count under § 42.24. A patent owner preliminary response shall not address discretionary denial, which may only be raised pursuant to paragraph (b) of this section, unless otherwise authorized by the Board.

(2) The preliminary response must be filed no later than three months after the date of a notice indicating that the petition to institute a post-grant review has been accorded a filing date. A patent owner may expedite the proceeding by filing an election to waive the patent owner preliminary response.

(b) *Request for discretionary denial.* (1) In addition to a preliminary response to the petition, the patent owner may file a single request for discretionary denial of the petition. Section 42.20(b) notwithstanding, no prior Board authorization is required to file the single request for discretionary denial. The request is limited to addressing any applicable discretionary institution

issues and factors other than those involving parallel petitions under § 42.208(e). Applicable discretionary institution issues include those enumerated in § 42.208(f) and (g), as well as any issue that the patent owner believes, based on Office rules, precedent, or guidance, warrants discretionary denial of the petition. If the patent owner files a request for discretionary denial, the petitioner may file an opposition limited to the issues raised in the request, and the patent owner may file a reply limited to the issues raised in the opposition. The request, opposition, and reply are subject to the page limits under § 42.24(e). The Board may also *sua sponte* raise discretionary denial, in which case the Board will provide an opportunity for briefing by the parties.

(2) A request for discretionary denial must be filed no later than two months after the date of a notice indicating that the petition to institute a post-grant review has been accorded a filing date. An opposition to the request for discretionary denial must be filed no later than one month after the filing of the request for discretionary denial. A reply in support of the request must be filed no later than two weeks after the filing of the opposition.

* * * * *

■ 9. Amend § 42.208 by revising paragraph (c) and adding paragraphs (e) through (g) to read as follows:

§ 42.208 Institution of post-grant review.

* * * * *

(c) *Institution considerations.* Post-grant review shall not be instituted unless the Board decides that the information presented in the petition demonstrates that there is a reasonable likelihood that at least one of the claims challenged in the petition is unpatentable. The Board’s decision will take into account a patent owner preliminary response when such a response is filed, including any testimonial evidence. A petitioner may seek leave to file a reply to the preliminary response in accordance with §§ 42.23 and 42.24(c). Any such request must make a showing of good cause.

(1) *Consideration of discretionary denial.* The Board’s decision will also take into account, where filed, a patent owner’s request for discretionary denial, including any opposition and reply, and a petitioner’s filing pursuant to § 42.208(e). To the extent the patent owner contends that there are substantive weaknesses in the petitioner’s grounds of unpatentability that are relevant to the exercise of discretion under 35 U.S.C. 324(a), the

patent owner may indicate in their request that they will address those substantive weaknesses in the preliminary response permitted by § 42.207(a). Nothing in this section shall be construed to limit the Board's discretion to deny institution or dismiss a proceeding as a sanction or for any other reason deemed warranted by the Board.

(2) *Discretionary considerations for joined petitions.* In reaching a decision on institution of a petition accompanied by a timely motion for joinder, the Board will not consider arguments on discretionary considerations under paragraph (e) of this section (parallel petitions) or paragraph (g) of this section (35 U.S.C. 325(d)) where the petition sought to be joined was instituted. However, the Board may deny the accompanying motion for joinder where the later-filed petition implicates other bases for discretionary denial.

* * * * *

(e) *Parallel petitions challenging the same patent.* The Board will not institute parallel petitions, as defined in § 42.2, absent a showing of good cause as to why more than one petition is necessary. A petitioner filing a parallel petition may, either in the petition or in a separate paper filed concurrently with the petition and limited to no more than five pages, provide information relevant to the good cause determination. Section 42.20(b) notwithstanding, the patent owner is authorized, without prior Board authorization, to file a separate paper of no more than five pages, on or before the deadline for the preliminary response, limited to providing an explanation of why the Board should not institute more than one petition. Information relevant to the good cause determination may include:

(1) A petitioner's ranking of their petitions in the order in which petitioner desires the Board to consider the merits of their petitions relative to their other parallel petitions;

(2) An explanation of the differences between the petitions and why the issues addressed by the differences are material;

(3) The number of patent claims of the challenged patent that have been asserted by the patent owner in district court litigation;

(4) The number of claims the petitioner is challenging;

(5) Whether there is a dispute about the priority date of the challenged patent;

(6) Whether there are alternative claim constructions that require different prior art references on mutually exclusive grounds;

(7) Whether the petitioner lacked information, such as the identity of asserted claims, at the time they filed the petitions;

(8) The complexity of the technology in the case; and

(9) Any other information believed to be pertinent to the good cause determination.

(f) *Institution factors for serial petitions.* The Board, in its discretion, may deny institution of any serial petition, as defined in § 42.2, for post-grant review challenging claims of the same patent that overlap with claims challenged in a previously filed petition for *inter partes* review, post-grant review, or covered business method patent review. The Board will consider the following factors in determining whether to deny institution:

(1) Whether, at the time of filing of the first petition, the petitioner knew of the prior art asserted in the second petition or should have known of it;

(2) Whether, at the time of filing of the second petition, the petitioner had already received the patent owner preliminary response to the first petition or had received the Board's decision on whether to institute review in the first petition;

(3) The length of time that elapsed between the time the petitioner learned of the prior art asserted in the second petition and the filing of the second petition; and

(4) Whether the petitioner provided an adequate explanation for the time elapsed between the filings of multiple petitions directed to the same claims of the same patent.

(g) *Discretion based on previously presented art or arguments.* A petition for post-grant review may be denied under 35 U.S.C. 325(d) if the same or substantially the same prior art was previously meaningfully addressed by the Office or the same or substantially the same arguments were previously meaningfully addressed by the Office with regard to the challenged patent or a related patent or application, unless the petitioner establishes material error by the Office. If some, but not all, of the grounds of unpatentability presented in a petition implicate considerations under 35 U.S.C. 325(d), the Board may deny the petition if section 325(d) is sufficiently implicated such that instituting on all grounds of unpatentability would not promote the efficient administration of the Office or support the integrity of the patent system.

(1) *Request to deny institution pursuant to discretion under 35 U.S.C. 325(d).* A patent owner may file a request for discretionary denial under

35 U.S.C. 325(d) under the provisions of § 42.207(b). Such request must identify whether the same or substantially the same prior art was previously meaningfully addressed by the Office and/or whether the same or substantially the same arguments were previously meaningfully addressed by the Office. A petitioner may file an opposition under the provisions of § 42.207(b) to argue that the same or substantially the same prior art or arguments were not previously meaningfully addressed by the Office and/or to argue that there was material error by the Office. The patent owner may file a reply to the opposition under the provisions of § 42.207(b).

(2) *The same prior art.* Prior art is deemed to be "the same prior art" if a reference that forms the basis of the challenges in the petition was previously meaningfully addressed by the Office and the petition relies on the reference for a factual proposition that directly contradicts a finding made by the Office when the reference was previously meaningfully addressed.

(3) *Substantially the same prior art.* Prior art is "substantially the same prior art" if the disclosure in the prior art previously meaningfully addressed by the Office contains the same teaching as that relied upon in the petition.

(4) *Meaningfully addressed art or arguments.* Art or arguments are deemed to have been meaningfully addressed when the Office has evaluated the art or arguments and articulated its consideration of the art or arguments in the record of the patent or the application from which the patent issued or the record of a related application or patent with claims that are substantially the same. An initialed Information Disclosure Statement, without more, does not satisfy this standard. Art or arguments from a related application or patent will only be considered to be meaningfully addressed if they are addressed by the Office before the issuance of the challenged patent.

(5) *Related application or patent.* For purposes of this section, an application or patent is "related" to the challenged patent if it claims priority to a common application or is a parent application or parent patent of the challenged patent.

Dated: April 15, 2024.

Katherine K. Vidal,
Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office.

[FR Doc. 2024-08362 Filed 4-18-24; 8:45 am]

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9/9/25, 5:04 PM

USPTO rescinds memorandum addressing discretionary denial procedures | USPTO

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> USPTO rescinds memorandum addressing discretionary denial procedures



Update: On March 24, 2025, the USPTO published an updated [Guidance memorandum on USPTO's rescission of "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation"](#), which can be found in the Guidance Memorandum section of the [PTAB resources page](#).

USPTO rescinds memorandum addressing discretionary denial procedures

February 28, 2025

Today, the USPTO rescinded the June 21, 2022, memorandum entitled "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation" (Memorandum).

Parties to post-grant proceedings should refer to Patent Trial and Appeal Board (PTAB) precedent for guidance, including [Apple Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 \(PTAB Mar. 20, 2020\) \(precedential\)](#) and [Sotera Wireless, Inc. v. Masimo Corp., IPR2020-01019, Paper 12 \(PTAB Dec. 1, 2020\) \(precedential as to § II.A\)](#).

To the extent any other PTAB or Director Review decisions rely on the Memorandum, the portions of those decisions relying on the Memorandum shall not be binding or persuasive on the PTAB.

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USPTO rescinds memorandum addressing discretionary denial procedures | USPTO

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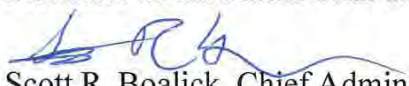


United States Patent and Trademark Office

Patent Trial and Appeal Board

MEMORANDUM

To: Members of the Patent Trial and Appeal Board

From: 
Scott R. Boalick, Chief Administrative Patent Judge

Subject: Guidance on USPTO's rescission of "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation"

Date: March 24, 2025

On February 28, 2025, the USPTO rescinded the June 21, 2022 memorandum entitled "Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation" ("Interim Procedure"). The Interim Procedure was intended to provide guidance while the USPTO explored potential rulemaking, but the USPTO did not subsequently propose a final rule addressing the Director's and, by delegation, the Patent Trial and Appeal Board's ("Board") exercise of discretionary institution in an *inter partes* review ("IPR") or a post-grant review ("PGR") in view of a parallel litigation. In the absence of rulemaking, the USPTO rescinded the Interim Procedure to restore policy in this area to the guidance in place before the Interim Procedure, including the Board's precedential decisions in *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (PTAB Mar. 20, 2020) ("*Fintiv*") and *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (PTAB Dec. 1, 2020) ("*Sotera*"). This memorandum sets forth additional guidance.

First, the Interim Procedure's recission applies to any case in which the Board has not issued an institution decision, or where a request for rehearing or Director Review of an institution decision was filed and remains pending. The Board will consider timely requests for additional briefing on the application of the Interim Procedure's recission on a case-by-case basis. Absent extraordinary circumstances, the Board will not revisit a decision on institution if the time for seeking Director Review or rehearing has passed.

Second, the Board will apply the *Fintiv* factors when there is a parallel proceeding at the International Trade Commission ("ITC"). As the *Fintiv* decision explains, although an ITC final invalidity determination does not have preclusive effect, it is difficult as a practical matter to assert patent claims that the ITC has determined are invalid. *See Fintiv*, Paper 11 at 8–9. Additionally, instituting an IPR or a PGR where the ITC has set a target date for completing its investigation (i.e., the full Commission's final determination) to occur earlier than the Board's deadline to issue a final written decision in a challenge involving the same patent claims means that multiple tribunals may be adjudicating validity at the same time, which may increase duplication and expenses for the parties and the tribunals. Thus, the Board is more likely to deny institution where the ITC's projected final determination date is earlier than the Board's deadline to issue a final written decision, and the Board is less likely to deny institution under *Fintiv* where the ITC projected final determination date is after the Board's deadline to issue a final written decision.

Third, a timely-filed *Sotera* stipulation¹ (i.e., a stipulation from a petitioner that, if an IPR or PGR is instituted, the petitioner will not pursue in district court

¹ *See NXP USA, Inc. v. Impinj, Inc.*, IPR2021-01556, Paper 13 (Sept. 7, 2022) (precedential) (holding that the only appropriate time for a petitioner to offer a stipulation is prior to the Board's decision on institution).

(or in the ITC) any ground raised or that could have been reasonably raised in the IPR/PGR) is highly relevant, but will not be dispositive by itself. Instead, the Board will consider such a stipulation as part of its holistic analysis under *Fintiv*.

Fourth, in applying *Fintiv*, the Board may consider any evidence that the parties make of record that bears on the proximity of the district court's trial date or the ITC's final determination target date, including median time-to-trial statistics for civil actions in the district court in which the parallel litigation resides.

Fifth, as stated in *Fintiv*, the factors considered in the exercise of discretion are part of a balanced assessment of all the relevant circumstances in the case, including the strength of the merits. However, compelling merits alone is not dispositive in making the assessment.

MEMORANDUM

To: All PTAB Judges

From: Coke Morgan Stewart 
Acting Under Secretary of Commerce for Intellectual Property
and Acting Director of the United States Patent and Trademark Office

Subject: Interim Processes for PTAB Workload Management

Date: March 26, 2025

The Patent Trial and Appeal Board (PTAB) is tasked with several statutory duties under 35 U.S.C. § 6(b), including deciding *ex parte* appeals from adverse examiner decisions by patent applicants and conducting America Invents Act (AIA) trial proceedings, such as *inter partes* reviews (IPRs) and post-grant reviews (PGRs). To ensure that the PTAB continues to meet its statutory obligations as to *ex parte* appeals, while continuing to maintain its capacity to conduct AIA proceedings, the Director will exercise her discretion on institution of AIA proceedings under 35 U.S.C. §§ 314(a) and 324(a) as outlined below.

First, decisions on whether to institute an IPR or PGR will be bifurcated between (i) discretionary considerations and (ii) merits and other non-discretionary statutory considerations. Under this interim procedure, the Director, in consultation with at least three PTAB judges, will determine whether discretionary denial of institution is appropriate. If it is appropriate, the Director will issue a decision denying institution. If it is not appropriate, the Director will issue a decision regarding that determination and refer the petition to a three-member panel of the PTAB assigned according to Standard Operating Procedure (SOP) 1 (Rev. 16). The three-member panel will then handle the case in the normal course including by issuing a decision on institution addressing the merits and other non-discretionary statutory considerations.

Second, to facilitate this bifurcated approach, the USPTO will permit parties to file separate briefing on requests for discretionary denial of institution. The discretionary denial briefing shall proceed as follows: (1) within two months of the date on which the PTAB enters a Notice of Filing Date Accorded to a petition, a patent owner may file a brief explaining any applicable bases for discretionary denial of institution; and (2) a petitioner may file an opposition brief no later than one month after the patent owner files its brief. Leave to file further briefing may be permitted for good cause. Consistent with 37 C.F.R. § 42.24, discretionary denial briefing will be limited to 14,000 words. A reply brief, if any, will be limited to 5,600 words. The merits briefing schedule and the schedule for requesting rehearing or Director Review as to a decision on institution remain unchanged.

Third, consistent with the discretionary considerations enumerated in existing Board precedent (including *Fintiv*, *General Plastic*, and *Advanced Bionics**) and the Consolidated Trial Practice Guide (Nov. 2019), the parties are permitted to address all relevant considerations, which may include:

- Whether the PTAB or another forum has already adjudicated the validity or patentability of the challenged patent claims;
- Whether there have been changes in the law or new judicial precedent issued since issuance of the claims that may affect patentability;
- The strength of the unpatentability challenge;
- The extent of the petition's reliance on expert testimony;
- Settled expectations of the parties, such as the length of time the claims have been in force;
- Compelling economic, public health, or national security interests; and

* *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential); *Gen. Plastic Indus. Co. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 (Sept. 6, 2027) (precedential as to § II.B.4.i); *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (Feb. 13, 2020) (precedential).

- Any other considerations bearing on the Director's discretion.

The Director will also consider the ability of the PTAB to comply with pendency goals for *ex parte* appeals, its statutory deadlines for AIA proceedings, and other workload needs. *See* 35 U.S.C. § 316(b).

These processes aim to improve PTAB efficiency, maintain PTAB capacity to conduct AIA proceedings, reduce pendency in *ex parte* appeals, and promote consistent application of discretionary considerations in the institution of AIA proceedings. The processes described herein will be implemented in IPR and PGR proceedings where the deadline for the patent owner to file a preliminary response has not yet passed. In that situation, if the time for filing discretionary denial briefing as described herein has already elapsed, the patent owner may submit discretionary denial briefing within one month of the date of this memorandum.

The processes described herein are temporary in nature due, in part, to the current workload needs of the PTAB.

[Director Discretionary Decision@uspto.gov](mailto:Director_Discretionary_Decision@uspto.gov)

571-272-7822

Paper 21

Date: June 18, 2025

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE OFFICE OF THE UNDER SECRETARY OF COMMERCE
FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE
UNITED STATES PATENT AND TRADEMARK OFFICE

DABICO AIRPORT SOLUTIONS INC.,
Petitioner,

v.

AXA POWER APS,
Patent Owner.

IPR2025-00408
Patent 9,771,169 B2

Before COKE MORGAN STEWART, *Acting Under Secretary of
Commerce for Intellectual Property and Acting Director of the United States
Patent and Trademark Office.*

DECISION

Granting Patent Owner's Request for Discretionary Denial and Denying
Institution of *Inter Partes* Review

IPR2025-00408

Patent 9,771,169 B2

AXA Power ApS (“Patent Owner”) filed a request for discretionary denial (Paper 10, “DD Req.”) in the above-captioned case, and Dabico Airport Solutions Inc. (“Petitioner”) filed an opposition (Paper 17, “DD Opp.”)

After considering the parties’ arguments and the record, and in view of all relevant considerations, discretionary denial of institution is appropriate in this proceeding. This determination is based on the totality of the evidence and arguments the parties have presented.

Some facts counsel against discretionary denial. For example, Patent Owner’s arguments regarding 35 U.S.C. § 325(d) are unpersuasive.

However, the considerations favoring discretionary denial outweigh those that counsel against it. In particular, the challenged patent has been in force almost eight years, creating settled expectations. *See* Ex. 1001. The interim processes permit a patent owner to file a brief explaining why discretionary denial is appropriate and the petitioner not only to respond to patent owner’s arguments but also to identify reasons *not to exercise discretion to deny institution*. As the Office has explained, “the parties are permitted to address all relevant considerations . . . bearing on the Director’s discretion.”¹ The Office further has explained that “[p]arties are encouraged to address any fact or circumstance they believe bears on whether the Office *should* or should not institute trial.”²

¹ Memorandum for Interim Processes for PTAB Workload Management at 2–3, *available at* <https://www.uspto.gov/sites/default/files/documents/InterimProcesses-PTABWorkloadMgmt-20250326.pdf>.

² FAQ 20, *FAQs for Interim Processes for PTAB Workload Management* (“FAQs”), *available at* <https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management> (emphasis added).

IPR2025-00408
Patent 9,771,169 B2

Petitioner does not provide any persuasive reasoning why an *inter partes* review is an appropriate use of Office resources. There may be persuasive reasons why the Office should review the challenged patent, but, in the absence of any such information, the Office is disinclined to disturb the settled expectations of Patent Owner in this instance.

Although there is no bright-line rule on when expectations become settled, in general, the longer the patent has been in force, the more settled expectations should be. This approach aligns with other approaches to settled expectations and incentives, for example, for filing infringement lawsuits. *Cf.* 35 U.S.C. § 286 (“Except as otherwise provided by law, no recovery shall be had for any infringement committed more than six years prior to the filing of the complaint or counterclaim for infringement in the action.”).

Moreover, patent applications (after 18 months) and issued patents are almost always publicly available to provide notice to the public, other inventors, competitors, and commercial interests. 35 U.S.C. § 122. Interested parties may find published patents and patent applications using the Office’s automated search systems as well as publicly available resources on the Internet. *See* 35 U.S.C. § 41(i). As such, actual notice of a patent or of possible infringement is not necessary to create settled expectations.

Although certain arguments are highlighted above, the determination to exercise discretion to deny institution is based on a holistic assessment of all of the evidence and arguments presented. Accordingly, the Petition is denied under 35 U.S.C. § 314(a).

In consideration of the foregoing, it is:

IPR2025-00408
Patent 9,771,169 B2

ORDERED that Patent Owner's request for discretionary denial is *granted*; and

FURTHER ORDERED that the Petition is *denied*, and no trial is instituted.

IPR2025-00408
Patent 9,771,169 B2

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND WESTERN DIGITAL
TECHNOLOGIES, INC.,
Petitioner

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner.

IPR2025-00515
U.S. Patent No. 9,183,085

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

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PETITIONER’S EXHIBIT LIST

Ex.1001	U.S. Patent No. 9,183,085 (“the ’085 patent”)
Ex.1002	Prosecution History of U.S. App. No. 13/477,600 (issued as ’085 patent) (“’600 App”)
Ex.1003	Declaration of Dr. Lara Dolecek (“Dolecek Decl.”)
Ex.1004	CV of Dr. Lara Dolecek
Ex.1005	U.S. Pub. 2014/0136927 to Li, et al.
Ex.1006	U.S. 9,037,951 to Cideciyan, et al.
Ex.1007	U.S. Patent No. 8,176,360 to Frost et al.
Ex.1008	U.S. 2008/0222490 to Leung et al.
Ex.1009	Solid-State Drive (SSD) Requirements and Endurance Test Method, JESD218, JEDEC STANDARD, September 2010
Ex.1010	U.S. 7,823,043 to Lasser
Ex.1011	U.S. 8,042,029 to Alrod et al.
Ex.1012	Performance Impact and Interplay of SSD Parallelism through Advanced Commands, Allocation Strategy and Data Granularity, Hu et al., ICS ’11: Proceedings of the international conference on Supercomputing, pp. 96 – 107 (https://doi.org/10.1145/1995896.1995912), May 31, 2011
Ex.1013	FTL Design Exploration in Reconfigurable High-Performance SSD for Server Applications, ICS '09: Proceedings of the 23rd international conference on Supercomputing, pp. 338 – 349 (https://doi.org/10.1145/1542275.1542324), June 8, 2009
Ex.1014	Flash Management – Why and How?, A Detailed Overview of Flash Management Techniques, SMART Modular Technologies, 2009
Ex.1015	Complaint, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)

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Ex.1016	District Court Trial Statistics
Ex.1017	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, June 22, 2022
Ex.1018	Solid State Drives 101, Cactus Technologies, available at https://www.cactus-tech.com/wp-content/uploads/2019/04/Solid-State-Drives-101-EBook.pdf
Ex.1019	Product Code Schemes for Error Correction in MLC NAND Flash Memories, Yang et al., December 29, 2011, available at: https://ieeexplore.ieee.org/document/6118315 .
Ex.1020	Error Control Coding Fundamentals and Applications, Lin et. al, 1983
Ex.1021	Scheduling and Case Management Order, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)

I. INTRODUCTION

U.S. Patent No. 9,183,085 (“the ’085 patent”) is directed to memory systems such as flash memory systems, and more specifically to adaptively selecting an error correcting coding (ECC) scheme based on an observed bit error rate, to address memory degradation over its lifetime. Ex.1001, Abstract. As shown herein, a single prior art reference – Li (Ex.1005) – teaches or suggests nearly all the features of the challenged claims. Other references are used merely to provide obvious example implementations or to supplement teachings that are suggested in Li.

Accordingly, pursuant to 35 U.S.C. §§ 311, 314(a), and 37 C.F.R. § 42.100, Petitioner respectfully requests that the Board review and cancel as unpatentable under (pre-AIA) 35 U.S.C. § 103(a) claims 1-2, 4-7, 14-18, 22-25, and 29-33 (the “Challenged Claims”).

II. GROUNDS FOR STANDING

Petitioner certifies that the ’085 patent is eligible for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims. 37 C.F.R. § 42.104(a).

III. NOTE

Petitioner cites to exhibits’ original page numbers. Emphasis in quoted material has been added.

IV. BACKGROUND

Error Correction Coding (ECC) is a well-known technique by which a memory controller can detect and correct data errors in a memory system. There are many different types of ECC schemes, some being more robust than others in certain situations. One type of memory system that uses ECC is a flash memory system, e.g., a flash based Solid-State Drive (SSD). Dr. Dolecek’s declaration provides a brief background section describing flash memory systems, error correction code techniques including product code, and SSDs. Ex.1003, 25-46.

V. THE ’085 PATENT

The ’085 patent is directed toward adaptively selecting an ECC scheme from a plurality of such schemes based on data error rate. Ex.1001, Title. The ’085 patent criticizes the conventional approaches of “specifying a particular strength of ECC code” through the total service life. Ex.1001, 1:63-2:1; 2:23-27; Ex.1003, ¶¶ 47-48.

One purported novelty of the ’085 patent is “**Adaptive ECC**” (Ex.1001, 48:47), which selects from ECC schemes of different ECC strengths (corresponding to “gears”) based on an observed bit error rate. *See also* Ex.1001, Title, 51:1-2; Ex.1003, ¶49.

VI. PROSECUTION HISTORY OF THE ’085 PATENT

The ’085 patent application was filed on May 22, 2012. In response to the

rejections, Patentee amended the claims to recite “determining a bit error rate associated with a region comprising a fixed number of two or more flash memory pages or integer fractions thereof, wherein the region stores at least data payload and primary and secondary ECC parity symbols corresponding to the data payload of the region.” (see limitations [1.1.1] and [1.1.2]). Ex.1002, 614-630. The amended claims were again rejected based on prior art. Ex.1002, 642-679.

In response, patentee amended the claims to recite “wherein the two or more flash memory pages of a region can be read simultaneously,” (see limitation [1.1.1]), which resulted in allowance. Ex.1002, 693-705, 715-719.

VII. LEVEL OF ORDINARY SKILL IN THE ART

A Person of Ordinary Skill in The Art (“POSITA”) as of May 22, 2012 would have had a working knowledge of the flash memory system art, including flash memories, memory controllers, and ECC art as applied to flash memory systems that is pertinent to the ’085 patent. A POSITA would have had a bachelor’s degree in electrical engineering, or an equivalent, and approximately two years of professional experience relating to the field of flash memory systems, including ECC technologies as applied to flash memory systems. Lack of professional experience can be remedied by additional education, and vice versa. Ex.1003, ¶¶14-18.

VIII. CLAIM CONSTRUCTION

In light of the prior art, no claim term other than the terms identified below requires construction. EX.1003, ¶¶55-59.

A. “*gear*” (claim 1)

A POSITA would have understood that “*gear*” is defined by the specification as follows:

In the context of this disclosure, a “*gear*” is a set of parameter(s) specifying an error correction coding scheme, including one or more of the payload capacity, the type and parameters of each component code, the interleaving scheme, and parameters used for determining whether the gear is appropriate for a particular situation. For example, the “Gear 1” sections of Tables III, IV, and V, plus the Threshold G1, collectively define Gear 1.

Ex.1001, 20:18-25; Ex.1003, ¶¶57-58.

B. Means-Plus-Function Terms

Claims 24-25 include means-plus-function claim terms. Construction of means-plus-function claim terms that invoke 35 U.S.C. §112, ¶6, requires identifying the claim terms and identifying corresponding structure disclosed in the specification that performs the identified functions and equivalents thereof. These means-plus-function claim terms are identified below at [24.1.1], [24.2.1], [24.3],

[25.0], and [25.1], together with the corresponding structure disclosed in the specification.

IX. RELIEF REQUESTED AND THE REASONS FOR RELIEF

Petitioner asks that the Board institute a trial for *inter partes* review and cancel the Challenged Claims in view of the analysis below.

X. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

A. Challenged Claims

Petitioner challenges claims 1-2, 4-7, 14-18, 22-25, and 29-33 of the '085 patent.¹

B. Prior Art Patents and Printed Publications

1. U.S. Pub. 2014/0136927 to Li, et al. ("Li") (Ex.1005), PCT filed October 26, 2011, published May 15, 2014; is prior art under §§102(a) and (e).
2. U.S. 9,037,951 to Cideciyan, et al. ("Cideciyan") (Ex.1006), PCT filed December 12, 2010, PCT published June 23, 2011, issued May 19, 2015; is prior art under §§102(a) and (e).
3. US 8,176,360 to Frost, et al. ("Frost") (Ex.1007), filed September 5, 2009, published February 17, 2011, issued May 8, 2012; is prior art under §§102(a) and (b).

¹ The pre-AIA statutory framework applies to the '085 patent.

4. US 2008/0222490 to Leung et al. (“Leung”) (Ex.1008), filed March 8, 2007, published September 11, 2008; is prior art under §§102(a) and (b).

Li (Ex.1005) and patents related to Frost (Ex.1007, specifically US 8,255,620; 8,560,881; and 8,713,245) were cited during the original prosecution, but were never relied upon by the Office. Ex.1002, 633, 730.

Cideciyan (Ex.1006) and Leung (Ex.1008) were not cited during the original prosecution. As explained in detail below, Cideciyan addresses the claim 1 limitations: “*wherein the two or more flash memory pages of a region can be read simultaneously*” and “*wherein the region stores at least data payload and primary and secondary ECC parity symbols corresponding to the data payload of the region*” which served as a basis for allowance during the original prosecution.

C. Statutory Grounds for Challenges

Grounds	Claims	Basis
#1	1-2, 4-5, 14-17, 22-25, 29-33	Obvious under §103 over Li and Cideciyan
#2	1-2, 4-5, 14-17, 22-25, 29-33	Obvious under §103 over Li, Cideciyan, and Frost
#3	6-7, and 18	Obvious under §103 over Li, Cideciyan, and Leung
#4	6-7, and 18	Obvious under §103 over Li, Cideciyan, Frost, and Leung

D. Prior Art

Li is the primary prior art reference for each ground listed above. Cideciyan, Frost, and Leung are secondary references provided to show various teachings or example implementation details that would be obvious for Li to use. Ex.1003, ¶60.

1. Li

As shown in FIGS. 1 and 2A below, Li, like the '085 patent, relates to “adaptive ECC techniques for flash memory based data storage.” Ex.1005, Title, [0126]; Ex.1003, ¶62.

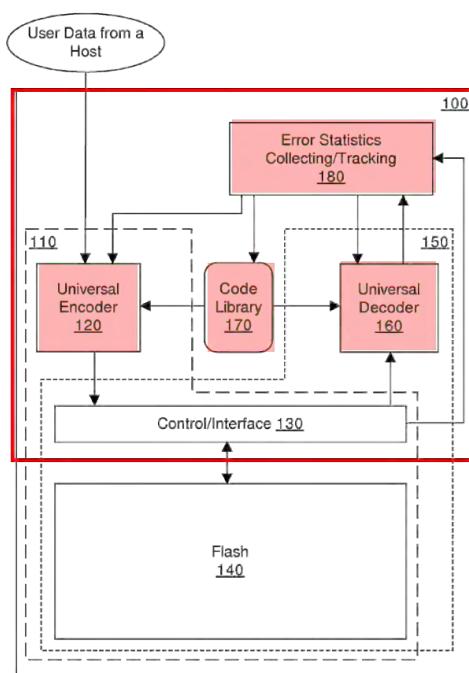


Fig. 1

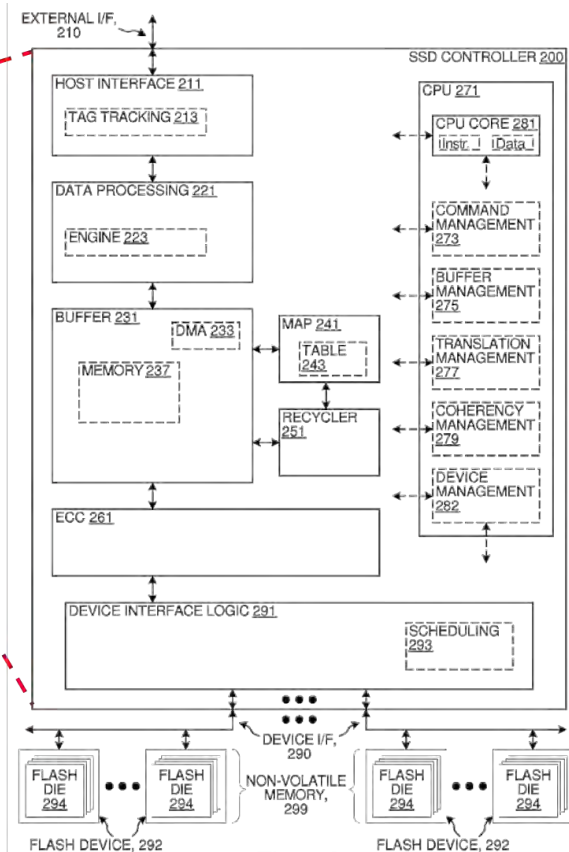


Fig. 2A

Ex.1005, FIGS. 1 and 2A, annotated.

Li states that “**adaptive ECC** techniques for use with flash memory enable improvements in flash memory lifetime, reliability, performance, and/or storage capacity.” Ex.1005, [0019]. “The techniques include **a set of ECC schemes** with **various code types, code rates, and/or various code lengths** (providing **different error correcting capabilities**), and **error statistic collecting/tracking**.” *Id.* Li also describes conditions (e.g., thresholds) used to determining whether a particular ECC scheme is appropriate for a particular situation. Ex.1005, [0105]. Further discussion of these terms, including common examples, is provided in the expert declaration. Ex.1003, ¶¶63-64.

Li’s adaptive ECC scheme selection is performed on the basis of a “portion” (**a region**), which includes monitoring BER of the “portion,” selecting the ECC scheme for the “portion,” and performing encoding/decoding with the selected ECC scheme for that “portion.” *See, e.g.*, Ex.1005, [0022], [0050], claim 15.

2. Li combined with Cideciyan

While Li describes a set of ECC schemes with **various code types** (Ex.1005, [0019]), Cideciyan provides an example ECC scheme using a well-known “product code” code type, described in detail in textbooks. *See, e.g.*, Ex.1020, 274-278; Ex.1006, FIG. 4 (illustrating a “C1/C2 product code” with component codes C1 and C2), 10:44-49. Cideciyan’s product-code-type ECC scheme is applied on a “group” basis, where the resulting array of encoded symbols (including data

symbols and corresponding parity symbols including C1 and C2 parity symbols) are stored in a single group of pages (**a region**). Ex.1003, ¶66.

Thus, Li combined with Cideciyan teaches: ***such that the region stores at least data payload and primary and secondary ECC parity symbols corresponding to the data payload of the region*** – one of the two claim elements added during prosecution of the '085 patent. Ex.1003, ¶67.

Cideciyan also addresses the other claim element added during prosecution. That is, Cideciyan teaches organizing the pages in groups, where each group includes a fixed number of multiple pages across different channels, **accessible in parallel**. Ex.1006, FIG. 2, 8:52-64, 11:44-46. The array of encoded symbols stored in a single group thus span across the multiple channels. Ex.1006, FIG. 5. A POSITA would understand that pages being parallelly accessible via multiple channels means that the pages can be read simultaneously. Ex.1003, ¶68, citing Ex.1012, 2; Ex.1018, 18; Ex.1007, Abstract, FIGS. 7A-7B, 11:20-64.

Thus, Li combined with Cideciyan teaches: ***wherein the two or more flash memory pages of a region can be read simultaneously*** – one of the two claim elements added during prosecution of the '085 patent. Ex.1003, ¶69.

Multiple reasons to combine Li and Cideciyan are described in more detail in the analysis below. Ex.1003, ¶70.

3. Li further combined with Frost

Frost is also directed at a “flash-based storage system,” and describes in greater detail how data in a particular region accessible in parallel can be read, “**at the same time.**” Ex.1007, Title, 6:46-67. In view of Frost, it would be obvious for Li’s parallel access capabilities to include *wherein the two or more flash memory pages of a region can be read simultaneously.* Ex.1003, ¶71. The reasons to combine Frost with Li and Cideciyan are described in more detail in the analysis below.

4. Li further combined with Leung

Leung is like Li in that it teaches selecting a gear in response to a change in a bit error rate. Leung is used to address some of the implementation details of the dependent claims directed to gear selection. Ex.1003, ¶72. The reasons to combine Frost with Li and Leung are described in more detail in the analysis below.

E. Ground 1: Claims 1-2, 4-5, 14-17, 22-25, and 29-33 are obvious in view of Li and Cideciyan.

1. Claim 1

[1.0] A method of selecting an error correction coding (ECC) scheme, the method comprising:

To the extent the preamble is limiting, Li renders obvious [1.0]. Ex.1003, ¶¶74-75.

Specifically, Li describes “encoding/decoding **in accordance with one or**

more of the ECC schemes, and dynamically switching encoding/decoding
amongst one or more of the ECC schemes based at least in part on information
from the error statistic collecting/tracking.” Ex.1005, Abstract; Ex.1003, ¶75.

[1.1.1] *determining a bit error rate associated with a region comprising a fixed number of two or more flash memory pages or integer fractions thereof, wherein the two or more flash memory pages of a region can be read simultaneously,*

Li combined with Cideciyan renders obvious [1.1.1]. Ex.1003, ¶¶76-99.

a. Li teaches “*determining a bit error rate associated with a region.*”

As shown in FIGS. 1 and 2A below, Li teaches using an error statistics
collecting and tracking hardware logic block to *determine* a raw Bit Error Rate
(BER) associated with a “portion” (*a region*). Ex.1005, [0022], [0097], [0099],
[0038], [0039]; Ex.1003, ¶77; ¶26.

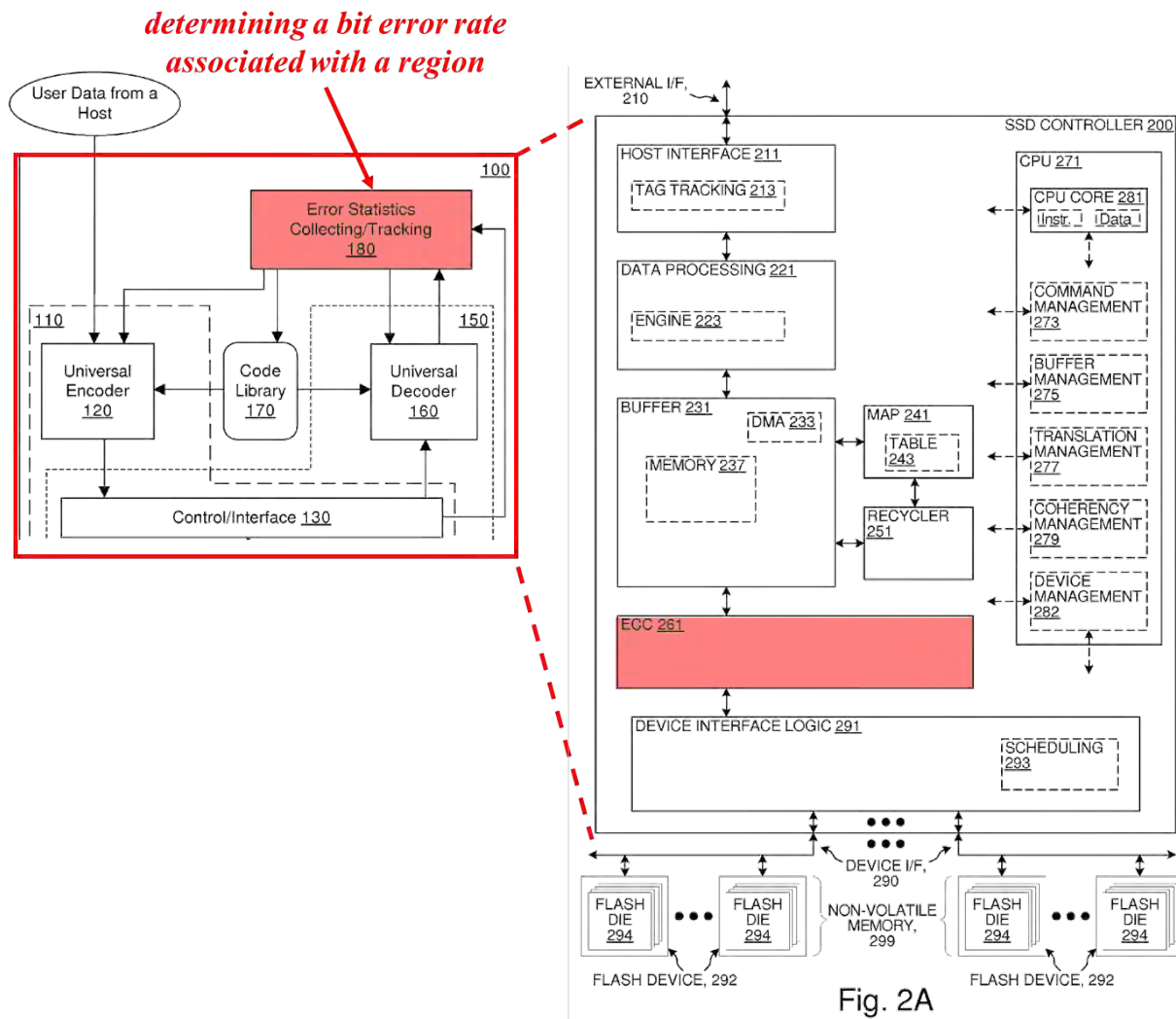


Fig. 2A

Ex.1005, FIGS. 1 (partial) and 2A, annotated.

In more detail, Li describes adaptively selecting an ECC scheme with a correction strength for each “portion” of a plurality “portions” of the memory. In other words, Li’s adaptive ECC scheme selection is performed on the basis of a particular “portion” (*a region*), which includes monitoring BER of the “portion,” selecting the ECC scheme for the “portion,” and performing encoding/decoding with the selected ECC scheme for that “portion” (*“the region”*). See, e.g., Ex.1005,

[0022] (“determine a raw Bit Error Rate (BER) of accesses to **a portion** of a flash memory”); [0047]-[0048], [0050]-[0051]; claim 15; *see also id.* [0042]-[0043]; Ex.1003, ¶78.

b. Li’s “portion” associated with the bit error rate determination comprises a fixed number of multiple pages.

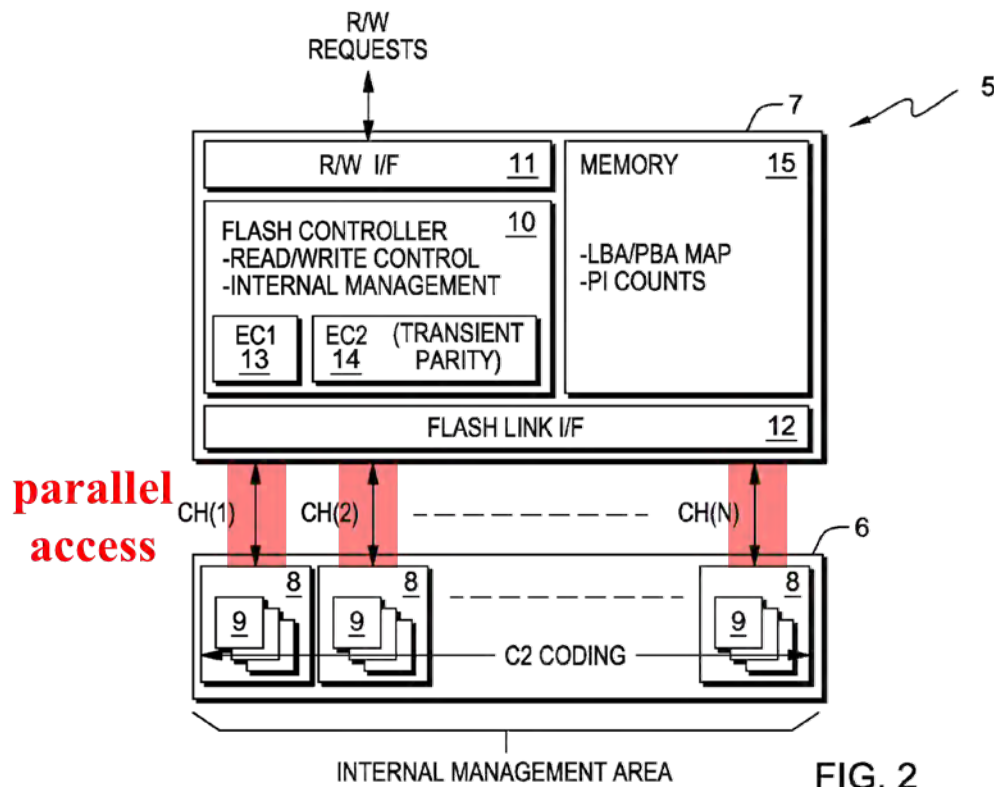
Li describes a “portion” of the flash memory that includes multiple pages, and “each of the portions is enabled to store a **pre-determined** amount of information” (*comprising a fixed number of two or more flash memory pages*). Ex.1005, [0099] (“a flash memory is operated as portions (such as **pages**[] or **multiples** thereof), [0038] (“the portion is one or **more** pages of the flash memory”). Li’s “portion” including a predetermined fixed number of pages, which is fixed by the “predetermined amount of information” of the portion and the predetermined fixed size for each page. *Id.*, [0097] (“each of the portions is enabled to store a **pre-determined** amount of information”). Ex.1003, ¶¶79-80.

c. It would be obvious for Li’s portion including a fixed number of multiple pages to span multiple channels as taught by Cideciyan, thereby supporting simultaneous read for the pages.

First, Li explains that its plurality of flash dies in the flash memory are “**accessible in parallel.**” Ex.1005, Li, [0111], [0112]. Li also describes that its adaptive ECC scheme selection is performed on a “portion” basis, where the portion can be a group of multiple pages. Ex.1005, Li, [0022], [0097], [0099],

[0038], [0039]. Ex.1003, ¶64. As such, in light of the well-known benefits that parallel access improves performance (e.g., reduced latency, increased speed, distributed wear for extending the memory device life span) by allowing simultaneous read/write operations across the busses, Li's flash dies accessible in parallel (Ex.1005, [111]-[112]) at least suggest organizing its portion including a fixed number of multiple pages to span multiple channels for simultaneous read and write and improved performance. Ex.1003, ¶64-81.

Second, as shown in FIG. 2 of Cideciyan below, Cideciyan describes **N channels** (CH(1) through CH(N)) in the SSD, providing **parallel access** to pages of the flash memory chips. Ex.1003, ¶81.

**Ex.1006, FIG. 2, annotated**

In further detail, Cideciyan describes “N logical subdivisions corresponding to respective storage banks 8 on the set of N channels,” which are accessible in parallel. Ex.1006, 10:3-11; 11: 44-46 (pages allocated on different channels “can be written **in parallel** to the N channels”). Ex.1003, ¶81.

Cideciyan teaches “storing input data in **groups**” (Ex.1006, 19:43), and performing ECC encoding, storing the encoded symbols, and ECC decoding in “groups,” each group including pages distributed across the channels. Ex.1006, FIGS. 4 and 5, 4:30-45 (“storing input data in successive **groups**,” “encoding the

input data to be **stored in each group**"). As will be discussed in detail at [1.1.2] below, the array of encoded symbols (including data symbols and parity symbols as illustrated in Ex.1006, FIG. 4) generated using Cideciyan's product-code-type ECC scheme will be written into a single group of pages distributed across the channels. Similarly, Cideciyan's decoding process is performed on data read from each group. Ex.1003, ¶82.

Cideciyan teaches "the **pages of each group** are **distributed across** all [N] **logical subdivisions**." Ex.1006, Abstract; 19:43; 10:9-11. Cideciyan uses the term "stride" to refer to such a group of pages distributed across the channels. *Id.*, 10:11-12. As shown in FIG. 5 below, the example group of pages (a stride) includes "one page in each of the N channels," which is what is more commonly referred to as a "page stripe." Ex.1006, 11:9-18; Ex.1003, ¶¶83, 46. The group of pages ("page stripe") of FIG. 5 is *a region comprising a **fixed** number (N) of multiple pages as claimed*. As shown in FIG. 5, there are at least 4 channels, which teaches *a fixed number of **two or more** flash memory pages*. Ex.1003, ¶83.

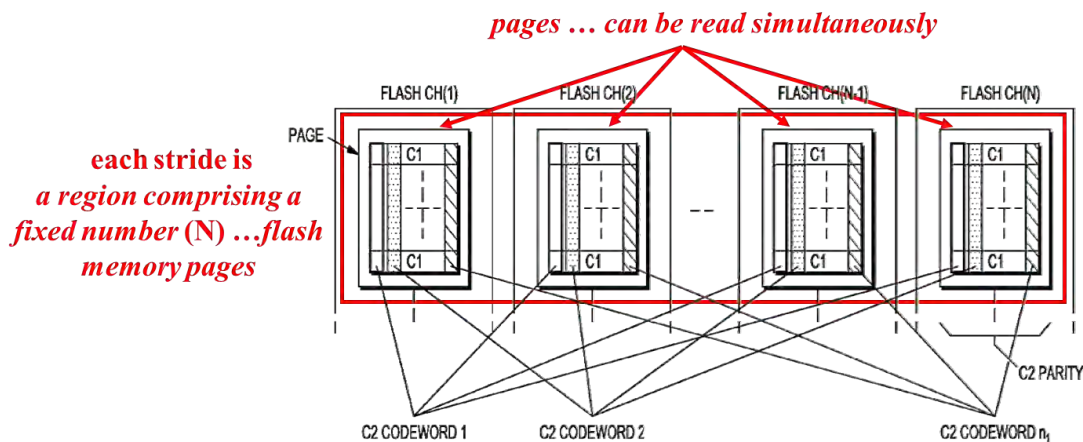


FIG. 5

Ex.1006, FIG. 5, annotated.

Thus, it would be obvious for Li's portion including a fixed number of multiple pages to span multiple channels as taught by Cideciyan, which achieves various benefits of parallel access, and additional benefits of implementing the product-code-type ECC scheme on the group basis as taught by Cideciyan (e.g., "efficient, reliable and robust solid state storage systems with exceptional overall performance" with orthogonal primary and secondary codewords, with "improved error protection offered by the coding process both within storage subdivisions and across the storage as a whole." Ex.1006, 5:2-13), which will be discussed in detail in [1.1.2]. Ex.1003, ¶84.

d. It would be obvious for multiple pages spanning multiple channels to be read simultaneously.

In the group of pages in FIG. 5 of Cideciyan above, each of the N pages can

be accessed in parallel through the N channels, and a POSITA would understand that accessing the pages in parallel includes performing *read* operations *simultaneously* using the N channels. Ex.1012, FIG. 4, 98 (“a **request is served by channel 0 and channel 1 simultaneously**, it exploits the channel-level parallelism.”), FIG. 11, 102; Ex.1018, 18 (“Channels refer to the number of flash chips the controller can talk to **simultaneously**.”). Ex.1003, ¶85.

To the extent that it is argued that parallel access is not necessarily simultaneous, that argument is addressed at Ground 2 below. Ex.1003, ¶86.

e. Reasons to Combine Li and Cideciyan

It would have been obvious to a POSITA to combine Li and Cideciyan to provide the obvious, predictable, and beneficial results obtained from Cideciyan’s memory arrangement and accessibility. Ex.1003, ¶87.

First, the implementation with Cideciyan’s technique of organizing data in “groups,” each group include pages distributed across channels, has the advantage that the fixed number of multiple pages in a group are distributed across the channels of an SSD, utilizing the channel-level parallelism in SSD to gain better parallel performance, which is important for overall SSD performance. Ex.1012, 105 (explaining the well-known channel-level parallelism in SSDs which is important for SSD performance); Ex.1013, 1 (describing various well-known technologies of using flash channels in an SSD for achieving desirable parallel

read and write access). Ex.1003, ¶88. Benefits of parallelism include lower latency, better data protection by spreading data across multiple dies if one die has higher failures. *See, e.g.*, Ex.1006, 5:2-6 (“protection against failures of individual storage subdivisions in the system” by error correcting coding process across the channels); Ex.1007, Frost, 11:57-60 (parallel access through channels allowing “relatively quick read and write operations and allows data to be stored to and retrieved from the memory array 14 in an efficient and effective manner.”). Ex.1003, ¶88.

Second, Cideciyan provides implementation details of the “portions” and the parallel accessibility across a plurality of flash dies described in Li. Therefore, it would be obvious to implement Li’s teaching of organizing the flash memory (including a plurality of flash dies assessable in parallel) in portions, with the organization of the flash memory in groups of pages across channels as taught by Cideciyan. Ex.1003, ¶89.

Li describes organizing the flash memory (including a plurality of dies accessible in parallel), in a plurality of “**portions**” such that each “portion” includes a fixed number of multiple pages. Li describes applying ECC schemes and monitoring the bit error rate of “portions” generally. Ex.1005, Li, [0037]-[0038], [0099]. A POSITA would have found it obvious to look to known techniques for how to implement those portions. Ex.1003, ¶90.

Cideciyan is such a reference. The specific implementation in Cideciyan's FIG. 5 includes storing data in groups, each group including N pages across N channels, with the advantage that each page is accessible in parallel through the N channels, thereby achieving channel-level parallelism among these pages in the group. It was well-known in the art that channel-level parallelism is important for achieving peak performance in SSD. Ex.1012, 2. Ex.1003, ¶91.

Additionally, Cideciyan is a patent application by International Business Machines (IBM) Corporation, which was a top storage provider during the timeframe of the earliest priority date of the '085 patent. A POSITA with Li in hand would have looked to patents and publications like Cideciyan from IBM to improve Li's flash-based SSD. Ex.1003, ¶¶91-95.

Third, as shown in FIG. 2A of Li and FIG. 2 of Cideciyan below, Li and Cideciyan are similar devices with similar objectives. Ex.1005, FIG. 2A (illustrating a flash memory based storage system with SSD controller and flash devices accessible in parallel channels), [0019] (aiming for "improvements in flash memory lifetime, reliability, performance, and/or storage capacity"); Ex.1006, FIG. 2 (illustrating a flash memory based storage system with a flash controller and flash devices accessible in parallel channels), 5:11-13 (to "provide efficient, reliable and robust solid state storage systems with exceptional overall performance"). Ex.1003, ¶96.

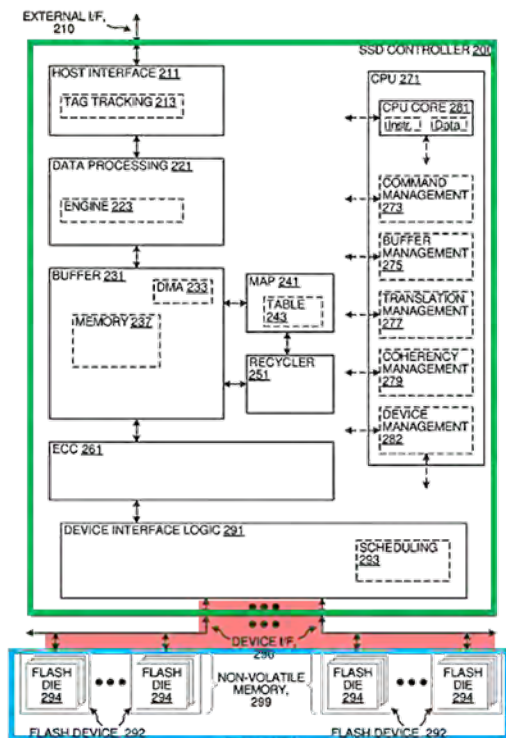


Fig. 2A

Ex.1005, Li, FIG. 2A, annotated

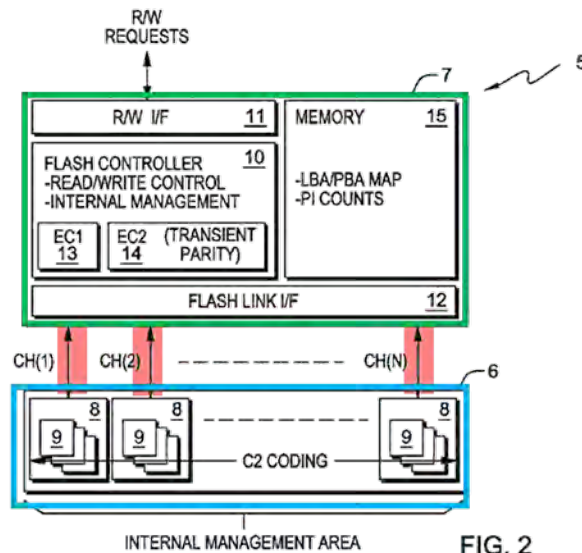


FIG. 2

Ex.1006, Cideciyan, FIG. 2,
annotated

A POSITA would recognize that a known technique (using strides, where each stride including N pages distributed across N channels) has been used to improve one device (the flash-based storage system of Cideciyan), it would improve similar devices (Li's flash memory based storage system) in the same way (with the benefits as taught by Cideciyan), using the prior art elements (using group of pages, where each group including N pages distributed across N channels) according to their established functions. Ex.1003, ¶197; *Intel Corp.*, 61 F.4th at 1380–81.

Fourth, and as will be explained in detail below at [1.1.2], it would have

been obvious to implement Li's ECC technique using the product code type ECC scheme applied on groups of pages as taught by Cideciyan. Using that technique, the "portion" for ECC and the BER monitoring of Li associated with a portion would span multiple channels that are accessible simultaneously and in parallel. Ex.1003, ¶87.

Additionally, the results of the proposed combination would have been predictable and a POSITA would have had a reasonable expectation of success, because the combination of Li and Cideciyan merely applies known technique to a known device (Li's flash memory based storage system implementing adaptive ECC schemes) to yield the predictable results of "efficient, reliable and robust solid state storage systems with exceptional overall performance." Ex.1006, 5:11-13; Ex.1003, ¶98.

As shown in Example 1.1 of Li combined with Cideciyan (based on based on FIGS. 1, 2A of Li and FIG. 5 of Cideciyan) below, a POSITA would have reasonably expected to succeed in combining Li with Cideciyan, because Cideciyan's group-based ECC encoding/decoding is described as applicable to flash memory devices such as those taught by Li. *See, e.g.*, Ex.1006, FIG. 2. Additionally, the implementation of Cideciyan's teaching would have required only routine knowledge well within the skill of a POSITA prior to the earliest effective filing date of the '085 patent. *See, e.g.* Ex.1006, 11:55-57

region

Appx97

[1.1.2] wherein the region stores at least data payload and primary and secondary ECC parity symbols corresponding to the data payload of the region;

Li combined with Cideciyan renders obvious [1.1.2]. Ex.1003, ¶¶100-118.

Li teaches that the “portion” of a flash memory (“*the region*”) as discussed at [1.1.1] stores user data and a number of error correcting bits (“*data payload and ECC parity symbols corresponding to the data payload of the region*”). Ex.1003, ¶101.

For example, claims 1-3 of Li recite:

1. A system, comprising:

means for error statistics collecting and tracking enabled to dynamically determine a raw Bit Error Rate (BER) of accesses to a **portion** of a flash memory; and

means for adaptive encoding enabled to encode according to a dynamically selected one of a plurality of error correcting codes, and further enabled to dynamically determine the dynamically selected error correcting code based at least in part on the raw BER.

2. The system of claim 1, wherein encoding according to a first one of the error correcting codes results in a number of **error correcting bits** to **store in the portion** that is less than when encoding according to a second one of the error correcting codes.

3. The system of claim 2, wherein when encoding according to the first error correcting code, a number of bits of the portion used as user data is increased by up to a difference between the number of error correcting bits used by the second error correcting code minus the number of error correcting bits used by the first error correcting code.

See also Ex.1005, [0021]-[0025], claim 15; [0099] (“each portion is organized as a **data sub-portion** and a respective corresponding **error correcting sub-portion**”); [0060] (“the portion comprises a plurality of sub-portions, and the adaptive encoder is further enabled to encode such that error correcting information is storable to one or more of the sub-portions and data information is storable to only one of the sub-portions”); Ex.1003, ¶101.

It would have been obvious to implement Li’s ECC technique using one of the known, available ECC techniques such as Cideciyan’s product code type ECC scheme. As discussed below, Cideciyan describes implementing a product code ECC scheme on a group basis, where each group spans across the channels, which provides implementation detail of an ECC scheme and associated “portions” that would be obvious to use in Li. Ex.1003, ¶102.

Generation of the primary and secondary ECC parity symbols:

Cideciyan describes **generating** the primary codewords (including primary parity symbols) and secondary codewords (including secondary ECC parity

symbols) using a product code type ECC scheme as shown in FIG. 4. To be clear, FIG. 4 is merely a logical representation of the well-known product code scheme (see, e.g., Ex.1020, FIG. 9.6; Ex.1019, FIG. 5), which illustrates the encoded symbols using the product code (with component codes C1 and C2) **to be stored in a single physical region**. FIG. 4 does not display physical pages of a flash memory. However, FIG. 5 which is discussed in detail below, is a **physical** representation of **a single physical region** (a group of N pages from across N channels (“stride”)) storing the array of encoded symbols of FIG. 4; Ex.1003, ¶103.

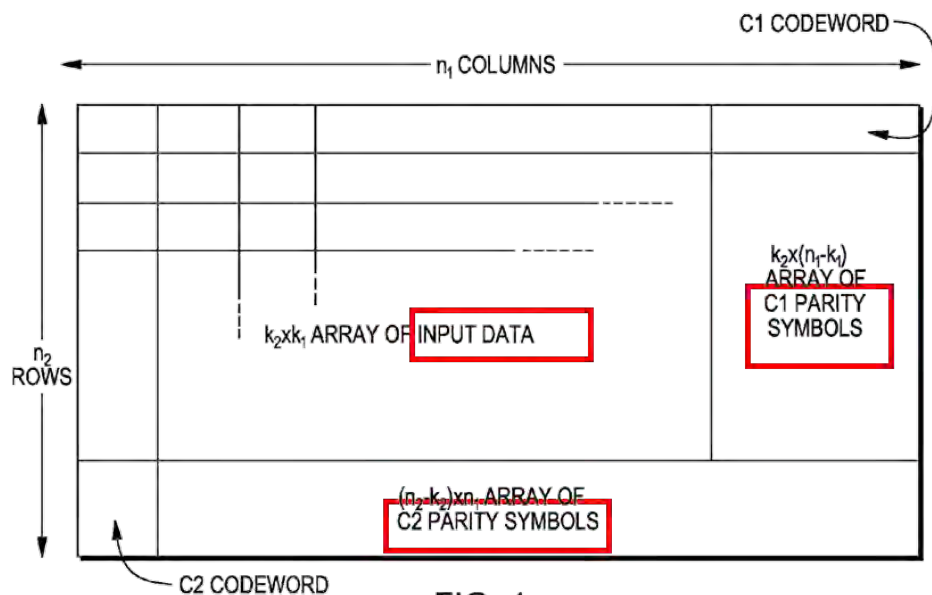


FIG. 4

Ex.1006, FIG. 4, annotated.

Referring to the logical representation of the product code scheme shown in FIG. 4, the encoded symbols of the product code include input data symbols (*data*

payload symbols), C1 parity symbols (*primary ECC parity symbols*), and C1 parity symbols (*secondary ECC parity symbols* generated during the C1 and C2 encoding processes. Ex.1006, 10:53-11:8. “The array of encoded symbols shown in the FIG. 4 is written **in a single stride**”. *Id.*, 11:9-11; Ex.1003, ¶¶35-40, 104.

In further detail, Cideciyan describes “systematic encoding” is used, “whereby each codeword is produced by addition of parity symbols to the unencoded data and the data itself remains unchanged by the encoding process.” Ex.1006, 10:54-56. Ex.1003, ¶105. Cideciyan describes in detail the C1 and C2 encoding process:

The input data to be encoded is partitioned by controller 10 into successive logical blocks each comprising a logical array of k_2 rows and k_1 columns of data symbols.... The EC1 encoder 13 systematically encodes each row in accordance with the C1 code This **C1 parity code** is added to the **k_1 input data symbols** to produce an **n_1 -symbol C1 codeword**. ... the resulting set of k_2 C1 codewords forms a logical array of k_2 by n_1 C1-encoded symbols.... The EC2 encoder 14 systematically encodes each column in accordance with the C2 code to generate **(n_2-k_2) parity symbols** for that column. This **C2 parity code** is added to the **k_2 column symbols** to produce an **n_2 -symbol C2 codeword**.

Ex.1006, 10:53-11:8; Ex.1003, ¶105.

Storage of the primary and secondary ECC parity symbols:

Referring to FIG. 5 below, Cideciyan further describes storing the array of encoded symbols of FIG. 4 in the single group of pages (“stride”). Ex.1006, 11:9-11. Specifically, Cideciyan describes that *the region* (a group of pages including N pages across N channels) storing a long product code codeword (with a codelength n_1n_2), which includes C1 and C2 codewords for component codes C1 and C2. It is noted that in FIG. 5, the C2 parity symbols are stored in the N^{th} page (corresponding to CH(N)) in this group (“stride”) as an example only, and “**any channel could be used for the parity.**” Ex.1006, 11:39-42); Ex.1003, ¶106.

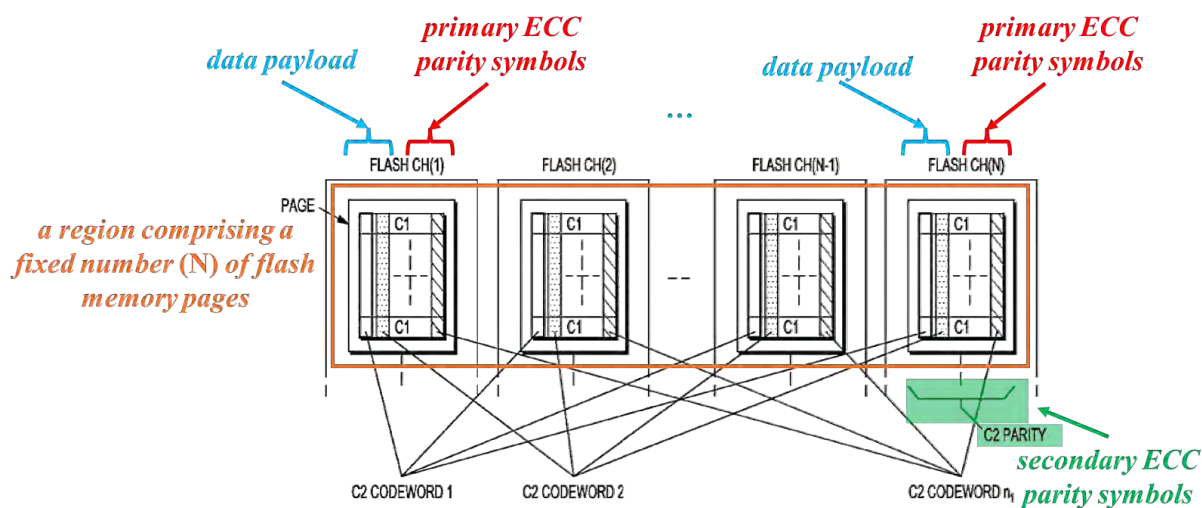


FIG. 5

Ex.1006, FIG. 5, annotated.

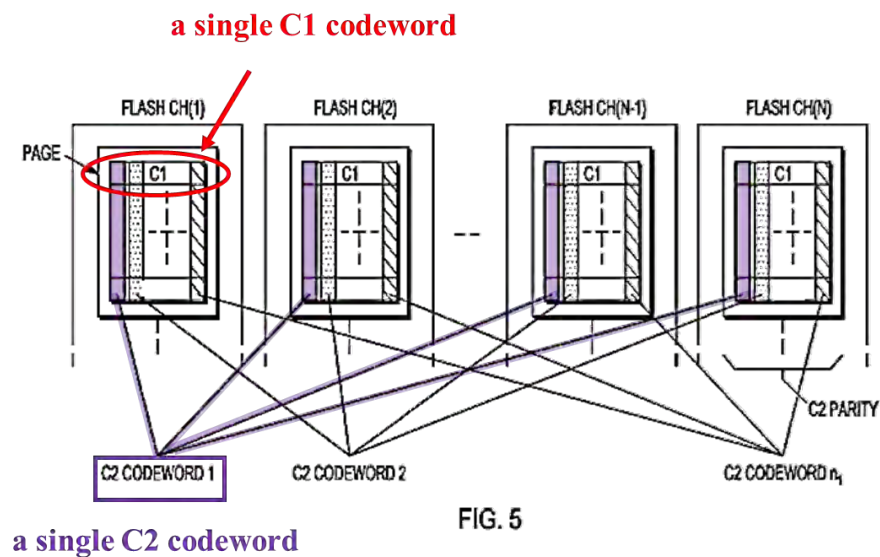
In further detail, referring to FIG. 5 above, Cideciyan describes:

The array of encoded symbols shown in the FIG. 4 is written in **a single**

stride....illustrated by the schematic diagram of FIG. 5....a stride contains one page in each of the N channels and each page stores a plurality of C1 codewords. The key features of the codeword arrangement here are that: (1) **each storage subdivision spanned by the stride contains a plurality of C1 codewords;** and (2) **each of these storage subdivisions contains a portion of each of the second codewords** in the stride. In the stride shown in FIG. 5, different C2 codewords are indicated by differently-shaded vertical bars. The first channel contains the first portion of each of the n_1 C2 codewords. The second channel contains the second portion of each of the C2 codewords, and so on. The last channel, channel N, contains the C2 parity codes for each C2 codeword **in this example**.

Ex.1006, 11:9-28; Ex.1003, ¶107.

In annotated FIG. 5 below, a single C1 (primary) codeword is illustrated in **red**, and a single C2 (secondary) codeword is annotated in **purple**.

**Ex.1006, FIG. 5, annotated.**

Like the '085 patent, Cideciyan's C1 (primary) codewords each are stored within a page and provides protection within a page, and C2 (secondary) codewords each are stored across the group of N pages across the N channels, providing protection within a page stripe, because the example stride of FIG. 5 is a page stripe. Ex.1003, ¶108; Ex.1001, Table 1 (describing "Primary" and "Secondary" and corresponding data protection).

TABLE I

Type of Error Correction	Data Protection
Primary	within a page or integer fraction of a page
Secondary	within a page stripe
Tertiary	within a page grid

Ex.1001, Table 1.

Additionally, like the '085 patent, Cideciyan's C1 (primary) and C2 (secondary) codewords disclosure provides **orthogonal** primary and secondary ECC codewords. Ex.1001, 3:20-25; Ex.1006, FIG. 4, 11:29-31 (“[t]he ‘**orthogonal**’ arrangement of C1 and C2 codewords...**gives exceptional error performance.**”); Ex.1003, ¶109.

Further like the '085 patent, Cideciyan also describes that various code types may be used for C1 code and C2 code. Ex.1006, 18:31-34; Ex.1003, ¶110.

Reasons to Combine Li and Cideciyan

It would have been obvious to a POSITA to combine Li and Cideciyan to provide the obvious, predictable, and beneficial results from implementing the product-code-type ECC scheme as taught by Cideciyan. Ex.1003, ¶111.

First, a POSITA would have been motivated to combine Li with Cideciyan's teaching of using a product code type ECC scheme that provides improved error recovery in Li, because Li describes adaptive ECC selection using “a set of ECC schemes with **various code types.**” Ex.1005, [0019]. Cideciyan teaches an obvious way of implementing Li's ECC schemes, by providing product-code-type-ECC schemes, which use the well-known “product code” code type described in textbooks. Ex.1020, 274-278. “Compared to plain long length codes,” a POSITA would have found that such implementation of applying a product-code-type ECC scheme to the region provides the benefits of “high performance from

cross parity check” with orthogonal arrangement of C1 and C2 codewords, provides “low circuit overhead” by using two shorter length component codes, “improved error recovery,” (Ex.1006, 3:54-4:56), and is a suitable option for Li’s implementation of ECC schemes with various code types. Ex.1018, Yang, 4; Ex.1006, FIG. 4, 11:29-31 (“the ‘orthogonal’ arrangement of C1 and C2 codewords ...gives exceptional error performance”); Ex.1003, ¶¶35-40, ¶112; *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 800 (Fed. Cir. 2021).

Second, implementing Li’s “portion” of multiple pages to span different channels for parallel, simultaneous access provides the additional benefits of “efficient, reliable and robust solid state storage systems with exceptional overall performance,” and “improved error protection offered by the coding process **both within storage subdivisions** and **across the storage as a whole**.” Ex.1006, 5:2-13; *see also* 7:30-41(describing its invention provides “improved error protection... achieved **without the performance penalties**, in terms of increased write amplification and reduced endurance”). Ex.1003, ¶113.

In other words, in the example of Li combined with Cideciyan, improved protection can be achieved across multiple flash memory subdivisions, e.g., using information on other dies to reconstruct information on a failed die, as taught by Cideciyan, which Li alone does not describe. Ex.1003, ¶114.

Third, as shown in FIG. 2A of Li and FIG. 2 of Cideciyan below, Li and

Cideciyan are similar flash-based SSD devices (each including a SSD controller and flash devices accessible in parallel) with similar objectives. Ex.1005, FIG. 2A, [0019], Ex.1006, FIG. 2, 5:12-13; Ex.1003, ¶115.

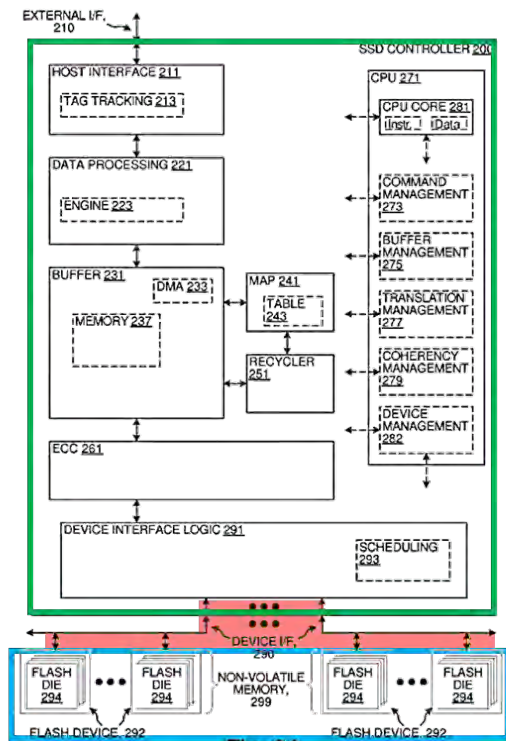


Fig. 2A

Ex.1005, Li, FIG. 2A, annotated

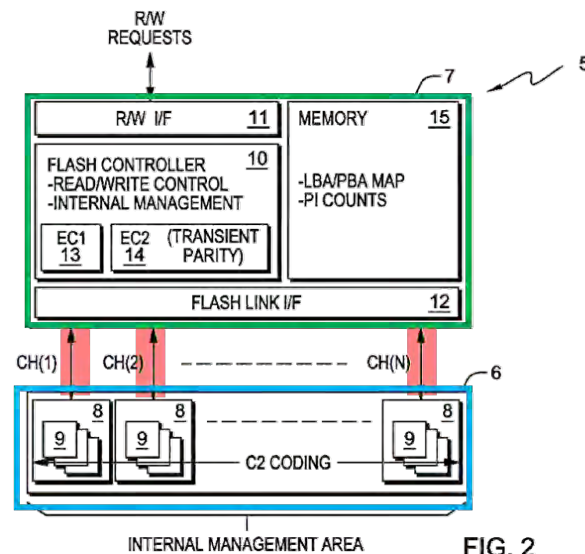


FIG. 2

Ex.1006, Cideciyan, FIG. 2,
annotated

A POSITA would have found it obvious for a known technique (applying a product-code-type ECC scheme to a group of pages across the channels) improves one device (the flash-based storage system of Cideciyan) to improve similar devices (Li's flash-based storage system) in the same way (with the benefits as taught by Cideciyan), using the prior art elements according to their established functions. Ex.1003, ¶116; *Intel Corp.*, 61 F.4th at 1380–81.

Fourth, the combination of Li and Cideciyan allows the pages of the memory to be operated in multi-level cell (MLC) mode for a longer period of time than Li alone, such that the switching from MLC to SLC is delayed or avoided. Li describes that “when a raw BER exceeds a threshold, a portion (such as a page) of flash memory previously operated as an MLC page is thereafter operated as an SLC [single level cell].” Ex.1005, [0103]. Switching from MLC to SLC is at expense of a big reduction of data payload – for example, a reduction around 50% by switching from a 2-bit-level MLC mode to an SLC mode. This switching should be avoided or delayed as much as possible. Ex.1003, ¶117.

By applying Cideciyan’s product code ECC scheme with “exceptional error performance,” (Ex.1006, FIG. 4, 11:29-31), the switch from MLC mode to SLC mode is delayed. *See also* Ex.1006, 3:54-4:4 (“MLC is inherently less reliable than single-level memory cells (SLC)... **Additional coding is therefore required to extend MLC NAND lifetime**”); Ex.1003, ¶117.

Additionally, the results of the proposed combination would have been predictable and a POSITA would have had a reasonable expectation of success, because the combination of Li and Cideciyan merely applies known technique to a known device (Li’s flash memory based storage system implementing adaptive ECC schemes) to yield the predictable results of “efficient, reliable and robust solid state storage systems with exceptional overall performance.” Ex.1006, 5:11-

13; Ex.1003, ¶118.

[1.2.1] comparing the determined bit error rate to one or more predetermined thresholds corresponding to a set of predefined gears comprising at least a first gear and a second gear, wherein the predefined gears correspond to different predefined ECC schemes,

Li, as combined above with Cideciyan, renders obvious [1.2.1]. Ex.1003,

¶¶119-135. A “gear” is:

a set of parameter(s) specifying an error correction coding [ECC] scheme, including one or more of the payload capacity, the type and parameters of each component code, the interleaving scheme, **and parameters** used for determining whether the gear is appropriate for a particular situation.

Ex.1001, 20:18-25

a. Li teaches “a set of predefined gears... the predefined gears correspond to different predefined ECC schemes”

First, Li teaches “a set of predefined gears,” and each predefined gear corresponds to a predefined ECC scheme. Specifically, Li describes multiple sets of parameters (*predefined gears*):

The techniques include a set of ECC schemes with **various code types, code rates, and/or various code lengths (providing different error correcting capabilities)**, and error statistic collecting/tracking (such as via a dedicated hardware logic block).

Ex.1005, [0019]; Ex.1003, ¶121. Each set of parameters in Li (including but not

limited to “code type,” “code rate,” “code length”) is a “*gear*” specifying an ECC scheme providing a corresponding error correcting capability (ECC capability/strength). *See* similarly 085 patent equating a “*gear*” with “ECC strength.” Ex.1001, 51:1-2; *see also* Li’s teaching of BER thresholds at [1.2.1].b below. Li’s above multiple sets of parameters are ***predefined***, and specify ***predefined ECC schemes*** with corresponding ECC strengths. Ex.1003, ¶122, Ex.1005, [0091].

In Li combined with Cideciyan, as discussed at [1.1.2], it would be obvious for a predefined set of parameters specifying an ECC scheme to include a product-code-type ECC scheme as taught by Cideciyan. Each product-code-type ECC scheme is specified with a set of parameters specifying a code type of “product code,” component code C1 (with corresponding parameters), component code C2 (with corresponding parameters), a code rate, and a code length. Ex.1003, ¶¶35-40; *see also* Ex.1020, xv, 274-278; Ex.1019, 4. The set of parameters specifying a product-code-type ECC scheme, together with parameters (including the corresponding BER thresholds) used for determining whether this set of parameters (with the specified ECC scheme) is appropriate for a particular situation (as discussed below at [1.2.1.b]), is a “*gear*” corresponding to that ECC scheme. Ex.1003, ¶124.

Dr. Dolecek has provided a table including examples “*gears*” in “*a set of*

predefined gears” in Li combined with Cideciyan. Ex.1003, ¶125; Ex.1005, Abstract, [0019], [0091], [0035], [0036]; Ex.1006, Cideciyan, 18:31-34, FIG. 11, 16:34-60, FIG. 12, 16:61-17:12; Ex.1009, 5; Ex.1003, ¶¶32-34 and 35-40.

<i>parameters specifying an ECC scheme</i>		<i>ECC scheme</i>	<i>parameters used for determining whether the gear is appropriate</i>
Set 1 (Example Gear 1)	code type: Product Code with c1:BCH, c2: Hamming code; code-rate-1; code-length-1; component-code-c1: c1-code-rate-1, c1-code-length-1; component-code-c2: c2- code-rate-1; c2-code-length-1; etc.	ECC scheme 1	BER-threshold- x1 < Determined BER < BER- threshold-y1
Set 2 (Example Gear 2)	code type: Product Code with c1:BCH, c2:RS; code-rate-2; code-length-2; component-code-c1; c1-code-rate-2; c1-code-length-2; component-code-c2: c2-code-rate-2; c2-code-length-2; etc.	ECC scheme 2	BER-threshold- x2 < Determined BER < BER- threshold-y2

Ex.1003, Table 1.

As shown in Table 1, in Li combined with Cideciyan, *set of predefined gears comprising at least a first gear and a second gear* includes at least “*a first gear*” and “*a second gear*”, each corresponding to a predefined set of parameters specifying an ECC scheme and parameters for determining whether the gear is

appropriate for a particular situation. Ex.1003, ¶¶126-128; *see also* Ex.1005, Claims 1-2.

b. “comparing the determined bit error rate to one or more predetermined thresholds corresponding to a set of predefined gears”

Li teaches the “*comparing*” as claimed, because Li teaches comparing the determined raw BER to “*one or more predetermined thresholds*” (including “a first threshold,” “a second threshold,” and “a third threshold”), where the comparison results are used to select a gear having a corresponding ECC scheme. Ex.1005, [0105]. The one or more thresholds are parameters used for determining whether the gear is appropriate for a particular situation, and are included in the “*gear*” for that corresponding ECC scheme, as construed. Ex.1003, ¶129.

Namely, as an example, Li teaches

while a raw BER of a page of a flash memory is less than **a first threshold**, the page is operated as an MLC page and encoded with **a first short code length ECC**. If/when the raw BER **exceeds the first threshold (but remains less than a second threshold)**, then the page is encoded with a **first longer code length ECC** (while still operated as an MLC page).

If/when the raw BER exceeds **the second threshold (but remains less than a third threshold)**, then the page is encoded with **an even longer code length ECC**.

Ex.1005, [0105]; Ex.1003, ¶130.

A POSITA would have understood that “a first short code length ECC,” “a first longer code length ECC,” “an even longer code length ECC” corresponding to different ECC schemes, each ECC scheme is specified by a set of parameters of a “*gear*,” including parameters of code type and code rate, in addition to the parameter of the code length. Ex.1003, ¶131.

Further, a POSITA would have understood that Li’s teaching of comparing and then selecting a gear corresponding an ECC scheme based on the comparison as described in [0105] applies to gears for various ECC schemes having various code types, code rates, and code lengths, and is not limited to only “a first short code length ECC,” “a first longer code length ECC,” “an even longer code length ECC” as described in [0105] of Li. Ex.1003, ¶132.

c. Li’s thresholds relate to “*gears*”.

Li’s thresholds relate to the “*gears*” corresponding to ECC schemes. The thresholds used for determining whether the particular ECC scheme with corresponding correction capability is appropriate for a particular situation, together with the parameters (including e.g., code type, code rate, code length) for specifying the particular ECC scheme, collectively define a “*gear*”. Ex.1003, ¶133.

In other words, Li’s set of ECC schemes (“*different predefined ECC schemes*”) providing different error correcting capabilities correspond to “*a set of*

predefined gears” (each gear includes a plurality of parameters specifying an ECC scheme and parameters including the one or more thresholds to determine whether the gear is appropriate for the situation). Ex.1005, [0019]. Ex.1003, ¶134.

According, as discussed at [1.2.1].a-c, Li as combined with Cideciyan renders obvious [1.2.1]. Ex.1003, ¶135.

[1.2.2] wherein the first gear has a different data payload size and correction capability than the second gear, wherein the amount of memory space allocated for the storage of data payload within the region varies between the first gear and the second gear to accommodate a varying number of parity symbols between the first gear and the second gear, and

Li, as combined above with Cideciyan, renders obvious [1.2.2]. Ex.1003, ¶¶136-144.

First, as discussed at [1.2.1].a and shown in Table 1 provided by Dr. Dolecek below, Li as combined with Cideciyan renders obvious “***first gear***” and “***second gear***,” which are selected based on different raw BERs, and as such, have different correction capabilities corresponding to the different raw BERs. Ex.1003, ¶¶125, 137.

<i>parameters specifying an ECC scheme</i>		<i>ECC scheme</i>	<i>parameters used for determining whether the gear is appropriate</i>
Set 1 (Example Gear 1)	code type: Product Code with c1:BCH, c2: Hamming code; code-rate-1; code-length-1;	ECC scheme 1	BER-threshold- x1 < Determined BER < BER- threshold-y1

	component-code-c1: c1-code-rate-1, c1-code-length-1; component-code-c2: c2-code-rate-1; c2-code-length-1; etc.		
Set 2 (Example Gear 2)	code type: Product Code with c1:BCH, c2:RS; code-rate-2; code-length-2; component-code-c1; c1-code-rate-2; c1-code-length-2; component-code-c2: c2-code-rate-2; c2-code-length-2; etc.	ECC scheme 2	BER-threshold- x2 < Determined BER < BER- threshold-y2

Ex.1003, Table 1

Second, Li describes different gears having different data payload sizes and correction capabilities, and different number of parity symbols. Ex.1003, ¶138. As an example, Li describes:

2. The system of claim 1, wherein encoding according to a **first** one of the error correcting codes results in a number of **error correcting bits** to **store in the portion** that is **less than** when encoding according to a **second** one of the error correcting codes.

Ex.1005, claim 2; Ex.1003, ¶138. A POSITA would have understood that Li's teaching of gears as described in claims 1-4 applies to various gears corresponding to various ECC schemes having various code types, code rates, and code lengths, including Example Gear 1 and Example Gear 2 in Ex.1003, Table 1.

Li as combined with Cideciyan teaches “*a varying number of parity symbols between the first gear and the second gear*,” because Li describes a number of error correcting bits (“*number of parity symbols*”) according to a first gear corresponding to a first ECC scheme (e.g., specified by a set of parameters including a first ECC code of Example Gear 1 and other parameters) is less than (“*varies*”) when encoding according to a second gear corresponding to a second ECC scheme (e.g., specified by a set of parameters including a second ECC code of Example Gear 2 and other parameters). Ex.1003, ¶139.

Third, Li as combined with Cideciyan renders obvious that “the amount of memory space allocated for the storage of data payload within the region varies between the first gear and the second gear to accommodate a varying number of parity symbols” as claimed. Specifically, Li provides,

3. The system of claim 2, wherein when encoding according to the first error correcting code, a number of bits of the portion used as user data is increased by up to a difference between the number of error correcting bits used by the **second** error correcting code **minus** the number of error correcting bits used by the **first** error correcting code.

4. The system of claim 2, wherein when encoding according to the second error correcting code, a number of bits of the portion used as user data is decreased by up to a difference between the number of

error correcting bits used by the second error correcting code minus the number of error correcting bits used by the first error correcting code.

Ex.1005, claims 3-4; Ex.1003, ¶140.

As described in claims 3 and 4 of Li, in the combination of Li and Cideciyan, “***the first gear has a different data payload size,***” because a number of bits of the portion used as user data (“*data payload size*”) of the first ECC scheme (corresponding to “***first gear***”, e.g., Example Gear 1) is greater than number of bits of the portion used as user data of the second ECC scheme (“***second gear***”, e.g., Example Gear 2). Ex.1003, ¶141.

Further, as described in claims 3 and 4 of Li, Li teaches that in the “portion” of the flash memory, the number of bits of the portion used as user data between the first ECC scheme and the second ECC scheme changes (“increased by up to a difference” or “decreased by up to a difference”) based on the difference of error correcting bits in the region. As such, Li as combined with Cideciyan renders obvious “*the amount of memory space allocated for the storage of data payload within the region varies between the first gear and the second gear to accommodate a varying number of parity symbols.*” Ex.1003, ¶142.

In other words, Li as combined with Cideciyan applies adaptive ECC scheme selection to a portion (a group of pages across the channel) of the flash memory, and the portion has a fixed size. See discussion at Ground 1:[1.1.1]. In

this portion with a fixed size, when dynamically switching between gears (corresponding to different ECC schemes with respective ECC strength), the number of parity symbols (error correcting bits) varies (e.g., increases/decreases) between the gears, and the storage for the data payload changes (decreases/increases according to the difference of number of parity symbols) to accommodate the varying number parity symbols. Ex.1003, ¶143.

This is also consistent with the well-known knowledge in the art. *See e.g.*, Ex.1008, Table 1 (illustrating that gear 2 reduces data payload size to accommodate increased parity size). Ex.1003, ¶144.

[1.3] selecting a gear from the set for the region based at least partly on the comparisons to the one or more predetermined thresholds;

Li, as combined above with Cideciyan, renders obvious [1.3]. Ex.1003, ¶¶145-148, VIII.A.

First, as discussed at [1.2.1].b, Li as combined with Cideciyan describes *comparing the determined bit error rate to one or more predetermined thresholds* for adaptive ECC scheme selection. Ex.1003, ¶146.

Second, as discussed at [1.2.1].b, Li as combined with Cideciyan describes that SSD controller 200 (e.g., implementing an adaptive encoder hardware block) is used for *selecting a gear from the set* (selecting from the set of predefined gears as discussed at [1.2.1]) *for the region* (the group including N pages distributed

across N channels) *based at least partly on the comparisons to the one or more predetermined thresholds*. Ex.1005, [0105], [0023] (“**an adaptive encoder hardware block** ... enabled to dynamically **determine** the selected error correcting code **based at least in part on the raw BER.**”); [0105]; *see also* Ex.1005, Claim 1 (“**dynamically determine** the dynamically selected error correcting code based at least in part on the raw BER”); Ex.1003, ¶147.

It is noted that a POSITA would have understood that Li’s teaching of comparing and then selecting an ECC scheme based on the comparison as described in [0105] applies to various ECC schemes having various code types, code rates, and code lengths, and is not limited to only “a first short code length ECC,” “a first longer code length ECC,” “an even longer code length ECC” as described in [0105] of Li. Ex.1003, ¶148.

[1.4] wherein determining, comparing, and selecting are performed by an integrated circuit,

Li, as combined above with Cideciyan, renders obvious [1.4]. Ex.1003, ¶¶149-151.

As discussed at [1.1.1], [1.2.1], and [1.3], Li as combined with Cideciyan describes an SSD controller for performing *determining, comparing, and selecting*. Li further describes that the SSD controller is implemented on an integrated circuit. Ex.1005, [0125], [0014] (“all [] of an SSD controller (or a computing-host flash

memory controller) are implemented **on a single IC [Integrated Circuit]**, a single die of a multi-die IC.” See also Ex.1007, Frost, 5:4-7 (“The FLASH controller 10 may take many forms. In the example of FIG. 1, the FLASH controller 10 is a **field programmable gate array (FPGA)** that, during start-up of the system is programmed and configured by the CPU 15.”). It was well-known that an FPGA is an integrated circuit; Ex.1003, ¶150 (explaining that it was well-known that an FPGA is an integrated circuit).

This is consistent with the description of the ’085 patent. Ex.1001, 56:56-59 (“the SSD controller 1300 is implemented in an integrated circuit, such as by an application specific integrated circuit (ASIC), a field programmable gate array (FPGA).”); Ex.1003, ¶151.

2. Claim 2

[2.0] The method of claim 1, further comprising repeatedly determining the bit error rate and comparing the determined bit error rate to one or more predetermined thresholds such that the bit error rate is actively monitored.

Li combined with Cideciyan renders obvious [2.0]. Ex.1003, ¶¶152-153.

Specifically, Li teaches repeatedly determining (periodically determining) the bit error rate and comparing it to the thresholds based on the number of program/erase cycles, *such that the bit error rate is actively monitored* (for adaptively selecting the suitable ECC scheme throughout the lifetime of the flash memory). Ex.1005, [0092] (“the Error Statistics Collecting/Tracking hardware

block is enabled to **periodically** determine (such as **once every 100 PE cycles**) a current raw (measured) BER of one or more portions of flash storage.”), [0048] (“wherein the measured raw BER is determined periodically”), [0019] (“**dynamically switching** encoding/decoding of all or any portions of the flash memory amongst a respective one or more of the ECC schemes based at least in part on information from the error statistic collecting/tracking”); Ex.1003, ¶153.

3. Claim 4

[4.0] The method of claim 1, wherein determining, comparing, and selecting are performed in connection with at least one of flash initialization, read, or write operations for an end user.

Li combined with Cideciyan renders obvious [4.0]. Ex.1003, ¶¶154-158.

As illustrated in FIGS. 1 and 2A below, Li describes determining, comparing, and *selecting* (as discussed at [1.1.1], [1.2.1], and [1.3]) *are performed in connection with* (based on parameters related to) *at least one of flash initialization, read* (a number of errors corrected, a number of errors detected, a number of read cycles, a read time), *or write operations* (a number of program/erase cycles, a program time, an erase time) *for an end user* (including read and write operations for an end user received through host interface 211). Ex.1005, [0114] (“**Host interface 211 sends and receives commands and/or data via external interface 210....** the commands include a **read command** specifying an address (such as an LBA) and an amount of data (such as a number

of LBA quanta, e.g. sectors) to read; **in response the SSD provides read status and/or read data**. For another example, the commands include a write command specifying an address (such as an LBA) and an amount of data (such as a number of LBA quanta, e.g. sectors) to write; in response the SSD provides write status and/or requests write data and optionally subsequently provides write status.”). Ex.1003, ¶155.

As further detail, Li describes a write-storage-data path and a read-storage-data path. Ex.1005, [0088] (“A **write-storage-data path 110** includes various hardware blocks:....A **read-storage-data path 150** includes various hardware blocks:... An **Error Statistics Collecting/Tracking 180** hardware block is coupled to the Universal Encoder, the Code Library, the Universal Decoder, and the Control/Interface hardware blocks”). Ex.1003, ¶156.

A POSITA would have understood that in Li, the parameters “a number of errors corrected, a number of errors detected,...a number of read cycles..., a read time” are related to (*in connection with*) *read operations for an end user*, and parameters “a number of program/erase cycles,...a program time, an erase time” are related to (*in connection*) *with write operations for an end user*. Ex.1005, Claim 16. Ex.1003, ¶157.

determining, comparing, and selecting are performed in connection with at least one of flash initialization, read, or write operations for an end user

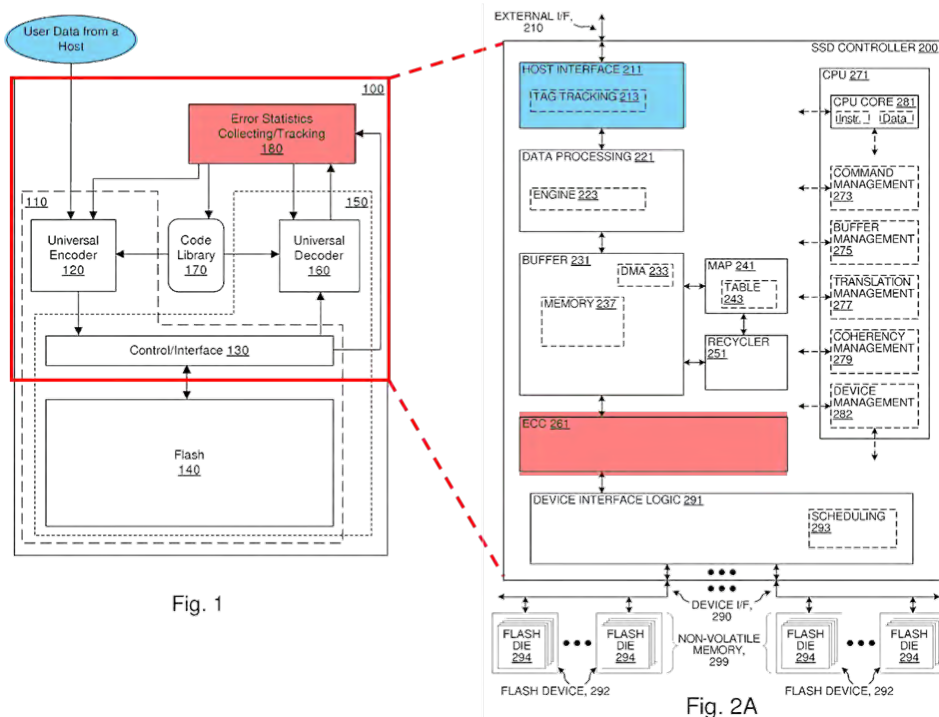


Fig. 1

Fig. 2A

Ex.1005, FIGS. 1 and 2A, annotated.

Li provides additional description on how the determining, comparing, and selecting are performed in connection with at least one of flash initialization, read, or write operations **for an end user**, because they are performed based on parameters related to read/write operations commanded by the host for an end user. Ex.1005, FIG. 1 (illustrating “**user data** from a host,” which is from an end user), [0089] (describing write operation from an end user, where ““User Data **from a Host**’ to write as storage data is received by the Universal Encoder and encoded according to an error correcting code”); [0090] (describing read operations from an

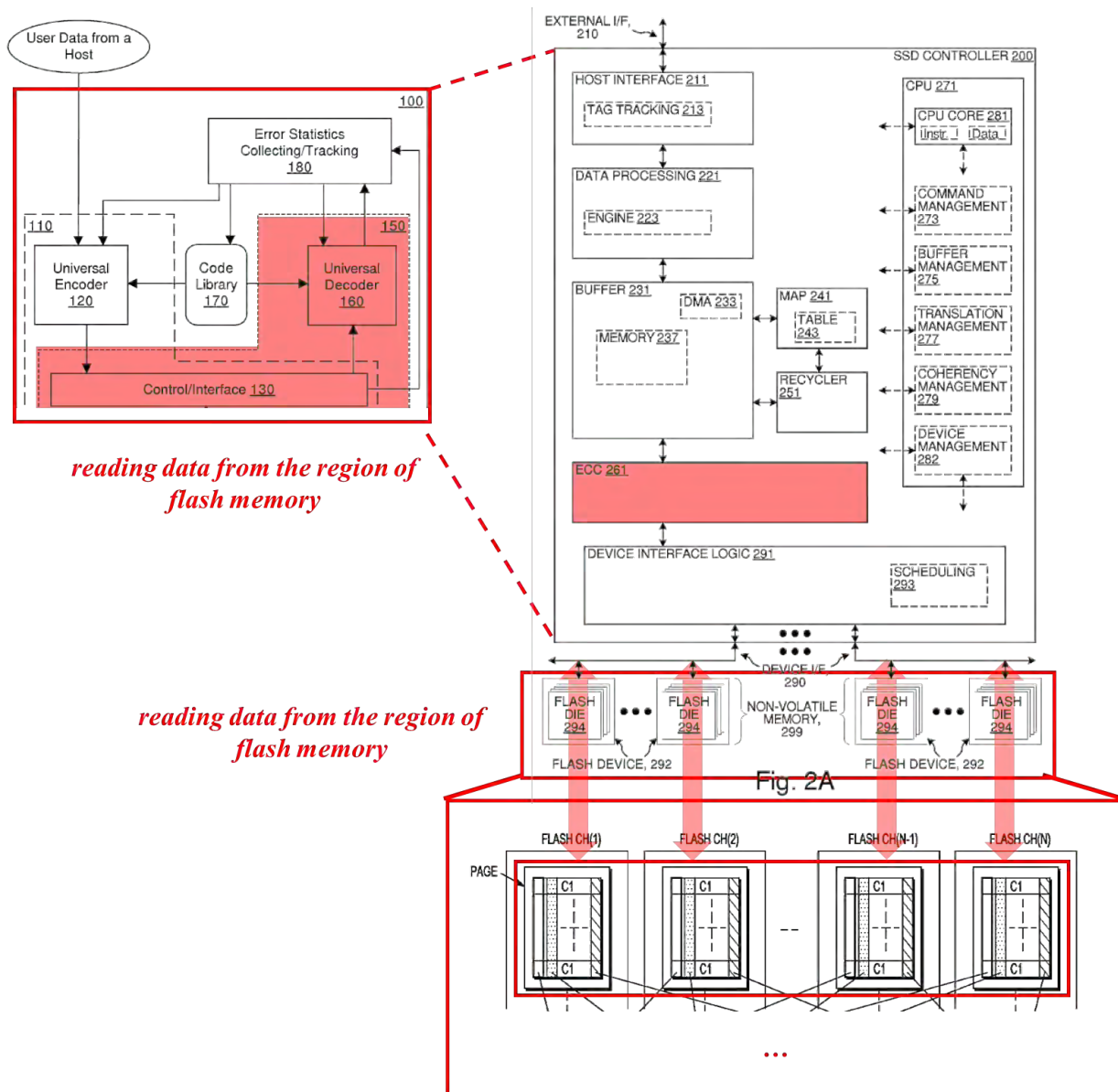
end user, where “[r]eading storage data begins by Control/Interface reading raw information,” and the decoded “data information is then **passed to the Host.**”); Ex.1005, [0023] (“**an adaptive encoder hardware block** enabled to encode according to a selected one of a plurality of error correcting codes, and further enabled to dynamically **determine the selected error correcting code** based at least in part on the raw BER.”). Ex.1003, ¶158.

4. Claim 5

[5.0] *The method of claim 1, further comprising reading data from the region of flash memory,*

Li combined with Cideciyan renders obvious [5.0]. Ex.1003, ¶¶159-160.

As shown in Example 1.1 of Li combined with Cideciyan below, Li as combined with Cideciyan describes “*reading data*” (e.g., using SSD controller 200 including elements implementing the read-storage-data path) “*from the region of flash memory*” (from a portion/a group of pages across channels of the flash-based SSD). Ex.1005, [0050] (“observing a BER associated with at least some **reads of the portion**”); [0088]. Ex.1003, ¶160.



Example 1.1 of Li Combined with Cideciyan.

[5.1] wherein determining the bit error rate further comprises estimating the bit error rate based at least partly on a number of errors corrected by ECC in connection with reading the data from the region.

Li combined with Cideciyan renders obvious [5.1]. Ex.1003, ¶¶161-162.

Li as combined with Cideciyan describes *determining the bit error rate*

*further comprises includes estimating (using SSD controller 200 including elements implementing Error Statistics Collecting/Tracking 180) the bit error rate based at least partly on a number of errors corrected by ECC (by comparing raw read data from the flash memory with an error-corrected version of the raw read data) in connection with reading the data from the region (associated with the reads of the portion). Ex.1005, [0050] (“the measured raw BER is determined at least in part by observing a BER associated with at least some **reads of the portion**”); [0051] (“measured raw BER is determined at least in part by comparing raw read data from the flash memory with an error-corrected version of the raw read data.”); see also Ex.1005, [0079] (describing that an ECC scheme and/or its parameter base on “a number of errors corrected.”). Ex.1003, ¶162.*

5. Claim 14

[14.0] *The method of claim 1, wherein the gear includes a lower-latency ECC decode option and one or more higher-latency ECC decode options,*

[14.1] *wherein the gear is selected such that performing ECC decoding using the lower-latency ECC decode option alone is sufficient to provide corrected data at least 90% of the time.*

Li combined with Cideciyan renders obvious [14.0]-[14.1]. Ex.1003, ¶¶163-170.

Li describes “decoding in accordance with one or more of the ECC schemes.” Ex.1005, Abstract. It would be obvious to implement in Li, well-known

examples of providing decode options with different latencies for a single ECC scheme, as taught by Cideciyan. Ex.1003, ¶164.

First, Cideciyan provides *a lower-latency ECC decode option* (C1 decode option) *and one or more higher-latency ECC decode option* (the decode option of using both C1 and C2 decoding), where the decode option of using both C1 and C2 decoding inherently has a higher-latency because the system first incurs the latency of C1 decoding. Ex.1006, 14:29-33 (the failed “**C1 erasures can then be corrected** by the C2 decoder”); 14:41-50 (“Whenever a strip contains page or block errors that **cannot be corrected by the C1 error correction process**,” it is reconstructed “via the **C2 decoding** algorithm.”). Ex.1003, ¶165.

Second and alternatively, Cideciyan describes C1 decode option and C2 decode option having different latencies. Ex.1006, 18:21-25, 14:29-33, 14:41-50. Ex.1003, ¶¶166-167 (Dr. Dolecek explaining that it was well-known to provide different coding options having different latencies, citing Ex.1010, 14:1- 5; Ex.1011, 11:5-8); Ex.1003, ¶168.

Third, [14.1] is prima facie obvious, because the specification of the ’085 patent does not show any unexpected result or other unexpectedly improved properties. See Ex.1001, 23: 40-46; Ex.1003, ¶169. A long-held rule is that a percentage amount is prima facie obvious without a showing of some unexpected result or other unexpectedly improved properties. See *In re Dillon*, 919 F.2d 688,

692 (Fed. Cir. 1990) (en banc); *see also*, *In re Aller*, 220 F.2d 454, 456 (CCPA 1955); *In re Scherl*, 156 F.2d 72, 74-75 (CCPA 1946).

Regardless, a POSITA would have found it obvious to select a gear based on the determined BER, such that *performing ECC decoding using the lower-latency ECC decode option alone is sufficient to provide corrected data at least 90% of the time*. Ex.1006, FIG. 11, 4:1-4; 16:25-40; Ex.1009, JESD218, 11; Ex.1003, ¶170.

6. Claim 15

[15.0] *An apparatus comprising:*

To the extent that the preamble is limiting, Li as combined with Cideciyan renders obvious [15.0]. Specifically, Li describes that its invention “may be implemented in ...an **apparatus**.” Ex.1005, [0007]. Further, as discussed below at [15.1.1] and [15.3], Li describes that the apparatus includes the claimed first circuit and second circuit. Ex.1003, ¶¶171-172.

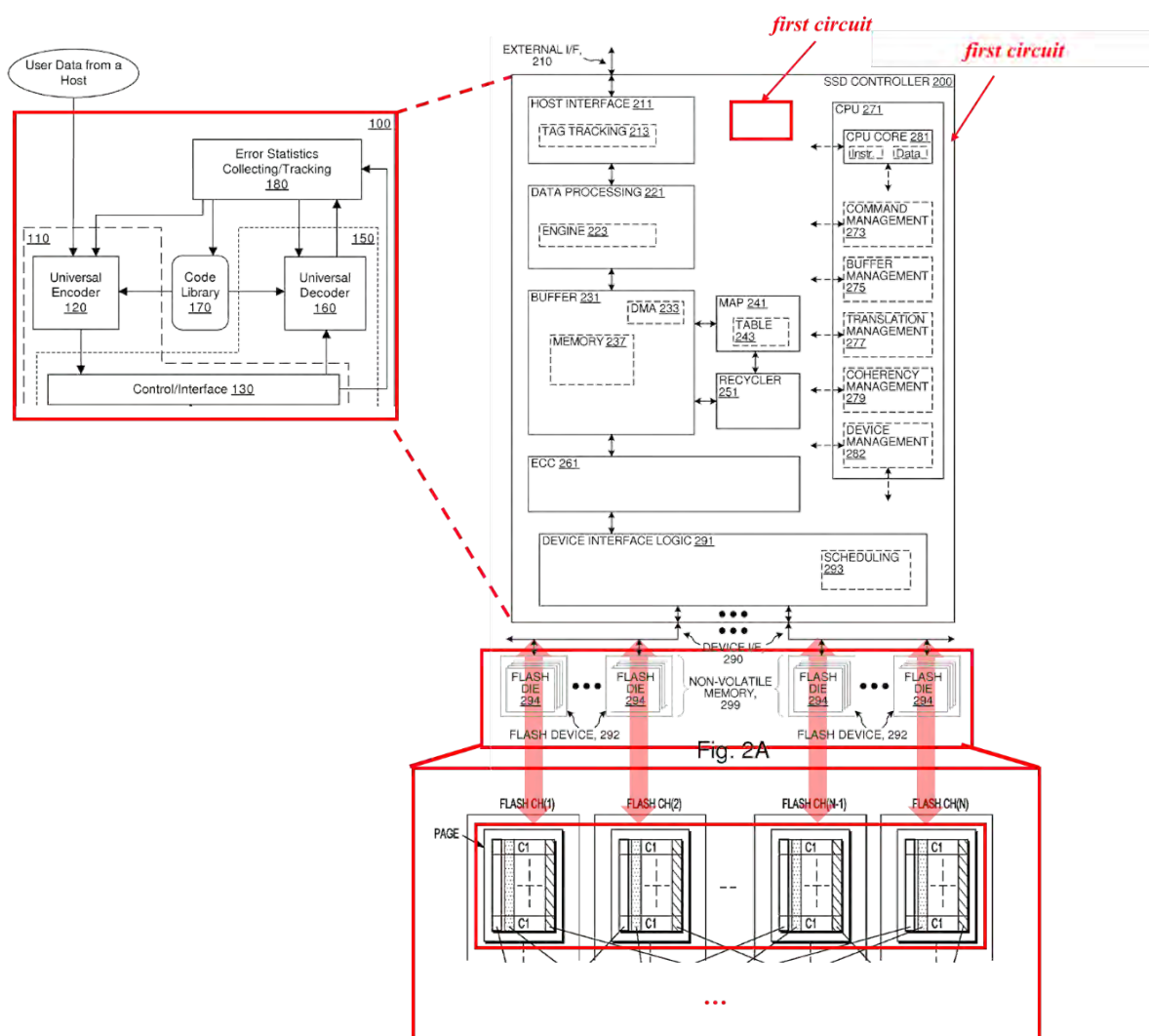
[15.1.1] a first circuit configured to determine a bit error rate associated with a region comprising a fixed number of two or more flash memory pages or integer fractions thereof, wherein the two or more flash memory pages of a region can be read simultaneously,

Li combined with Cideciyan renders obvious [15.1.1]. Ex.1003, Ex.1003, ¶¶173-174.

As discussed at [1.2.1] and shown in Example 1.1, the combination of Li and Cideciyan renders obvious *a first circuit* (e.g., using SSD controller 200 and/or

elements thereof implementing the read-storage-data path, including the Code Library, Error Statistics Collecting/Tracking 180, Universal Decoder 160) configured to determine a bit error rate associated with a region comprising a fixed number of two or more flash memory pages or integer fractions thereof.

Ex.1005, [0126]; Ex.1003, ¶174.



Example 1.1 of Combination of Li and Cideciyan

[15.1.2] wherein the region stores at least data payload and primary and secondary ECC parity symbols corresponding to the data payload of the region and

Li combined with Cideciyan renders obvious [15.1.2] for reasons discussed at [1.1.2]. Ex.1003, ¶175.

[15.2.1] [the first circuit] configured to compare the determined bit error rate to one or more predetermined thresholds corresponding to a set of predefined gears comprising at least a first gear and a second gear, wherein the predefined gears correspond to different error correction coding (ECC) schemes,

Li combined with Cideciyan renders obvious [15.2.1], because *the first circuit* (SSD controller 200 including elements implementing Error Statistics Collecting/Tracking 180, e.g., using ECC 261 or any other suitable elements of SSD controller 200 as well-known in the art) performs the comparing for reasons discussed at [1.2.1] and [1.2.2]. Ex.1003, ¶176.

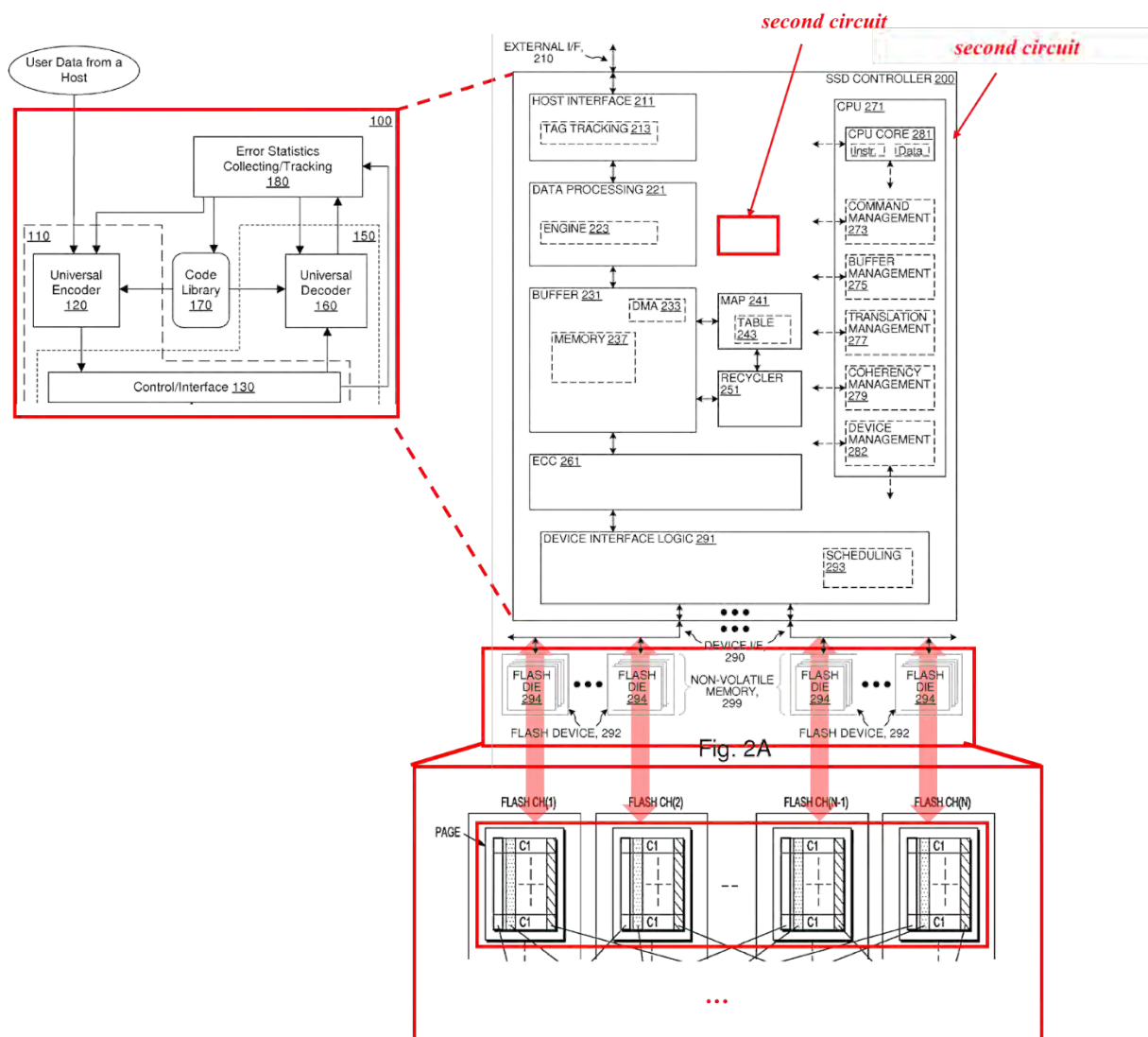
[15.2.2] wherein the first gear has a different data payload size and correction capability than the second gear, wherein the amount of memory space allocated for the storage of data payload within the region varies between the first gear and the second gear to accommodate a varying number of parity symbols between the first gear and the second gear; and

Li combined with Cideciyan renders obvious [15.2.2] for the reasons discussed at [1.2.2]. Ex.1003, ¶177.

[15.3] a second circuit configured to select a gear from the set for the region based at least partly on the comparisons to the one or more predetermined thresholds.

Li combined with Cideciyan renders obvious [15.3]. Ex.1003, ¶178.

As discussed at [1.3] and shown in Example 1.1 of the combination below, Li combined with Cideciyan renders obvious *a second circuit* (SSD controller 200 or elements thereof implementing adaptive encoder hardware block) *configured to select a gear from the set for the region based at least partly on the comparisons to the one or more predetermined thresholds*. Ex.1005, [0023] (“**an adaptive encoder hardware block** enabled to encode according to a selected one of a plurality of error correcting codes, and further enabled to dynamically **determine the selected error correcting code** based at least in part on the raw BER.”); [0126]; Ex.1003, ¶¶180. The “selected error correcting code” corresponds to an ECC scheme.



Example 1.1 of Combination Li and Cideciyan.

7. Claim 16

[16.0] *The apparatus of claim 15, wherein the ECC encoder is configured to determine the bit error rate and*

Li combined with Cideciyan renders obvious [16.0]. Ex.1003, ¶¶181-182.

Specifically, Li describes that *the ECC encoder (ECC 261) is configured to determine the bit error rate*. Ex.1005, [0126] (“ECC 261 implements one or more

functions performed by the **Error Statistics Collecting/Tracking, Universal Encoder**); Ex.1003, ¶182.

[16.1] the processor is configured to compare and to select in connection with at least one of flash initialization, read, or write operations for an end user.

Li combined with Cideciyan renders obvious [16.1]. Ex.1003, ¶¶183-185.

As discussed at [4.0], Li combined with Cideciyan renders obvious performing comparing and selecting *in connection with at least one of flash initialization, read, or write operations for an end user*. Ex.1005, [0114], Claim 16, FIGS. 1, 2A; Ex.1003, ¶184.

Li combined with Cideciyan renders that the “**processor**” is configured to perform selected functions including the comparing and selecting as a routine implementation. Ex.1005, [0137] (“It is also understood that **many functional aspects** of embodiments **are realizable selectively** [using] **processor**”); [0131]; *see also* Ex.1006, 9:29-31; Ex.1003, ¶185.

8. Claim 17

[17.0] The apparatus of claim 15, wherein the first circuit is further configured to read data from the region of flash memory,

Li combined with Cideciyan renders obvious [17.0]. Ex.1003, ¶¶186-187.

Specifically, in Li combined with Cideciyan, the first circuit (e.g., using SSD controller 200 including elements implementing the read-storage-data path) is *further configured to read data from the region of flash memory* for the reasons

discussed at [5.0]. Ex.1003, ¶187.

[17.1] wherein the ECC decoder is further configured to determine the bit error rate based at least partly on a number of errors corrected by ECC in connection with a read of data from the region.

Li combined with Cideciyan renders obvious [17.1]. Ex.1003, ¶¶188-189.

As discussed at [5.1], in Li combined with Cideciyan, *the ECC decoder* (e.g., using SSD controller 200 including elements implementing the read-storage-data path) is further configured to determine the raw BER “*based at least partly on a number of errors corrected by ECC*” (by comparison between the raw BER and the error-corrected version of the raw read data) *in connection with a read of data from the region* (associated with the reads of the portion). Ex.1005, [0050] (“the measured raw BER is determined at least in part by observing a BER associated with at least some **reads of the portion**”); [0051] (“measured raw BER is determined at least in part by comparing raw read data from the flash memory with an error-corrected version of the raw read data”); *see also* Ex.1005, [0079] (describing that an ECC scheme selected based on “a number of errors corrected.”). Ex.1003, ¶189.

9. Claims 22 and 29

[22.0/29.0] The apparatus of claim 15/24, wherein the gear includes a lower-latency ECC decode option and one or more higher-latency ECC decode options, wherein the gear is selected such that performance of ECC decoding with the lower-latency ECC decode option alone is sufficient to provide corrected data at least 90% of the time.

Li combined with Cideciyan renders obvious [22.0/29.0] for the reasons discussed at [14.0]. Ex.1003, ¶190.

10. Claim 23

[23.0] *The apparatus of claim 15, further comprising a plurality of flash memory devices, wherein the apparatus comprises a flash drive.*

Li combined with Cideciyan renders obvious [23.0]. Ex.1003, ¶191.

As shown in FIG. 2A, Li describes an apparatus comprising *a plurality of flash memory devices* (flash devices 292). Ex.1005, FIG. 2, [0110] (“one or more storage devices, such as **flash devices 292.**”). Li further describes the apparatus *comprises a flash drive* (Solid State Disk/Drive (SSD)). Ex.1005, [0014], [0016] (“Some SSDs use flash memory to provide non-volatile storage.”); Ex.1003, ¶192.

11. Claim 24

[24.0] *An apparatus for selecting an error correction coding (ECC) scheme, the apparatus comprising:*

To the extent that the preamble is limiting, Li combined with Cideciyan renders obvious [24.0] for reasons discussed at [15.0]. Ex.1003, ¶193.

[24.1.1] *a means for determining a bit error rate associated with a region comprising a fixed number of two or more flash memory pages or integer fractions thereof, wherein the two or more flash memory pages of a region can be read simultaneously,*

Li combined with Cideciyan renders obvious [24.1.1] for the reasons discussed at [1.1.1] and [15.1.1]. Ex.1003, ¶¶194-199; VII.B.1.

A POSITA would have understood that [24.1.1] to have:

Function: determining a bit error rate associated with a region comprising a fixed number of two or more flash memory pages or integer fractions. Ex.1001, 4:38-40. Ex.1003, ¶197.

Structure: a circuit. Ex.1001, 4:38-40 (“**a first circuit** configured to determine a bit error rate associated with a region...”); Ex.1003, ¶198.

As discussed at [1.1.1] and [15.1.1], Li combined with Cideciyan renders obvious [24.1.1], because it renders obvious a circuit (ECC 261 implementing Error Statistics Collecting/Tracking 180) for performing the function of determining a bit error rate associated with a region comprising a fixed number of two or more flash memory pages. Ex.1003, ¶199.

[24.1.2] wherein the region stores at least data payload and primary and secondary ECC parity symbols corresponding to the data payload of the region;

Li combined with Cideciyan renders obvious [24.1.2] for the reasons discussed at [1.1.2]. Ex.1003, ¶200.

[24.2.1] a means for comparing the determined bit error rate to one or more predetermined thresholds corresponding to a set of predefined gears comprising at least a first gear and a second gear, wherein the predefined gears correspond to different predefined ECC schemes,

Li combined with Cideciyan renders obvious [24.2.1] for reasons discussed at [1.2.1] and [15.2.1]. Ex.1003, ¶¶201-206.

A POSITA would have understood that [24.2.1] to have:

Function: comparing the determined bit error rate to one or more

predetermined thresholds corresponding to a set of predefined gears comprising at least a first gear and a second gear. Ex.1001, 4:38-40; Ex.1003, ¶204.

Structure: a circuit. Ex.1001, 4:38-47 (“**a first circuit** configured...to compare the determined bit error rate...”); Ex.1003, ¶205.

As discussed at [1.2.1] and [15.2.1], Li combined with Cideciyan renders obvious [24.2.1], because it renders obvious a circuit (Error Statistics Collecting/Tracking 180) for performing the function of comparing the determined bit error rate to one or more predetermined thresholds corresponding to a set of predefined gears, wherein the predefined gears correspond to different predefined ECC schemes. Ex.1003, ¶206.

[24.2.2] wherein the first gear has a different data payload size and correction capability than the second gear, wherein the amount of memory space allocated for the storage of data payload within the region varies between the first gear and the second gear to accommodate a varying number of parity symbols between the first gear and the second gear;

Li combined with Cideciyan renders obvious [24.2.2] for reasons discussed at [1.2.2]. Ex.1003, ¶207.

[24.3] a means for selecting a gear from the set for the region based at least partly on the comparisons to the one or more predetermined thresholds.

Li combined with Cideciyan renders obvious [24.3] for reasons discussed at [1.3] and [15.3]. Ex.1003, ¶¶208-213.

A POSITA would have understood that [24.3] to have:

Function: selecting a gear from the set for the region based at least partly on the comparisons to the one or more predetermined thresholds. Ex.1003, ¶¶211.

Structure: a circuit. Ex.1001, 4:47-49 (“**a second circuit** configured to select a gear...”); Ex.1003, ¶212.

As discussed at [1.3] and [15.3], Li combined with Cideciyan renders obvious renders obvious a circuit (SSD controller 200 including elements implementing adaptive encoder hardware block) for performing the function of selecting a gear as recited. Ex.1005, [0023], [0126]; Ex.1003, ¶213.

12. Claim 25

[25.0] *The apparatus of claim 24, further comprising means for reading data from the region of flash memory,*

Li combined with Cideciyan renders obvious [25.0] for the reasons discussed at [5.0] and [17.0]. Ex.1003, ¶¶214-218.

First, a POSITA would have understood that [25.0] to have:

Function: reading data from the region of flash memory. Ex.1003, ¶216.

Structure: a circuit including an ECC encoder/decoder. Ex.1001, 53:1-7; Ex.1003, ¶217.

As discussed at [5.0] and [17.0], Li combined with Cideciyan renders obvious a circuit (e.g., using SSD controller 200 including elements implementing the read-storage-data path) that performs the function of *reading data from the*

region of flash memory. Ex.1003, ¶218.

[25.1] wherein the determining means further comprises means for estimating the bit error rate based at least partly on a number of errors corrected by ECC in connection with reading the data from the region.

Li combined with Cideciyan renders obvious [25.1] for the reasons discussed at [5.1] and [17.1]. Ex.1003, ¶¶219-223.

A POSITA would have understood that [25.1] to have:

Function: estimating the bit error rate based at least partly on a number of errors corrected by ECC in connection with reading the data from the region. Ex.1003, ¶221.

Structure: a circuit including an ECC encoder/decoder. Ex.1001, 4:38-40 (“**a first circuit** configured to determine a bit error rate associated with a region associated with a plurality of flash memory pages or integer fractions thereof”); 53:1-7; Ex.1003, ¶222.

As discussed at [5.1] and [17.1], Li combined with Cideciyan renders obvious a circuit (ECC 261 implementing Error Statistics Collecting/Tracking 180, Universal Encoder 120 and Universal Decoder 160) for determining (see [24.1.1]) further performs the estimating function above. Ex.1003, ¶223.

13. Claim 30

[30.0] The apparatus of claim 24, further comprising a plurality of flash memory devices, wherein the apparatus comprises a flash drive.

Li combined with Cideciyan renders obvious [30.0] for reasons discussed at [23.0]. Ex.1003, ¶225.

14. Claims 31, 32, and 33

[31.0/32.0/33.0] *The method of claim 1/apparatus of claim 15/apparatus of claim 24, wherein the data payload and corresponding primary ECC parity symbols comprise primary codewords,*

Li combined with Cideciyan renders obvious [31.0/32.0/33.0]. Ex.1003, ¶¶226-227.

As shown in FIG. 4 below, Cideciyan as applied in the combination provides that *data payload* (input data) *and corresponding primary ECC parity symbols* (C1 parity symbols) *comprise primary codewords* (C1 codeword). Ex.1006, 10:60-64; 11:9-14; Ex.1003, ¶227.

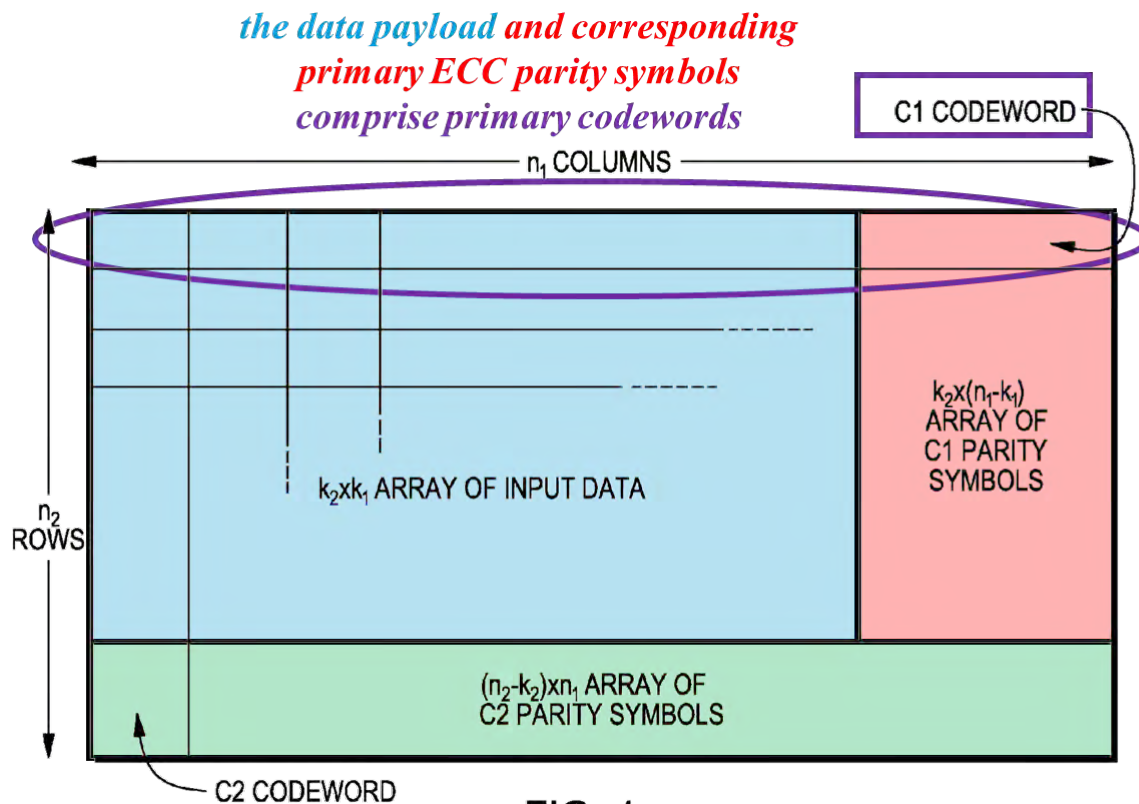


FIG. 4

Ex.1006, FIG. 4, annotated.

[31.1/32.1/33.1] wherein the data payload and corresponding secondary ECC parity symbols comprise secondary codewords,

Li combined with Cideciyan renders obvious [31.1/32.1/33.1]. Ex.1003,

¶¶228-229.

As shown in FIG. 4 below, Cideciyan as applied in the combination provides that data payload (input data) and corresponding secondary ECC parity symbols (C2 parity symbols) comprise secondary codewords (C2 codeword). Ex.1006, 11:1-5; 11:9-14; Ex.1003, ¶229.

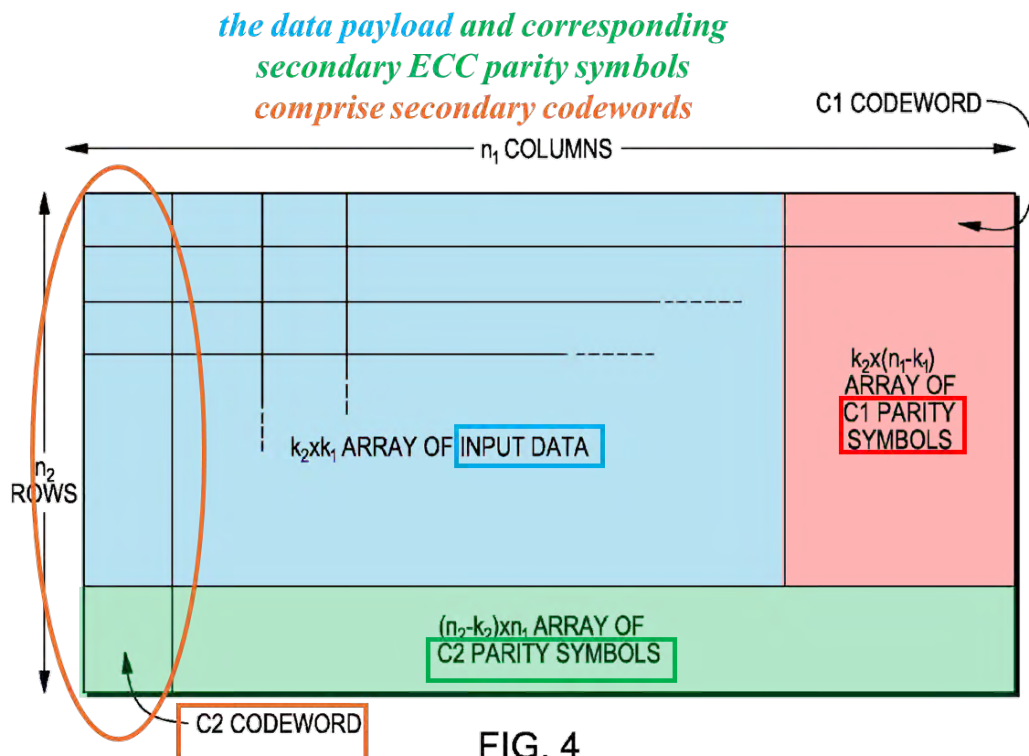


FIG. 4

[31.2/32.2/33.2] wherein the secondary ECC parity symbols of each secondary codeword are programmed across the region,

Li combined with Cideciyan renders obvious [31.2/32.2/33.2]. Ex.1003,

¶¶230-232.

Cideciyan describes that “while the C2 parity codes are stored in the N^{th} channel here, **any channel** could be used for the parity.” Ex.1006, 11:39-42; Ex.1003, ¶231 (citing Ex.1006, 11:9-14; 17:50-55). As shown in annotated FIG. 5 below, a POSITA would have understood that one implementation that “**any channel**” could be used is to program C2 parity symbols *across the region* (across the N channels), for the benefits of balancing the workload of both reading and writing operations, reducing the burden on any single channel or chip. Ex.1003,

¶232.

*the secondary ECC parity symbols
of each secondary codeword are
programmed across the region*

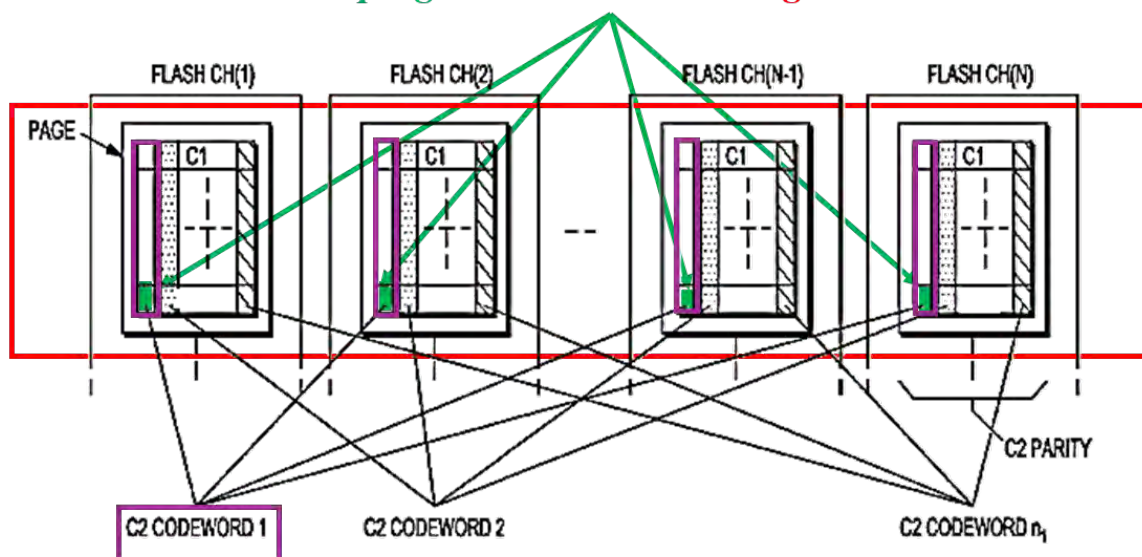


FIG. 5

Ex.1006, FIG. 5, annotated.

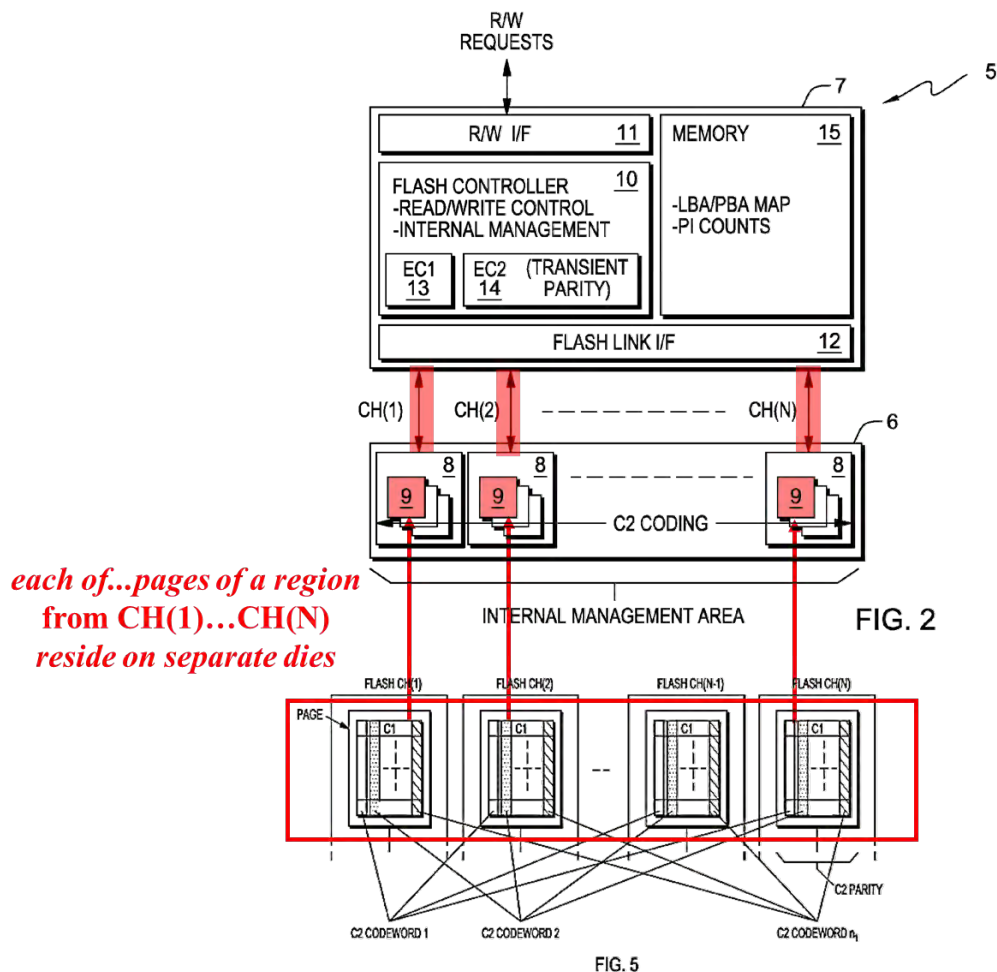
[31.3/32.3/33.3] wherein each of the two or more flash memory pages of a region reside on separate dies.

Li combined with Cideciyan renders obvious [31.3/32.3/33.3]. Ex.1003,

¶¶233-234.

Cideciyan as applied in the combination provides that the fixed number of multiple pages of a region reside on separate dies, corresponding to N channels.

Ex.1006, 8:53-59; Ex.1003, ¶234.



Ex.1006, FIGS. 2 and 5, annotated.

F. Ground 2: Claims 1-2, 4-5, 14-17, 22-25, and 29-33 are obvious in view of Li, Cideciyan, and Frost.

1. Claim Analysis

The claim analysis for Ground 2 is similar to that of Ground 1, with the additional analysis below explaining that Li combined with Cideciyan and Frost renders [1.1.1] of Claim 1 obvious. *See supra* X.E; Ex.1003, ¶235.

[1.1.1] determining a bit error rate associated with a region comprising a fixed number of two or more flash memory pages or integer fractions thereof, wherein

the two or more flash memory pages of a region can be read simultaneously,

The combination of Li, Cideciyan, and Frost renders obvious [1.1.1].

Ex.1003, ¶¶236-247.

To the extent that it is argued that Li combined with Cideciyan’s teaching that a group of N pages from across N channels (which is a traditional “page stripe”) accessible in parallel (*see* Ground 1:[1.1.1]) does not explicitly teach that those pages “***can be read simultaneously,***” the further combination with Frost renders it obvious, because the feature that pages from different channels “***can be read simultaneously***” as recited in [1.1.1] is a well-known and conventional implementation detail as taught by Frost. Ex.1003, ¶238.

For further detail, referring to FIG. 1 reproduced below, Frost describes that: each group of two chips forms a ‘Lane,’ also sometimes referred to as a ‘Channel,’....the controller 10 can issue commands and send or receive data across the various communication buses at the same time such that the system controller can access the memory chips corresponding to the individual Lanes at, or very nearly at, the same time.

Ex.1007, 6:46-67, 11:51-60 (all of the pages from separate lanes “can be written to or read from the memory array 14 simultaneously or near-simultaneously”);

Ex.1003, ¶239.

“the system controller can access the memory chips corresponding to the individual Lanes at, or very nearly at, the same time”

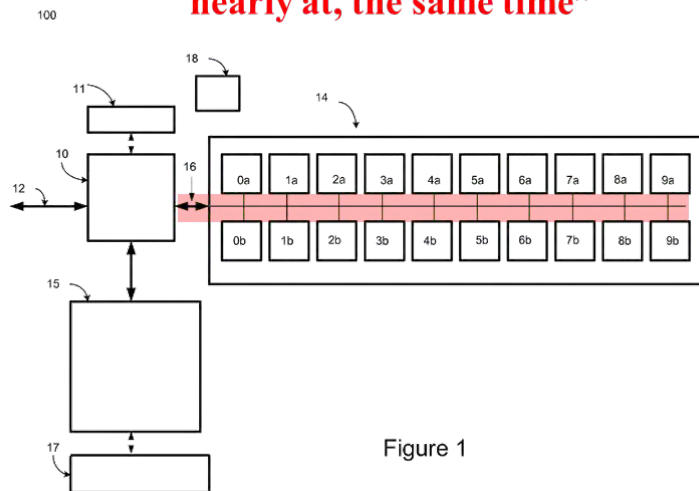


Figure 1

Ex.1007, FIG. 1, annotated.

As one example, referring to FIG. 7B below, Frost describes all of the pages associated with a **page stripe** can be read simultaneously across the multiple Lanes/Channels. Ex.1007, 11:51-60; Ex.1003, ¶240

“all of the Pages associated with Page Stripe 700 can be written to or read from the memory array 14 simultaneously or near-simultaneously.”

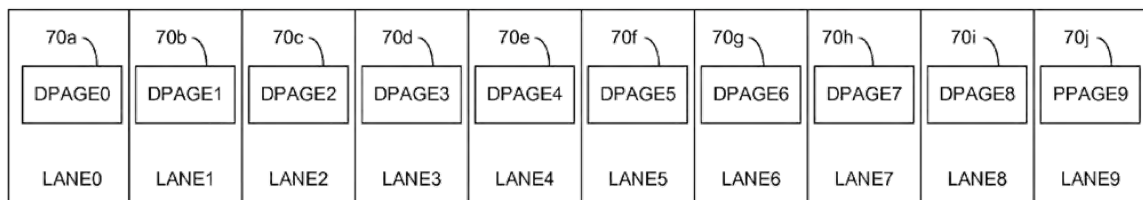


Figure 7B

Ex.1007, FIG. 7B, annotated.

As such, in Li combined with Cideciyan and Frost, pages in the region (a group of pages (page stripe) distributed across the channels) can be read simultaneously in Li combined with Cideciyan, which provides the benefit of “relatively quick read[] operations,” which renders obvious [1.1.1]. Ex.1007, 11:51-60; Ex.1003, ¶¶241-242.

Reasons to Combine Li, Cideciyan, and Frost

First, a POSITA would understand that parallel access (including read operations) using channels in Cideciyan (and Li) would be implemented simultaneously as shown in Frost. Ex.1003, ¶243.

Second, Li combined with Cideciyan teaches a region including pages distributed across multiple channels, while Frost provides how channels provide simultaneous access to those pages. The combination would provide the obvious, predictable, and beneficial result of simultaneous access, including “relatively quick read and write operations” and efficient and effective data storage and retrieval, as taught by Frost. Ex.1003, ¶244.

Third, as discussed at Ground 1:[1.1.1], a POSITA would have understood Cideciyan’s group of pages of FIG. 5 to be a traditional “page stripe.” Ex.1003, ¶245. Frost provides that pages in a “page stripe” are read simultaneously. *See, e.g.*, Ex.1007, FIG. 7B; Ex.1003, ¶245.

Additionally, the results of the proposed combination would have been

predictable and a POSITA would have had a reasonable expectation of success, because the combination merely applies known technique (channels and page stripes providing simultaneously read of pages) to a known device to yield the predictable results of quick read and write operations. Ex.1003, ¶246.

G. Grounds 3 and 4: Claims 6-7 and 18 are rendered obvious by each of Combination of Li, Cideciyan, and Leung (Ground 3) and Combination of Li, Cideciyan, Frost, and Leung (Ground 4).

1. Reasons to Combine Leung with Each of Grounds 1 and 2.

Li combined with Cideciyan and/or Frost, teaches that selecting a gear from the set of predetermined gears for the region, based on the determined bit error rate. Leung provides an obvious way of selection of the gear based on a *predetermined acceptable uncorrectable bit error rate (aUBER)* in addition to the bit error rate. Applying Leung's teaching in Li combined with Cideciyan and/or Frost would provide the benefit of optimal ECC scheme selection and memory array configuration to satisfy the aUBER requirements, while maximizing data payload size. Ex.1008, Table 1, [0033]; Ex.1003, ¶¶248-249.

The results of the proposed combinations would have been predictable and a POSITA would have had a reasonable expectation of success, because the combination merely applies known technique (Leung's selecting a gear based on a predetermined aUBER, in addition to the bit error rate) to a known device to yield the predictable results. Ex.1003, ¶249.

2. Claim 6

[6.0] The method of claim 1, wherein selecting further comprises selecting the gear that has the highest data payload size and sufficient correction capability for the determined bit error rate such that memory reads from the region can be corrected with no more than a predetermined acceptable uncorrectable bit error rate (aUBER).

Leung as combined with Grounds 1 and 2 each renders obvious [6.0].

Ex.1003, ¶¶250-255.

First, Li at least suggests [6.0] because its goal to provide more space “available to store data.” Ex.1005, [0104]; Ex.1003, ¶251.

Second, Leung describes choosing a gear (e.g., choosing bit error rate level 1 for incoming BER $3.4E-5$) with the lowest error correction capability among all three gears (bit error rate levels 1, 2, and 3), where all three gears satisfy the output error rate requirement (e.g., $1E-15$). Ex.1008, Table 1 reproduced below. Ex.1003, ¶¶252-253; Ex.1008, [0034] (“Initially, [operating] using **bit error rate level 1**. When the detected error rate approaches $3.4e-5$, the device may...operate at **bit error level 2..**”).

TABLE 1

Bit error rate level	Information bits per codeword	Parity per codeword	Codeword size	Information bits per 524 B	Capacity	Code rate	Incoming BER to maintain 1E-15 output error rate
1	512 B	12 B	524 B	512 B	100%	97.7%	3.4E-5
2	250 B	12 B	262 B	500 B	97.7%	95.45	6.3E-5
3	119 B	12 B	131 B	476 B	93.0%	90.8%	11.6E-5

Ex.1008, FIG. 1.

As discussed at X.G.1, a POSITA would have implemented Leung's teaching in the combination of Li, Cideciyan, and Frost, for maximizing data payload size while satisfying the aUBER requirement. Ex.1003, ¶254.

3. Claim 7

[7.0] The method of claim 6, wherein the aUBER is 1E-16.

Leung as combined with Grounds 1 and 2 each renders obvious [7.0].
Ex.1003, ¶¶256-258.

First, the limitation is a percentage without showing of any unexpected result, therefore is prima facie obvious.

Second, Leung describes that the aUBER (outgoing error rate) is 1E-16.
Ex.1008, FIG. 2, [0035]; Ex.1003, ¶257.

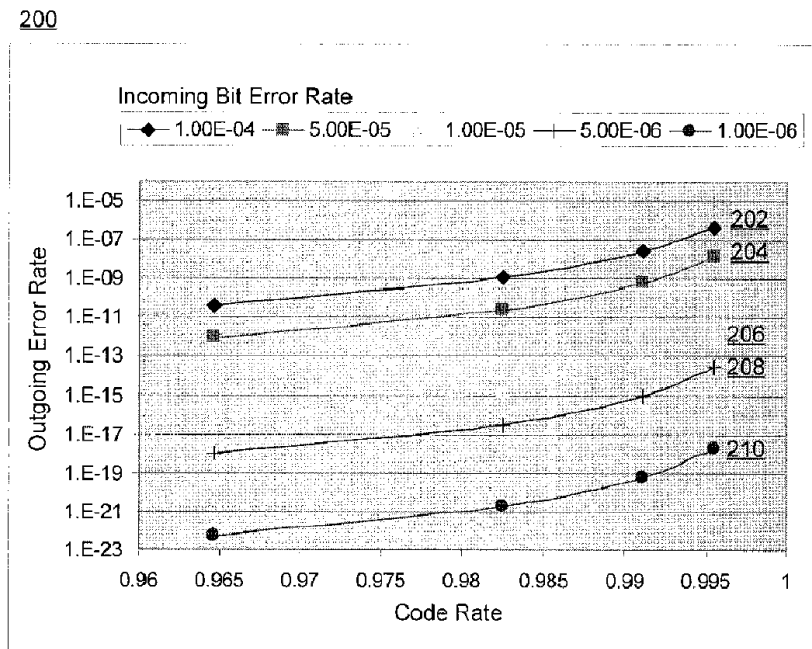


Fig. 2

Ex.1008, FIG. 2.

Thus, Leung as combined with Grounds 1 and 2 each renders obvious [7.0].

Ex.1003, ¶258.

4. Claim 18

[18.0] The apparatus of claim 15, wherein the processor is further configured to select a gear that has the highest data payload size and sufficient correction capability for the determined bit error rate such that memory reads from the region can be corrected with no more than a predetermined acceptable uncorrectable bit error rate (aUBER).

Leung as combined with Grounds 1 and 2 each renders obvious [18.0].

Ex.1003, ¶¶259-262.

First, Leung as combined with Grounds 1 and 2 renders obvious selecting a

gear as recited for reasons discussed at Grounds 3 and 4:[6.0]. Ex.1003, ¶260.

Second, Li combined with Cideciyan and Leung renders that the “**processor**” is configured to perform selected functions including the selecting a gear function. Ex.1005, [0137] (“many functional aspects of embodiments are realizable selectively [using] processor”); [0131]; *see also* Ex.1006, 9:29-31; Ex.1003, ¶261.

Accordingly, Li combined with Cideciyan and Leung renders obvious [18.0]. Ex.1003, ¶262.

XI. DISCRETIONARY DENIAL IS NOT WARRANTED

Petitioner respectfully submits that the Board should not exercise its discretion under 35 U.S.C. §§314(a) or 325(d) to deny this Petition.

A. The Fintiv factors favor institution.

Denial would be improper based on factors in *Apple v. Fintiv*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential).

1. No evidence regarding a stay

No motion to stay has been filed, so the Board should not infer the outcome of such a motion.

2. Parallel proceeding trial date

This factor weighs against discretionary denial. While the scheduled trial date is June 16, 2026, (Ex.1021, 25), the projected trial date—based on median time-to-trial statistics—is in January of 2027², which is well after the projected date for the Board to issue a Final Written Decision in July of 2026. Because the

² The current average time-to-trial for the district court hearing the co-pending litigation is 29.1 months. *See* Ex.1015 and Ex.1016. The Director recently clarified that in weighing Fintiv Factor 2 the Board may consider “evidence regarding the most recent statistics on median time-to-trial for civil actions in the district court in which the parallel litigation resides.” Ex.1017, *Fintiv* Memorandum, at 8–9.

projected trial date is approximately six months *after* the Board’s expected date for issuing a Final Written Decision, this factor weighs against discretionary denial.

3. Investment in the parallel proceeding

The investment in the co-pending litigation has been minimal. No schedule has been set. Thus, the Markman hearing is unlikely to occur before the Board issues an institution decision. This lack of investment favors institution.

4. Overlapping issues with the parallel proceeding

The co-pending litigation is in its early stages. Petitioner served its preliminary invalidity contentions on December 16, 2024. However, Petitioner has not served its final invalidity contentions, nor has the deadline for doing so been set. The extent of overlap is thus speculative at this point in time.

5. Petitioner is a defendant

Petitioner is a defendant in the co-pending litigation. That is true of most Petitioners in IPR proceedings, making this factor neutral.

6. Other circumstances

“[T]he PTAB will not deny institution of an IPR or PGR under *Fintiv* (i) when a petition presents compelling evidence of unpatentability.” Ex.1017, 9. Here, the petition—along with Dr. Dolecek expert testimony—plainly shows that the ’085 patent claims no more than known concepts related to adaptive ECC in a flash memory based storage system.

B. Advanced Bionics Test Favors Institution.

Denial under § 325(d) is not warranted because the challenges presented in this petition are neither cumulative nor redundant to the prosecution of the '085 patent. The Examiner did not consider Cideciyan, Frost, and Leung during prosecution. Li (Ex.1005) and patents (US 8,255,620; 8,560,881; and 8,713,245) related to Frost (Ex.1007) were listed on IDS, but were never relied upon by the Office. Ex.1002, 633, 730. There is no evidence that the Examiner substantively considered Li and the patents related to Frost with respect to the Challenged Claims. Moreover, the Examiner did not consider Li and the patents related to Frost in combination with Cideciyan and/or Leung as presented in Petitioner's grounds.

Thus, the first prong of the *Advanced Bionics* analysis is not met, because the same or substantially the same art or arguments were not presented during prosecution. *Advanced Bionics*, IPR2019-01469, Paper 6 at 8 (Feb. 13, 2020) (precedential). The second prong is also not met, because the Examiner erred in a material to patentability by overlooking Li and Cideciyan for teaching adaptive ECC techniques applying to a region including a fixed number of pages that can be read simultaneously, where the region stores data payload and primary and secondary ECC parity symbols. *Id.* at 8-9, n.10.

XII. CONCLUSION

Petitioner has established a reasonable likelihood that the Challenged Claims are unpatentable.

XIII. MANDATORY NOTICES**A. Real Party-in-Interest**

The real parties-in-interest (“RPI”) are Sandisk Technologies, Inc. and Western Digital Technologies, Inc. (“Petitioner”).

B. Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), to the best knowledge of the Petitioner, the ’085 patent is or was involved in the following cases:

Case Heading	Number	Court	Filed	Status
<i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i>	2-24-cv-02864	CDCA	April 9, 2024	Pending
<i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i>	1-24-cv-00101	WDTX	January 30, 2024	Pending

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Please address all correspondence in this proceeding to lead and back-up counsel. Petitioner consents to service in this proceeding by email at the addresses above.

Respectfully submitted,

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CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner hereby certifies, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,858. Pursuant to 37 C.F.R. § 42.24(d), this word count excludes the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: January 29, 2025

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CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105, service was made on Patent Owner as detailed below.

Date of service January 29, 2025

Manner of service FEDERAL EXPRESS

Documents served Petition for *Inter Partes* Review Under 35 U.S.C. § 312 and 37 C.F.R. § 42.104 of U.S. 9,183,085; Petitioner's Power of Attorney; Petitioner's Exhibit List; and All Exhibits.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND
WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioners

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner

Case IPR2025-00515
U.S. Patent No. 9,183,085

**PATENT OWNER POLARIS POWERLED TECHNOLOGIES, LLC'S
BRIEF ON DISCRETIONARY DENIAL**

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PATENT OWNER'S EXHIBIT LIST

Exhibit No.	Description
2001	List of Docket Entries, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 1-24-cv-00101 (W.D. Tex.)
2002	List of Docket Entries, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal)
2003	List of Docket Entries, <i>Micron Technology Inc. et al. v. Polaris PowerLED Techs., LLC</i> , 1-25-cv-00073 (D. Idaho)
2004	Scheduling and Case Management Order, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Jan. 27, 2025), ECF No. 54
2005	Western Digital's Notice of Motion and Motion to Stay Action Pending <i>Inter Partes</i> Review, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Feb. 3, 2025), ECF No. 58
2006	Minute Order, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Feb 3, 2025), ECF No. 59
2007	Plaintiff's Opposition to Motion to Stay, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Feb. 10, 2025), ECF No. 60
2008	Patent L.R. 3-3 and 3-4 Invalidity Disclosures of Western Digital Defendants, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal), ECF No. 60-3 and Appendices A-C of the Invalidity Disclosures
2009	Defendants' Identification of Claim Terms for Construction, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal), ECF No. 60-4
2010	Stipulated Protective Order, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal), ECF No. 61

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Exhibit No.	Description
2011	Western Digital’s Reply in Support of Motion to Stay Action Pending <i>Inter Partes</i> Review, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Feb. 14, 2025), ECF No. 62
2012	USPTO Appeal Statistics (Mar. 31, 2025), <i>available at</i> https://www.uspto.gov/patents/ptab/statistics
2013	Patent Trial & Appeal Board (PTAB) Dashboard, <i>available at</i> https://www.uspto.gov/dashboard/ptab/
2014	Press Release: SanDisk Celebrates Nasdaq Listing After Completing Separation from Western Digital (Feb. 24, 2025), <i>available at</i> https://shop.sandisk.com/company/newsroom/press-releases/2025/sandisk-celebrates-nasdaq-listing-after-completing-separation
2015	Excerpt from the Prosecution History of U.S. Patent Application No. 14/483,915—including a Notice of References Cited (Apr. 11, 2016)
2016	U.S. Patent No. 9,411,669 to Reddy <i>et al.</i>
2017	Defendants’ Identification of Claim Terms for Construction (Apr. 18, 2025), <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal. Feb. 10, 2025)

I. INTRODUCTION

The Board should exercise its discretion under 35 U.S.C. § 314(a) and *Fintiv* to deny institution of this *inter partes* review (IPR) because the same parties are in advanced stages of litigating the validity of this patent in district court. The district court trial is scheduled for June 16, 2026—more than two months *before* the Board’s projected deadline for issuing a final written decision. Litigating the same issues at the Board would therefore be duplicative and contrary to the intent of IPRs for “providing a more efficient system for challenging patents” and “reducing unwarranted litigation costs.” H.R. Rep. No. 112-98 at 39-40 (2011); *see also NHK Spring Co. Ltd. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 19-20 (P.T.A.B. Sept. 12, 2018) (precedential).

Other considerations also strongly favor discretionary denial. For example, Petitioners have not agreed to a *Sotera* stipulation or identified any reason why instituting an IPR would reduce the number of issues litigated in district court. Since the district court trial is already scheduled and instituting an IPR would not improve judicial efficiencies, the Board should deny institution and focus its limited resources on other pending cases at the Board.

II. THE BOARD SHOULD DENY INSTITUTION UNDER § 314(A).

A. The *Fintiv* factors favor discretionary denial.

When the patent owner raises an argument for discretionary denial due to an earlier trial date in a co-pending litigation, the Board weighs the following factors:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Apple Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 at 5-6 (P.T.A.B. Mar. 20, 2020) (precedential) ("*Fintiv*"). These factors, when considered as a whole, support *denying* institution. Factor 1 is neutral, factors 2-6 all weigh in favor of denial, and no factor weighs against exercising the Board's discretion to deny institution.

1. Factor 1 is, at worst, neutral because there is no evidence a stay order will be granted in the district court.

Under the first factor, if the district court stays the case or provides guidance that it will stay the case and await the Board's final resolution of the patentability issues, this fact usually weighs against exercising authority to deny institution. *Fintiv*, 7. However, here, the district court has not provided such guidance and issued a scheduling order to continue through trial. EX2004.

Actions in the district court indicate that a stay is *not* imminent because the case is moving faster than initially scheduled. On January 27, 2025, the district

court issued its scheduling and case management order, which set the deadlines to file infringement contentions and invalidity contentions as February 18, 2025, and April 4, 2025, respectively. EX2004, 26. After Western Digital filed a motion to stay the case (EX2005), the parties decided to advance the case by jointly stipulating to serve, before they were due, amended infringement and invalidity contentions. EX2006.

The amended infringement and invalidity contentions were served early to resolve a discovery dispute over the scope of accused products. Polaris's initial infringement contentions, served in October 2024, accused all Western Digital and SanDisk solid-state drive products from 2018 onward supporting NVMe, among other features, and included a list of exemplar product lines. Western Digital challenged the sufficiency of these contentions, arguing they lacked adequate detail for products beyond WD Black-branded SSDs, and consequently limited its discovery production to only those SSDs. To break this impasse and advance discovery on the full scope of accused products, Polaris prepared and sent proposed amended infringement contentions to Western Digital. These amended contentions included significantly expanded claim charts, reflecting a substantial increase in detail about exemplary SSD product lines. Polaris maintained that its initial contentions were sufficient and compliant with applicable rules, and the amended contentions were offered to address Western Digital's concerns and

resolve the dispute amicably. Western Digital acknowledged that the proposed amended contentions addressed its concerns about detail but conditioned its agreement to Polaris' service of these contentions on Polaris allowing Western Digital to serve amended invalidity contentions. Western Digital claimed its December 2024 invalidity contentions inadvertently omitted certain details and sought to amend them. After negotiations, the parties reached an agreement and submitted a stipulation to the Court on February 3, 2025. That same day, the Court approved the stipulation, permitting both Polaris' amended infringement contentions and Western Digital's amended invalidity contentions. As ordered, the parties exchanged the amended infringement and invalidity contentions early.

The parties also exchanged proposed terms for construction earlier than required. EX2002 (deadline for exchange April 18, 2025); EX2009 (identification of claim terms served on January 24, 2025). Such proactive measures show that the district court case is advancing according to schedule (if not faster).

Western Digital's motion to stay the district court case (EX2005) is still pending, but there is no indication that the court will grant the motion. In fact, the district court canceled the hearing on the motion. EX2002, ECF No. 63. And the court has denied motions to stay in cases—like this one—where the defendant waited almost a year after it was served with a complaint to file an IPR petition. Order Denying Defendant Skechers U.S.A., Inc.'s Motion to Stay Pending *Inter*

Partes Review at 2, *Nike, Inc. v. Skechers U.S.A., Inc.*, 2-19-cv-9230 (C.D. Cal Dec. 30, 2020), ECF No. 82 (“Defendant waited almost a year after it was served with the Complaint to file its IPR petitions. Defendants’ delay in filing its IPR petitions also weighs against granting a stay.”) (citation omitted); Order Denying Defendant’s Motion to Stay at 5, *Jiaying Super Lighting Elec. Appliance Co., Ltd. et al. v. MaxLite, Inc.*, 2-19-cv-4047 (C.D. Cal June 17, 2020), ECF No. 73 (“Such a delay cuts against granting a stay because ‘courts expect accused infringers to evaluate whether to file, and then to file, IPR petitions as soon as possible after learning that a patent may be asserted against them.’”) (citation omitted).

Regardless of Western Digital’s arguments in favor of a stay (EX2005, EX2011), there is no specific evidence that the district court will stay the case. “In the absence of specific evidence, [the Board] will not attempt to predict how the district court in the related district court litigation will proceed because the court may determine whether or not to stay any individual case . . . based on a variety of circumstances and facts beyond [the Board’s] control and to which the Board is not privy.” *Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (P.T.A.B. June 16, 2020) (informative). The first *Fintiv* factor is therefore, at worst, neutral. *Id.*; *Fintiv*, 6-9.

2. Factor 2 favors discretionary denial because the district court’s trial date is scheduled to occur before the projected final written decision.

The second factor weighs in favor of denying institution because the district court’s scheduled trial date is before the Board’s projected statutory deadline. See *Fintiv*, 9. The district court scheduled trial for June 16, 2026. EX2004, 25. This trial date is *before* the Board’s projected final written decision. Polaris’s POPR is due May 27, 2025.¹ An institution decision is then due August 27, 2025. 35 U.S.C. § 314(b). If instituted, that timeline would make the final written decision due August 27, 2026—more than two months *after* the district court’s trial date. 35 U.S.C. § 316(a)(11). “If the court’s trial date is earlier than the projected statutory deadline, the Board generally has weighed this fact in favor of exercising authority to deny institution” *Fintiv*, 9. In *Fintiv*, a scheduled district court trial date two months before the projected final written decision—a similar timeframe—weighed in favor of discretionary denial. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 13 (P.T.A.B. May 13, 2020) (informative) (“*Fintiv II*”).

Petitioners’ statistical-based argument for a 2027 trial date is no longer

¹ The POPR is due three months after the February 26th Notice of Filing Date. 37 C.F.R. § 42.107(b). May 26th is a Federal holiday, which makes the POPR due the next business day. 37 C.F.R. § 1.7(a).

relevant. In the petition, Petitioners projected a trial date in January 2027 based on the median time-to-trial for civil cases in the Central District of California. Pet., 85 n.2 (citing EX1016). But after Petitioners filed the petition, the court scheduled trial for June 16, 2026. EX2004, 25. Nothing in the district court record indicates that the court intends to deviate from this schedule. To the contrary, the court stated that this date was “firm.” EX2004, 1.

The second *Fintiv* factor therefore weighs in favor of discretionary denial as it did in *Fintiv*. *Fintiv*, 9; *Fintiv II*, 13.

3. Factor 3 favors denial because the parties have already invested substantial resources in the parallel proceedings.

Under the third *Fintiv* factor, “[t]he Board also has considered the amount and type of work already completed in the parallel litigation by the court and the parties *at the time of the institution decision*.” *Fintiv*, 9 (emphasis added). The deadline for issuing an institution decision is August 27, 2025. *Supra* Section II.A.2. By this date, substantial work will have already been done, including final invalidity contentions, all discovery and briefing for claim construction, and the Markman hearing. This heavy investment by the parties and the district court favors denial of institution. *Fintiv*, 9-12.

Work Performed to Date:

- January 30, 2024: Polaris filed a complaint for patent infringement in the Western District of Texas. EX2001, ECF No. 1.

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- April 9, 2024: Polaris re-filed the case in the Central District of California to resolve a threatened motion to transfer. EX2002, ECF No. 1. Polaris dismissed its Western District of Texas (W.D. Tex.) case on April 5, 2024, and refiled in the Central District of California (C.D. Cal.) on April 9, 2024, at Western Digital's suggestion, to resolve a venue dispute and avoid related motion practice costs. Western Digital proposed a stipulated dismissal without prejudice for transfer to C.D. Cal. because Western Digital argued that W.D. Tex. was an improper venue.
- June 21, 2024: Polaris filed an amended complaint. EX2002, ECF No. 40. The complaint included claim charts detailing alleged infringement of claims 1, 2, 4, and 14-16 of the '085 patent. *See* EX2002, ECF No. 40-5.
- October 2, 2024: Polaris served its first sets of requests for production and interrogatories. *See* EX2007, *22.
- October 2, 2024: Polaris served its initial infringement contentions and accompanying document production. *See* EX2007, *22. The initial infringement contentions identified the asserted claims. *See* EX2008, *3.
- June 5, 2024: Western Digital filed answers to the amended complaint. EX2002, ECF Nos. 43-45.
- November 1, 2024: Western Digital responded to requests for production. *See* EX2007, *22.
- November 22, 2024: Western Digital responded to interrogatories. *See* EX2007, *22.
- December 16, 2024: Western Digital served invalidity contentions and accompanying document production. EX2008. The contentions charted 16 references for the '085 patent, cited numerous other references, and cited product art from different companies. *Id.*, *34-37. The contentions also analyze the motivation to combine for different combinations. *Id.*, *38-45. They also provide contentions under §§ 101 and 112. *Id.*, *45-51. In total, the invalidity contentions comprise over 3,000 pages. *See* EX2007, *22.
- January 24, 2025: Western Digital identified terms for construction, including eight terms for the '085 patent. EX2009.

Case IPR2025-00515
U.S. Patent No. 9,183,085

- February 4, 2025: Polaris had served amended infringement contentions that identified the asserted claims again. *See* EX2007, *22.
- February 6, 2025: Western Digital served amended invalidity contentions. *See* EX2007, *22.
- February 11, 2025: The court ordered entry of the protective order. EX2010.
- April 18, 2025: Western Digital served Defendants’ Identification of Claim Terms for Construction, which this time included four terms for the ’085 patent. EX2017, *3.

Additional Work To Be Completed Before the Institution Decision (EX2004, 26):

- May 9, 2025: Preliminary Claim Constructions and Extrinsic Evidence Due
- May 24, 2025: Damages Contentions Due
- June 3, 2025: Joint Claim Construction, Prehearing Statement, and Expert Reports on Claim Construction Due
- June 23, 2025: Responsive Damages Contentions Due
- July 28, 2025: Deadline to Amend Pleadings or Add Parties
- July 3, 2025: Claim Construction Discovery Cutoff
- July 18, 2025: Claim Construction Opening Briefs Due
- July 23, 2025: Damages Contentions Meeting Deadline
- August 1, 2025: Claim Construction Responsive Briefs Due
- August 8, 2025: Claim Construction Reply Briefs Due
- August 22, 2025: Markman Hearing

For the work scheduled between filing this brief and the deadline of the institution decision, the district court has stated that “[t]hese dates and requirements are firm.” EX2004, 1. Based on the level of investment and effort

already expended on claim construction and invalidity contentions in the district court, this factor weighs in favor of discretionary denial. *Fintiv II*, 14.

Under *Fintiv* factor 3, the Board also considers whether the petitioner could have filed the petition more expeditiously to avoid unnecessary investment by the parties and the court. *Fintiv*, 11. “[I]f the petitioner cannot explain the delay in filing its petition, these facts have favored denial.” *Fintiv*, 12; *Next Caller Inc. v. TRUSTID, Inc.*, IPR2019-00961, Paper 10 at 16 (P.T.A.B. Oct. 16, 2019) (weighing the petitioner’s unexplained delay in filing the petition in favor of denial and noting that had the petitioner filed the petition earlier, the PTAB proceeding may have resolved the issues before the district court).

Here, Petitioners could have filed the IPR petition well before substantial work started in the district court case. Western Digital Technologies, Inc. was first served with a complaint alleging infringement of the ’085 patent on January 30, 2024. EX2001 at ECF No. 1.² Polaris first identified the asserted claims on June

² The litigation was originally filed in the Western District of Texas on January 30, 2024, as Case No. 1:24-cv-00101, but refiled in the Central District of California on April 9, 2024. The one-year time bar for filing an IPR petition is tied to the filing of the first case. *Click-To-Call Techs., LP v. Ingenio, Inc.*, *Yellowpages.Com, LLC*, 899 F.3d 1321, 1328 n.3 (Fed. Cir. 2018) (*en banc*),

21, 2024, in its amended complaint, and then again on October 2, 2024, in its initial infringement contentions. *See* EX2002, ECF No. 40-6; EX2008, *3. So Western Digital first had notice of the asserted claims in June 2024. Rather than filing a petition in the early stages of the case after knowing the asserted claims, Petitioners waited *for about seven months* and filed the petition in the last possible week after substantial work ensued. Petitioners did not explain this lengthy delay in the Petition. This inexcusable delay makes factor 3 weigh even more in favor of denying institution. *Next Caller*, IPR2019-00961, Paper 10 at 16. It also makes a stay less likely. *Supra* Section II.A.1.

4. Factor 4 favors denial because there is substantial overlap between the IPR grounds and the invalidity contentions in the district court case.

The fourth *Fintiv* factor—overlap between issues raised in the petition and in the parallel proceeding—favors denying institution. “[I]f the petition includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding, this fact has favored denial.” *Fintiv*, 12. “Conversely, if the petition includes materially different grounds, arguments, and/or evidence than those presented in the district court, this fact has tended to weigh against exercising discretion to deny institution” *Id.*, 12-13.

vacated on other grounds.

Petitioners have relied on the same references in this IPR as the references in its invalidity contentions, showing that parallel proceedings would result in substantial overlap and duplicative work. The IPR grounds include four references: (1) U.S. Patent Application Pub. No. 2014/0136927 to Li *et al.*; (2) U.S. Patent No. 9,037,951 to Cideciyan *et al.*; (3) U.S. Patent No. 8,176,360 to Frost *et al.*; and (4) U.S. Patent Application Pub. No. 2008/0222490 to Leung *et al.* Pet., 11-12. The claim charts in Western Digital's invalidity contentions (B1, B2, B4, and B12) rely on the same four references, as shown below.

Claim Charts in the Invalidity Contentions

Claim Chart	Reference
Chart B1	U.S. Patent No. 8,176,360 to Frost <i>et al.</i>
Chart B2	U.S. Patent Application Pub. No. 2014/0136927 to Li <i>et al.</i>
Chart B4	U.S. Patent Application Pub. No. 2008/0222490 to Leung <i>et al.</i> ³
Chart B12	U.S. Patent No. 9,037,951 to Cideciyan <i>et al.</i>

Western Digital's invalidity contentions rely on additional references

³ The contentions incorrectly list Leung's publication number as 2008/0333490, which is a publication number that does not exist. EX2008, *34.

(EX2008, *34-35), but “Petitioner’s assertion of additional invalidity contentions in the District Court is not relevant to the question of the degree of overlap for this factor.” *Fintiv II*, 15. “[B]ecause the identical claims are challenged based on the same prior art in both the Petition and in the District Court, this factor weighs in favor of discretionary denial in this case.” *Id.*

Western Digital has also not submitted any stipulation limiting the art that it can present at trial, which indicates that it intends to raise the same invalidity positions in district court. *See Sand Revolution II*, IPR2019-01393, Paper 24 at 12 (“Petitioner’s stipulation, however, mitigates to some degree the concerns of duplicative efforts between the district court and the Board, as well as concerns of potentially conflicting decisions.”); *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (P.T.A.B. Dec. 1, 2020) (precedential as to II.A) (“such a broad stipulation better addresses concerns of duplicative efforts and potentially conflicting decisions in a much more substantial way.”). Even if Western Digital were to submit a stipulation, it is too late—the Board’s discretionary panels should consider stipulations only if they are filed with sufficient time for a patent owner to address the impact of the stipulation in its discretionary denial brief. *See* FAQs for Interim Process for PTAB Workload Management, FAQ14; PTAB Boardside Chat on Interim Process for PTAB Workload Management (Apr. 17, 2025) (petitioners “*must*” file a stipulation within one month of the notice of filing date for

consideration). Petitioners have had ample time to file a stipulation and have chosen not to. Factor 4 weighs in favor of denial on this basis alone.

Factor 4 also weighs in favor of denial because Western Digital relies on system prior art in its invalidity contentions, which prevents this case from being a “true alternative” to the district court proceeding. *Cf. Motorola Solutions, Inc. v. Stellar, LLC*, IPR2024-01205, Paper 19 at 3-4 (P.T.A.B. Mar. 28, 2025). In *Motorola*, the Director denied institution under 35 U.S.C. § 314(a) because “Petitioner’s invalidity arguments in the district court are more expansive and include combinations of the prior art asserted in these proceedings with unpublished system prior art” *Id.*, 4.⁴ Similar here, Western Digital’s invalidity contentions include combinations of the asserted art with system prior art. *See* EX2008, *34-37 (relying on system prior art from numerous companies). For example, Western Digital has alleged invalidity based on: “Texas Memory Systems, Inc. and/or IBM, Corp. products that embody US Patent No. 8,176,360 to

⁴ In *Motorola*, the Director suggested that the petitioner’s stipulation “is not likely to moot” a combination of prior art asserted in the IPR proceeding and system prior art. *Motorola*, IPR2024-01205, Paper 19 at 4. Patent Owner takes no position whether a *Sotera* stipulation is not likely to moot such a combination of prior art. Regardless, Petitioners have not offered such stipulations here.

Frost et al;” “LSI Corporation products that embody U.S. Patent Application Pub. 2014/0136927 to Li et al;” Intel Corporation products that embody U.S. Patent Application Pub. 2008/0333490 [sic] to Leung et al;” and “IBM Corp. products that embody US Patent No. 9,037,951.” EX2008, *35-37. Accordingly, this IPR would not be a “true alternative” to the district court case but instead litigate the same or (at best) substantially similar invalidity grounds.

The risk of duplicative litigation is even higher here because Western Digital Corporation is not a named petitioner, RPI, or privy, and may still try to raise the identical invalidity positions in the district court case. Petitioners appear to have strategically omitted the defendant Western Digital Corporation—the parent corporation of Western Digital Technologies, Inc.⁵—from the petition to evade estoppels.⁶ When Polaris raised this issue in briefing in the district court case

⁵ If the Board determines that Western Digital Corporation is an unnamed real party in interest or privy of Petitioners, Petitioners’ gamesmanship favors denying institution. *See* 35 U.S.C. §§ 312(a)(2).

⁶ Estoppels under 35 U.S.C. § 315(e)(2) apply only to a petitioner, real party in interest, or privy of the petitioner. Western Digital Corporation is not a petitioner, and is not listed as an RPI or privy of the petitioner. So Western Digital Corporation appears to be reserving an argument that it is not estopped in district

(EX2007, *16), Western Digital Corporation tried to cure the issue by agreeing to estoppels. EX2011, *5. But it did so conditionally, stating: “[S]hould a stay be granted, Western Digital Corporation agrees to be bound under 35 U.S.C. § 315(e)(2).” *Id.* (emphasis added). If the court does not grant a stay, Western Digital Corporation could try to litigate the same grounds in district court.

For these reasons, the fourth *Fintiv* factor weighs strongly in favor of denying institution. *Fintiv*, 12. This inefficiency and duplication of efforts is precisely what the Board’s discretionary authority is intended to prevent. *NHK Spring*, IPR2018-00752, Paper 8 at 19-20; H.R. Rep. No. 112-98 at 39-40 (2011). And the Board should not permit Western Digital Corporation’s gamesmanship.

5. Factor 5 favors denial because the parties in the IPR overlap with the parties in the district court litigation.

Under the fifth *Fintiv* factor, “[i]f a petitioner is unrelated to a defendant in an earlier court proceeding, the Board has weighed this fact against exercising discretion to deny institution” *Fintiv*, 13-14. But here, both of the Petitioners are or are related to a defendant in the co-pending litigation. Western Digital Technologies, Inc. is a defendant in the litigation. SanDisk Technologies, Inc. is a

court from raising the same grounds presented in the IPR, which further demonstrates that this IPR is not a “true alternative” to litigating validity before the district court.

related party and real party in interest because it was owned by Western Digital as of the filing date of the petition. *See* EX2014 (announcing on February 24, 2025 its separation from Western Digital); Pet., 88 (“The real parties-in-interest (‘RPI’) are SanDisk Technologies, Inc. and Western Digital Technologies, Inc. (‘Petitioner’).”). Even if SanDisk were unrelated to a defendant, “if the issues are the same as, or substantially similar to, those already or about to be litigated, or other circumstances weigh against redoing the work of another tribunal, the Board may, nonetheless, exercise the authority to deny institution.” *Fintiv*, 14.

This factor therefore weighs in favor of denial. *Fintiv*, 13-14. And, if the Board deems SanDisk unrelated, it should still deny institution. *Id.*

6. Factor 6 favors denial, but Polaris will raise its merits arguments in the POPR.

Under the sixth *Fintiv* factor, the Board may consider other circumstances that impact the Board’s exercise of discretion, including the merits. *Fintiv*, 14-15. Polaris’s merits arguments will be in its Patent Owner Preliminary Response (POPR), which will explain why the grounds fail to disclose the claim elements. The Director should consider these arguments when determining whether to exercise its discretion to deny institution under 35 U.S.C. § 314(a). *See* FAQs for Interim Process for PTAB Workload Management, FAQ8 (“The Director will receive each . . . POPR”), FAQ12 (“the Director will consider the merits in the merits briefing if the parties ask the Director to do so.”).

B. Other considerations also favor discretionary denial.

The Board's Memorandum on the Interim Process for PTAB Workload

Management presents additional considerations for discretionary denial, including:

Whether the PTAB or another forum has already adjudicated the validity or patentability of the challenged patent claims;

Whether there have been changes in the law or new judicial precedent issued since issuance of the claims that may affect patentability;

The strength of the unpatentability challenge;

The extent of the petition's reliance on expert testimony;

Settled expectations of the parties, such as the length of time the claims have been in force;

Compelling economic, public health, or national security interests; and

Any other considerations bearing on the Director's discretion.

Interim Processes for PTAB Workload Management at 2 (Mar. 26, 2025). There are several considerations that weigh in favor of discretionary denial here.

1. Instituting an IPR would not reduce the number of issues for the judge and jury to decide in the district court case.

The Board should also deny institution because the Petitioners have not explained how instituting an IPR would reduce the number of issues adjudicated by the district court judge and decided by a jury. For example, Petitioners have not represented or indicated that they would present fewer references or grounds to the jury if an IPR is instituted. Instead, Western Digital's extensive 3,000-page invalidity contentions show the opposite—that it will present as many grounds and

references to the jury as the court allows. In the invalidity contentions, Western Digital charted sixteen references for the '085 patent. EX2008, *34-35. It also served a list of approximately **600** different “References and Exemplary Combinations of References” for the '085 patent that it reserves the right to present to the jury. EX2008 (Appendix B).

Western Digital also cited product art from numerous companies. EX2008, *35-37. Even if the four references in the petition were removed from the candidate pool (EX1005, EX1006, EX1007, EX1008), Western Digital would still have many references to combine with product art. *See* 35 U.S.C. § 315(e) (estoppels do not apply to product prior art). Instituting an IPR would therefore not reduce the number of references or grounds but instead merely shift which references and grounds the defendants decide to present to the jury.

Instituting an IPR would also not resolve other invalidity theories such as Western Digital’s arguments under 35 U.S.C. §§ 101 and 112. “Where the petitioner is relying on corresponding system art in a co-pending proceeding *and/or several other invalidity theories*, a stipulation may not be particularly meaningful because the efficiency gained by any AIA proceeding will be limited.” FAQs for Interim Process for PTAB Workload Management, FAQ14 (emphasis added). Western Digital has raised, and is continuing to pursue, other invalidity theories under § 101 and § 112. EX2008, *45-51. Since these invalidity theories

cannot be resolved in an IPR (35 U.S.C. § 311(b)), instituting an IPR would not resolve all the invalidity defenses at issue in the district court case and therefore not serve as a “true alternative” to the district court proceeding. *Motorola*, IPR2024-01205, Paper 19 at 3-4.

Instituting an IPR would also not reduce issues for claim construction but rather increase the number of claim construction issues between the parties. In the IPR, Petitioners proposed a construction for the term “gear” (Pet., 10), which was *not* a term the defendants identified for construction in district court. The defendants initially identified for construction the term “the gear” in claim 14 to resolve a dispute regarding antecedent basis. EX2009. Then, on April 18, 2025, the defendants dropped this term and instead identified the term “a set of predefined gears” as recited in claims 1 and 15. EX2017, *3. Petitioners’ proposed construction for “gear” in the petition is therefore a different one. Petitioners also raised new means-plus-function constructions for claims 24 and 25, which are not asserted in the district court case. *See* Pet., 10-11; EX2008, *3. The claim construction issues in the IPR are therefore different than the ones in district court.

Additionally, Petitioners in the IPR allege that “no claim term other than the terms identified below [(i.e. “gear” and the means-plus-function terms)] requires construction.” Pet., 10. However, Western Digital in the district court has identified other terms of the ’085 patent for construction. EX2009, *4; EX2017,

*3. Since the grounds do not address any of the constructions the defendants intend to present in the district court, it is unclear how instituting an IPR would help the district court resolve these disputes. To the contrary, instituting an IPR may complicate claim construction issues because Petitioners appear to be taking inconsistent positions—plain and ordinary meaning for terms in the IPR but more narrow constructions in the district court, including indefiniteness.

2. The expert declaration does not provide adequate, independent analysis that should accompany a petition.

When deciding whether to deny institution under § 314(a), the Board should also consider the substantial overlap between the petition and the expert declaration. When the declaration “merely repeats, *verbatim*, the conclusory assertion for which it is offered to support” and “does not cite to any additional supporting evidence or provide any technical reasoning to support [the] statement,” the testimony is entitled to little weight. *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (P.T.A.B. Aug. 24, 2022) (precedential); *see also* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

Petitioners submitted a declaration by Dr. Lara Dolecek to support arguments in the petition. But like the expert declaration in *Xerox*, Dr. Dolecek’s declaration merely repeats, *verbatim*, conclusory assertions in the petition.

Dr. Dolecek does not provide additional technical reasoning to support many

of the substantive statements. Some examples of Dr. Dolecek's repeating the petition (or vice versa) are provided below. Dr. Dolecek repeats, *verbatim*, the arguments from the petition. She even uses the same italicized, bolded, and underlined styling and repeats legal conclusions with verbiage lifted straight from the petition. When Dr. Dolecek's declaration varies, it merely provides longer or additional block quotations that are cited in the petition.

Petition	Dr. Dolecek Declaration
Third, as shown in FIG. 2A of Li and FIG. 2 of Cideciyan below, Li and Cideciyan are similar devices with similar objectives. Ex.1005, FIG. 2A (illustrating a flash memory based storage system with SSD controller and flash devices accessible in parallel channels), [0019] (aiming for “improvements in flash memory lifetime, reliability, performance, and/or storage capacity”); Ex.1006, FIG. 2 (illustrating a flash memory based storage system with a flash controller and flash devices accessible in parallel channels), 5:11-13 (to “provide efficient, reliable and robust solid state storage systems with exceptional overall performance”). Ex.1003, ¶96. Pet., 26.	Third, as shown in FIG. 2A of Li and FIG. 2 of Cideciyan below, Li and Cideciyan are similar devices with similar objectives. Ex.1005, Li, FIG. 2A (illustrating a flash memory based storage system with SSD controller and flash devices accessible in parallel channels), [0019] (aiming for “improvements in flash memory lifetime, reliability, performance, and/or storage capacity”); Ex.1006, Cideciyan, FIG. 2 (illustrating a flash memory based storage system with a flash controller and flash devices accessible in parallel channels), 5:11-13 (to “provide efficient, reliable and robust solid state storage systems with exceptional overall performance”). Dolecek Declaration, ¶96.
As shown in Example 1.1 of Li combined with Cideciyan (based on	As shown in Example 1.1 of Li combined with Cideciyan (based on

based on FIGS. 1, 2A of Li and FIG. 5 of Cideciyan) below, a POSITA would have reasonably expected to succeed in combining Li with Cideciyan, because Cideciyan's group-based ECC encoding/decoding is described as applicable to flash memory devices such as those taught by Li. <i>See, e.g.</i>, Ex.1006, FIG. 2. Additionally, the implementation of Cideciyan's teaching would have required only routine knowledge well within the skill of a POSITA prior to the earliest effective filing date of the '085 patent. <i>See, e.g.</i> Ex.1006, 11:55-57 ("Corresponding decoder implementations will be readily apparent to those skilled in the art from the encoder description"); 17:13-17 (describing that considerations related to grouping pages "are similar to those encountered in RAID applications as will be apparent to those skilled in the art."); Ex.1003, ¶99. Pet., 28-29.	FIGS. 1, 2A of Li and FIG. 5 of Cideciyan) illustrated below, a POSITA would have reasonably expected to succeed in combining Li with Cideciyan, because Cideciyan's group-based ECC encoding/decoding is described as applicable to flash memory devices such as those taught by Li. <i>See, e.g.</i>, Ex.1006, Cideciyan, FIG. 2. Additionally, the implementation of Cideciyan's teaching would have required only routine knowledge well within the skill of a POSITA prior to the earliest effective filing date of the '085 patent. <i>See, e.g.</i> Ex.1006, Cideciyan, 11:55-57 ("Corresponding decoder implementations will be readily apparent to those skilled in the art from the encoder description"); 17:13-17 (describing that considerations related to grouping pages "are similar to those encountered in RAID applications as will be apparent to those skilled in the art."); Dolecek Declaration, ¶99.
In further detail, Cideciyan describes "systematic encoding" is used, "whereby each codeword is produced by addition of parity symbols to the unencoded data and the data itself remains unchanged by the encoding process." Ex.1006, 10:54-56. Ex.1003, ¶105. Cideciyan describes in detail the C1 and C2 encoding process: The input data to be encoded is partitioned by controller 10	In further detail, Cideciyan describes "systematic encoding" is used, "whereby each codeword is produced by addition of parity symbols to the unencoded data and the data itself remains unchanged by the encoding process." Ex.1006, Cideciyan, 10:53-56. Cideciyan describes in detail the C1 and C2 encoding process: The input data to be encoded is partitioned by controller 10 into

into successive logical blocks each comprising a logical array of k_2 rows and k_1 columns of data symbols.... The EC1 encoder 13 systematically encodes each row in accordance with the C1 code This C1 parity code is added to the k_1 input data symbols to produce an n_1-symbol C1 codeword. ... the resulting set of k_2 C1 codewords forms a logical array of k_2 by n_1 C1-encoded symbols.... The EC2 encoder 14 systematically encodes each column in accordance with the C2 code to generate (n_2-k_2) parity symbols for that column. This C2 parity code is added to the k_2 column symbols to produce an n_2-symbol C2 codeword. Ex.1006, 10:53-11:8; Ex.1003, ¶105. Pet., 33.	successive logical blocks each comprising a logical array of k_2 rows and k_1 columns of data symbols as shown in the figure. The EC1 encoder 13 systematically encodes each row in accordance with the C1 code to generate (n_1-k_1) parity symbols for that row. This C1 parity code is added to the k_1 input data symbols to produce an n_1-symbol C1 codeword. When all k_2 rows have been encoded by the EC1 encoder, the resulting set of k_2 C1 codewords forms a logical array of k_2 by n_1 C1-encoded symbols. The C2 encoding performed by EC2 encoder 14 operates on columns of this array. The EC2 encoder 14 systematically encodes each column in accordance with the C2 code to generate (n_2-k_2) parity symbols for that column. This C2 parity code is added to the k_2 column symbols to produce an n_2-symbol C2 codeword. When all n_1 columns have been encoded by the EC2 encoder, the resulting set of n_1 C2 codewords forms a logical $(n_2$ by $n_1)$-symbol array as shown in the figure. Ex.1006, Cideciyan, 10:53-11:8. Dolecek Declaration, ¶105.
Referring to FIG. 5 below, Cideciyan	Referring to FIG. 5 below, Cideciyan

further describes storing the array of encoded symbols of FIG. 4 in the single group of pages (“stride”). Ex.1006, 11:9-11. Specifically, Cideciyan describes that <i>the region</i> (a group of pages including N pages across N channels) storing a long product code codeword (with a codelength n_1n_2), which includes C1 and C2 codewords for component codes C1 and C2. It is noted that in FIG. 5, the C2 parity symbols are stored in the N^{th} page (corresponding to CH(N)) in this group (“stride”) as an example only, and “<u>any channel could be used for the parity.</u>” Ex.1006, 11:39-42); Ex.1003, ¶106. Pet., 34.	further describes storing the array of encoded symbols of FIG. 4 in the single group of pages (“stride”). Ex.1006, Cideciyan, 11:9-11 (“The array of encoded symbols shown in the FIG. 4 is written <u>in a single stride</u>”). Specifically, Cideciyan describes that <i>the region</i> (a group of pages (“stride”) including N pages across N channels) storing C1 codewords and C2 codewords. The C1 codewords include input data symbols (<i>data payload</i>) and C1 parity symbols (<i>primary ECC parity symbols</i>), and the C2 codewords include input data symbols (<i>data payload</i>) and C2 parity symbols (<i>secondary ECC parity symbols</i>). It is noted that in FIG. 5, the C2 parity symbols are stored in the N^{th} page (corresponding to CH(N)) in this group (“stride”) as an example only, and “<u>any channel could be used for the parity.</u>” Ex.1006, Cideciyan, 11:39-42). Doleck Declaration, ¶106.
A POSITA would have found it obvious for a known technique (applying a product-code-type ECC scheme to a group of pages across the channels) improves one device (the flash-based storage system of Cideciyan) to improve similar devices (Li’s flash-based storage system) in the same way (with the benefits as taught by Cideciyan), using the prior art elements according to their established functions. Ex.1003, ¶116; <i>Intel Corp.</i>,	A POSITA would have found it obvious for a known technique (applying a product code ECC scheme to a group of pages across the channels) improves one device (the flash based storage system of Cideciyan) to improve similar devices (Li’s flash memory based storage system) in the same way (with the benefits as taught by Cideciyan), using the prior art elements according to their established functions.

61 F.4th at 1380–81. Pet., 39.	Dolecek Declaration, ¶116.
Additionally , the results of the proposed combination would have been predictable and a POSITA would have had a reasonable expectation of success, because the combination of Li and Cideciyan merely applies known technique to a known device (Li’s flash memory based storage system implementing adaptive ECC schemes) to yield the predictable results of “efficient, reliable and robust solid state storage systems with exceptional overall performance.” Ex.1006, 5:11-13; Ex.1003, ¶118. Pet., 40-41.	Additionally , the results of the proposed combination would have been predictable and a POSITA would have had a reasonable expectation of success, because the combination of Li and Cideciyan merely applies known technique to a known device (Li’s flash memory based storage system implementing adaptive ECC schemes) ready for improvement to yield the predictable results of “efficient, reliable and robust solid state storage systems with exceptional overall performance.” Ex.1006, Cideciyan, 5:11-13. Dolecek Declaration, ¶118.
The claim analysis for Ground 2 is similar to that of Ground 1, with the additional analysis below explaining that Li combined with Cideciyan and Frost renders [1.1.1] of Claim 1 obvious. See supra X.E; Ex.1003, ¶235. Pet., 76.	The claim analysis for Ground 2 is substantially the same as that of Ground 1, with the additional analysis below explaining that Li combined with Cideciyan and Frost renders [1.1.1] of Claim 1 obvious. See analysis in Ground 1. Dolecek Declaration, ¶236.

Interestingly, Dr. Dolecek’s declaration follows the same formatting and verbiage as a declaration from a different expert (Dr. Paul Min), which was filed by the same law firm. *SanDisk Technologies, Inc. et al. v. Polaris PowerLED Techs., LLC*, IPR2025-00517, Exhibit 1003 (P.T.A.B. Jan. 24, 2025).

The lack of supporting evidence and additional technical reasoning in Dr. Dolecek's declaration is yet another reason why the Board should deny institution. The standard for what qualifies as independent expert testimony and its use within IPRs should be higher; the declaration should not merely "cop[y], word-for-word, Petitioner's conclusory assertions." *Xerox*, IPR2022-00624, Paper 9 at 5. When it does, the Board should deny institution.

3. The '085 patent issued nearly a decade ago.

Under the interim process, the Director can consider "[s]ettled expectations of the parties, such as the length of time the claims have been in force" when deciding whether to exercise discretion to deny institution. Interim Processes for PTAB Workload Management at 2 (Mar. 26, 2025). Here, the '085 patent issued on November 10, 2015—over nine years ago. Had Petitioners objected to the issuance of the '085 patent, they could have raised challenges many years ago. 35 U.S.C. §§ 302 (permitting any person at any time to file a request for reexamination), 321 (permitting post-grant review challenges up to 9-months after issuance). SanDisk could have also challenged the validity of the '085 patent after becoming aware of it at least as early as April 11, 2016. EX2015, *13 (in a SanDisk application, an examiner citing the '085 patent in a Notice of References Cited on April 11, 2016); EX2016, (56) (citing the '085 patent). Instead, Petitioners waited many years to challenge the '085 patent—after Polaris relied on

the issued claims in its complaint for patent infringement. This extended delay in challenging the claims also favors denying institution.

4. PTAB resources are better spent on *ex parte* appeals.

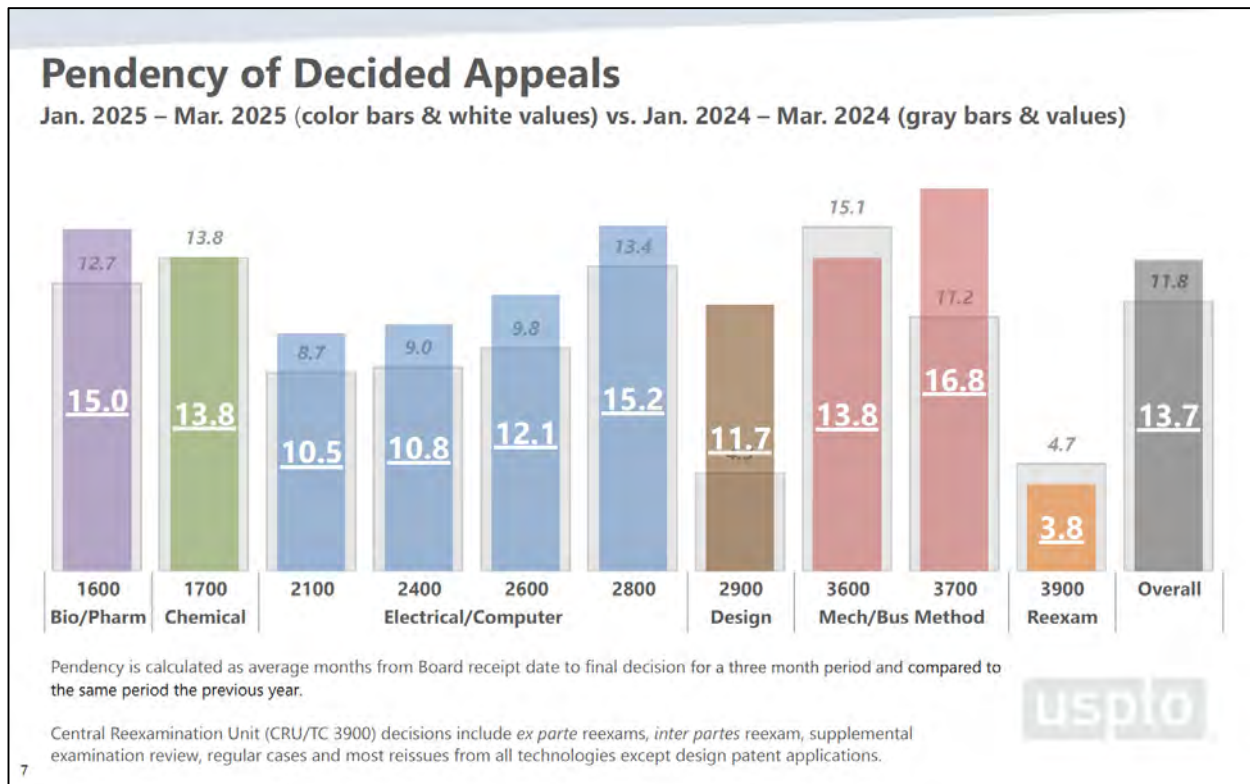
The Board should also deny institution because its limited resources are better spent on the growing backlog of *ex parte* appeals. In 35 U.S.C. § 6(b)(1), the Board is tasked with “review[ing] adverse decisions of examiners upon applications for patent pursuant to section 134(a).” Congress also tasked the Board with reviewing appeals of reexaminations, derivation proceedings, IPRs, and PGRs. 35 U.S.C. § 6(b)(2)-(4). But current Office policy is to focus on *ex parte* appeals: “To ensure that the PTAB continues to meet its statutory obligations as to *ex parte* appeals, while continuing to maintain its capacity to conduct AIA proceedings, the Director will exercise her discretion on institution of AIA proceedings” Interim Processes for PTAB Workload Management at 1 (Mar. 26, 2025). The Board should exercise that discretion here because the pendency of *ex parte* appeals has increased (EX2012, 7), nearly a quarter of *ex parte* appeals have been pending more than eleven months (EX2013), and the backlog is growing month-over-month in almost all technology centers (EX2012, 4).

According to the latest data published by the USPTO, roughly a quarter of

all *ex parte* appeals have been pending for over eleven months. EX2013.⁷ In 2025, the pendency has increased in almost every technical center. Shown below, the time (in months) to a final decision has increased in 2025 (shown with the color bars and white values) compared to the same data from 2024 (shown with the gray bars and gray values). For the technology center of the '085 patent—2100⁸—the pendency has increased from 8.7 months to 10.5 months, a 20.7% increase.

⁷ The latest data on the PTAB Dashboard is from November 2023. However, the data from FY24 and FY25 also indicates that a substantial number of cases have been pending for over eleven months.

⁸ The '085 patent describes systems and methods for adaptively selecting from error correction coding schemes in a flash drive. Patents for “Memory Access and Control” are under 2130 and patents for “Computer Error Control, Reliability, & Control Systems” are under 2110, both of which are within tech center 2100 (Computer Architecture Software and Information Security).



EX2012, 7.

In the current fiscal year (FY25), the PTAB's backlog of *ex parte* appeals in the 2100 technology center has also increased. Shown below, in FY25, the PTAB's starting inventory of *ex parte* appeals in the technology center 2100 was 367 cases. EX2012, 4. In FY25 (October 2024 through March 2025), 225 appeals have been filed, whereas the PTAB decided 181 appeals. *Id.* This has increased the backlog for technology center 2100 by 12% (44 cases)—the highest increase in number of cases outstanding for any technology center during FY25. *See id.*

Receipts & Dispositions (Fiscal Year through Mar. 31, 2025)												
Technology Center	Starting Inventory	Appeals Filed	Affirmed	Affirmed -in-Part	Reversed	Panel Remand	Admin Remand	Dismissed	Appeals Decided	Ending Inventory	Inventory Change	% of Inventory
1600	442	191	125	8	66	0	0	7	206	427	▼ -15	9.3%
1700	843	330	210	28	102	0	0	4	344	829	▼ -14	18.1%
2100	367	225	108	22	46	0	3	2	181	411	▲ 44	9.0%
2400	323	164	90	20	47	0	0	0	157	330	▲ 7	7.2%
2600	257	135	69	7	19	0	0	0	95	297	▲ 40	6.5%
2800	346	149	71	14	56	0	0	0	141	354	▲ 8	7.7%
2900	28	5	16	0	4	0	0	0	20	13	▼ -15	0.3%
3600	1,072	384	417	22	89	0	1	1	530	926	▼ -146	20.2%
3700	951	356	183	51	88	0	1	2	325	982	▲ 31	21.4%
3900 (Ex Parte)	12	23	13	0	4	0	1	0	18	17	▲ 5	0.4%
3900 (Sup. Exam)	0	0	0	0	0	0	0	0	0	0	— 0	0.0%
3900 (Reissue)	7	12	10	0	5	0	0	0	15	4	▼ -3	0.1%
3900 (Regular)	2	0	0	0	0	0	0	0	0	2	— 0	0.0%
Board Total	4,650	1,974	1,312	172	526	0	6	16	2,032	4,592	▼ -58	100.0%

% Decisions					
Affirmed	Affirmed-in-Part	Reversed	Panel Remand	Admin Remand	Dismissed
64.6%	8.5%	25.9%	0.0%	0.3%	0.8%

EX2012, 4 (annotated).

To reduce the average time to final decision, the 411 currently pending *ex parte* appeals in technology center 2100, the 12% backlog growth in the 2100 technology center during FY25, and the 4,592 currently outstanding *ex parte* appeals overall, the PTAB should focus its efforts on the pending *ex parte* appeals—not this IPR, especially since the district court is already scheduled to adjudicate validity months *before* the Board reaches its final decision.

In total, the other considerations also favor discretionary denial.

III. CONCLUSION

Litigating the same or similar issues at the Board as the issues that are already scheduled to get resolved in the district court would be duplicative and contrary to the intent of IPRs for “providing a more efficient system for challenging patents” and “reducing unwarranted litigation costs.” H.R. Rep. No. 112-98 at 39-40 (2011); *see also NHK Spring*, IPR2018-00752, Paper 8 at 19-20. The Board’s limited resources would be better spent elsewhere.

Respectfully submitted,

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Case IPR2025-00515
U.S. Patent No. 9,183,085

CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

1. This Patent Owner's Brief on Discretionary Denial complies with the type-volume limitation of 14,000 words, comprising 7,439 words, excluding the parts exempted by 37 C.F.R. § 42.24(a)(1).

2. This Patent Owner's Brief on Discretionary Denial complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word 2016 in 14-point Times New Roman font.

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Case IPR2025-00515
U.S. Patent No. 9,183,085

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

I certify that the above-captioned **PATENT OWNER'S BRIEF ON DISCRETIONARY DENIAL** and associated Exhibits 2001-2017 were served in their entireties on April 25, 2025, upon the following parties via electronic mail:

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24663644

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND
WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

POLARIS POWERLED TECHNOLOGIES, LLC,

Patent Owner.

IPR2025-00515
U.S. Patent No. 9,183,085

**PETITIONER'S OPPOSITION TO PATENT OWNER'S
REQUEST FOR DISCRETIONARY DENIAL**

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Opposition to Patent Owner’s Request for Discretionary Denial
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I. Introduction

Petitioner respectfully requests that the Director decline to exercise her discretion to deny institution and advance the Petition to a merits panel for consideration.

Petitioners Western Digital Technologies, Inc. and Sandisk Technologies Inc. (together “Petitioner”) oppose Patent Owner’s Request for Discretionary Denial (Paper 9, “PO Brief”). The *Fintiv* factors and the additional factors set forth in the Acting Director’s “Interim Processes for PTAB Workload Management” (“Director Memo”), considered as a whole, do **not** warrant denial—the parallel litigation has been stayed at an early stage of the case pending the resolution of the IPR.

With respect to *Fintiv*, five of the six *Fintiv* factors strongly weigh against denial. Because the parallel litigation has been stayed, this IPR is a “true alternative” to the parallel litigation in view of Petitioner’s “*Sotera*” stipulation.

The additional factors listed in the Director Memo similarly weigh against denial. Petitioner has a compelling interest in having access to cost-effective PTAB review when accused of infringement by entities that do not manufacture or innovate. Patent Owner (Polaris PowerLED) has no compelling interest or expectation sufficient to avoid PTAB review, because unlike the original owner of the ’085 patent, Patent Owner is an assertion entity who appears to have acquired

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the patent three years ago solely for the purpose of litigation—which changes everything with respect to settled expectations. Further, the Petition does not rely on expert testimony for gap-filling any claim elements. Instead, all claim elements are shown in the printed publication prior art, and the petition relies upon expert testimony to the extent necessary under Federal Circuit precedent to show how a POSITA would read and understand these references.

This IPR is one of three IPRs challenging three patents asserted in the stayed parallel litigation. Ex.1036, 1. These three patents are from different families and address three distinct and well-established technologies associated with memory systems respectively: Error Correcting Coding (ECC), redundant array of independent disks (RAID), and interrupt handling. Therefore, they are better suited for PTAB review, where the Board's technical expertise is well-suited to assess the distinctions and technical details of the asserted claims and the prior art presented in the obviousness grounds. The District Court in the parallel litigation agrees, having stayed the litigation so that the PTAB can handle this accordingly.

II. Discretionary denial under *Fintiv* is not warranted.

The *Fintiv* factors, considered as a whole, do **not** warrant denial. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential). Every factor either favors institution or is neutral.

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A. Factor 1 weighs strongly against denial: A stay was granted.

The parallel Litigation “is still in early stages of litigation” and has been stayed. EX1036, 4. The Court granted Petitioner's Motion to Stay Pending IPRs on June 24, 2025. *Id.*, 1. The stay remains in effect pending resolution of the IPR proceedings. With the parallel litigation stayed, this IPR is a true alternative to district court litigation. Thus, this factor strongly weighs against denial.

B. Factor 2 weighs strongly against denial: The parallel litigation was stayed.

While the scheduling originally indicated a trial date around the same time as the projected Final Written Decision (“FWD”), this previously scheduled trial date, together with other scheduled dates, was “**VACATED** and taken off the calendar.” Ex.1036, 9. No trial date is scheduled.

Accordingly, Factor 2 weighs strongly against denial in view of the stay in the parallel litigation.

C. Factor 3 weighs strongly against denial: Minimal relevant investment and diligent filing.

Factor 3 strongly weighs against discretionary denial because, at institution, investment by the court and parties will have been minimal as to the activities pertinent to *Fintiv*. Patent Owner's Request for Discretionary Denial includes a laundry list of activities allegedly showing substantial investment, but very few relate to invalidity of the '085 patent. See PO Brief, 7-11. Under *Fintiv*, “[i]f, at the

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time of the institution decision, the district court has not issued orders ***related to the patent at issue in the petition***, this fact weighs against exercising discretion to deny institution.” *Fintiv*, 10. Not only is there no order, no claim construction briefing had been done. The Court confirms the early stages of parallel litigation: “the case is in its ***early*** stages and there is still more work ahead of the parties and the Court than behind them.” Ex.1036, 4 (citations omitted, emphasis added).

This factor also weighs against denial because the Petitioner worked diligently to file the instant petition after receiving Patent Owner's infringement contentions and diligently filed the now-grated motion for stay. *Fintiv*, 11. Petitioner received Plaintiff's infringement contentions on October 2, 2024 (Ex.1026), and worked diligently to file three IPR petitions, including the instant petition, ***within four months***. At the time of the filing, the parallel litigation was in its early stages and claim construction briefing had yet to begin. The Board has recently agreed that similar diligence is reasonable and weighs against denial. See *Samsung Elecs. Co., Ltd. v. Mullen Industries LLC*, IPR2024-01472, Paper 9 at 10 (Mar. 31, 2025) (“Petitioner's diligence in filing its Petition (a) less than five months after receiving Patent Owner's infringement contentions and (b) prior to the parties briefing claim construction issues weighs against exercising discretionary denial.”).

Accordingly, Factor 3 strongly weighs against denial.

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D. Factor 4 weighs strongly against denial: Petitioner's "Sotera" stipulation.

Factor 4 weighs strongly against denial. First, the Court, in staying the parallel litigation, explained the benefits of PTAB review, including simplification of issues and trial in the parallel litigation. The Court reasoned that there is "a likelihood that the outcome of the [IPR] could eliminate the need for trial if the claims are cancelled or, if the claims survive, facilitate trial by providing the court with expert opinion of the [Patent and Trial Office] and clarifying the scope of the claims." EX1036, 6 (citations omitted). And "[i]f the PTAB cancels or narrows a portion of the asserted claims, the scope of this litigation may be significantly reduced." Ex.1036, 5 (citations omitted).

Second, Petitioner has made a *Sotera* stipulation in district court. See Ex.1022 (stipulation filed in parallel district court proceeding). Specifically, Petitioner stipulated that:

[I]f the PTAB institutes an IPR in response to Defendant's petition against Plaintiff's U.S. Patent No. 9,183,085 (IPR2025-00515), Defendant will not pursue in this litigation against the claims challenged in IPR2025-00515, (i) the specific grounds raised in IPR2025-00515, or (ii) any other grounds that could have reasonably been raised before the PTAB in that instituted proceeding (i.e., any ground that could have reasonably been raised under §§ 102 or 103 on the basis of prior art patents or printed publications).

Ex.1022, 1-2.

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Petitioner's *Sotera* stipulation was timely under the procedures in place when the petition was filed. At the time of filing on January 29, 2025, PTAB precedent provided that the "appropriate time for a petitioner to offer a stipulation related to the *Fintiv* factor 4 analysis is prior to the Board's decision of whether to institute review." *NXP USA, Inc. v. Impinj, Inc.*, IPR2021-01556, Paper 13 at 4 (Sept. 7, 2022) (de-designated precedential Apr. 25, 2025); *see also Nike, Inc. v. ADIDAS AG*, 955 F.3d 45, 52 (Fed. Cir. 2020) ("In interpreting the APA's notice provisions in the context of IPR proceedings, we have cautioned that an agency may not change theories in midstream without giving respondents reasonable notice of the change and the opportunity to present argument under the new theory.") (citation and quotation marks omitted).

Patent Owner argues that this stipulation is "too late" under the procedures defined in the FAQs. PO Brief, 13. The FAQs state: "A petitioner should file a *Sotera* or *Sand* stipulation as soon as practicable, so that a patent owner may address the impact of the stipulation in its discretionary denial brief." Ex.1024, FAQ 14. Petitioner filed this *Sotera* stipulation as soon as practicable on April 28, 2025—three days after the FAQs were issued. In an apparent attempt to preclude consideration of a stipulation, Patent Owner filed their brief on April 25, 2025—almost one month before their due date of May 24, 2025. Had Patent Owner filed on their actual due date, Patent Owner would have had nearly one month to

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consider and brief the *Sotera* stipulation—provided there is anything to be said.

Patent Owner's early filing should not preclude consideration of Petitioner's *Sotera* stipulation. And Patent Owner had ample opportunity to brief the expected *Sotera* stipulation in their discretionary denial brief or any supplemental briefing they could have asked for.

This case is distinguishable from the *Motorola Solutions* case cited by Patent Owner. PO Brief, 14. In *Motorola Solutions*, the Director found that the *Sotera* stipulation did not outweigh the substantial investment in the district court proceeding, where “the parties had served extensive infringement and invalidity contentions, served opening and rebuttal expert reports, filed claim construction briefs, and conducted several deposition,” and the “court also had held a claim construction hearing and construed the disputed claim terms,” before the litigation was stayed after institution. *See Motorola Solutions, Inc. v. Stellar, LLC*, IPR2024-01205, Paper 19 at 3-4 (P.T.A.B. Mar. 28, 2025). In contrast and as noted by the judge, “[t]his case is still in early stages of litigation.” Ex.1036, 4. Accordingly, Petitioner's *Sotera* stipulation weighs strongly against denial.

Also strongly weighing against denial under Factor 4 is that Petitioner's challenge encompasses a significantly broader range of claims compared to the litigation. The Petition challenges **twenty** claims (1-2, 4-7, 14-18, 22-25, and 29-33), but only **six** claims (1, 2, 4, 14, 15, 16) are currently asserted against Petitioner

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in the parallel litigation (i.e., 70% of the challenged claims in the IPR are **not** asserted in the parallel litigation). And only those six asserted claims (1, 2, 4, 14, 15, 16) are the subject of Petitioner's invalidity contentions on the parallel litigation. *See* Ex.2008, 1 (asserting invalidity "**only to the asserted claims identified by Polaris in its Infringement Contentions.**"). Petitioner elected to challenge additional, unasserted claims for efficiency reasons—for example, to avoid filing a second IPR in the event Patent Owner asserts additional claims in the parallel litigation.

These additional challenged (but unasserted) claims differ in claim scope from the asserted claims, meaning that key issues in the petition will not be resolved by the district court—further reducing the degree of overlap under Factor 4. *See Fintiv*, 13 (examining whether the district court will “resolve key issues in the petition”). In particular, construction of means-plus-function claim terms only pertain to **unasserted** claims 24-25, which does not apply to asserted claims. As such, this key issue of construction of means-plus-function claim terms is specific to this IPR and will not be resolved by the district court.

Petitioner's *Sotera* stipulation also moots Patent Owner's argument that “Petitioners appear to have strategically omitted the defendant Western Digital Corporation—the parent corporation of Western Digital Technologies, Inc.—from the petition to evade estoppels.” PO Brief, 15. Western Digital Corporation has

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explicitly agreed to be bound by Petitioner's *Sotera* stipulation. Ex.1022, 1.

Additionally, Western Digital Corporation has explicitly "agree[d] to be bound by the estoppel effect of the IPRs" in its Reply for Motion to Stay. Ex.2011, 2

("Western Digital Corporation agrees to be bound by statutory estoppel ***to the same extent as Western Digital Technologies***"). Western Digital Corporation's agreement to be bound by estoppel effect of the IPR is not conditioned upon the stay being granted. Western Digital Corporation is thus not "evad[ing] estoppel" as Patent Owner argues. PO Brief, 15; EX1036, 6.

Accordingly, Factor 4 weighs strongly against denial because of (i) Petitioner's *Sotera* stipulation and (ii) key issues in the Petition that will not be resolved by the district court.

E. Factor 5 is neutral: Petitioner is a defendant in the parallel litigation.

Petitioner Western Digital Technologies, Inc. is a defendant in the parallel litigation. That is true of most IPR petitioners, making this factor neutral. *See HP Inc. v. Slingshot Printing LLC*, IPR2020-01084, Paper 13 at 9 (Jan. 14, 2021); *see also NVIDIA Corp. v. Invensas Corp.*, IPR2020-00603, Paper 11 at 23 (Sept. 3, 2020) (this factor weighs against discretionary denial where the district court trial and IPR final written decision are expected "around the same time").

F. Factor 6 weighs strongly against denial: The merits of the Petition are particularly strong.

Factor 6 favors institution because the Petition plainly shows that the

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challenged claims of the '085 patent claims are unpatentable. In its PO Brief, Patent Owner does not raise any specific merits arguments other than stating that it will present merits arguments in its Patent Owner Preliminary Response (POPR). However, as discussed in detail below at III.A, Patent Owner's merits arguments in its POPR do not hold up under scrutiny, and indeed, provide admissions supporting the claimed method's invalidity at least during one or more "operating period[s]" of a flash memory device. See POPR, 5. Thus the merits of the Petition are particularly strong, weighing against denial.

G. The *Fintiv* factors as a whole weigh strongly against denial.

In summary, each *Fintiv* factor is either neutral or weighs strongly against denial:

Factor	Weight	Reason
1 (stay)	strongly against denial	a stay has been granted
2 (trial gap)	strongly against denial	a stay has been granted and thus there is no scheduled trial date
3 (investment)	strongly against denial	parallel litigation in early stages, no court orders regarding invalidity of the '085 patent
4 (overlap)	strongly against denial	<i>Sotera</i> stipulation; key issues not resolved by district court
5 (same party)	neutral	Petitioner is defendant
6 (merits)	strongly against denial	Strength of the invalidity challenge is particularly strong, POPR admits invalidity during at least some operating period(s)

In light of all the *Fintiv* factors as a whole, the Director should not

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discretionarily deny institution under §314(a).

III. The additional factors set forth in the Memorandum favor institution.

The Director Memo invites the parties to “address all relevant [discretionary denial] considerations” and provides a list of potential factors. Director Memo, 2-3.

Each of the potential factors favors institution:

- The unpatentability challenges in the Petition are particularly strong given that the prior art shows the same error correction coding techniques that are claimed.
- The Petition relies upon expert testimony to the extent necessary under Federal Circuit precedent, and such expert testimony is supported by evidence as required under 37 CFR § 42.65 and *Xerox*.
- Patent Owner cannot reasonably allege settled expectations regarding the '085 patent based on a few years of ownership and the lack of any post-issuance validity challenge.
- Neither the PTAB nor another forum has adjudicated the validity of the '085 patent.
- Patent Owner does not allege that any changes in the law or new judicial precedent issued since issuance of the claims affects patentability.
- The United States has a compelling economic and national security interest in ensuring Sandisk and Western Digital, leading domestic technology innovators, have access to efficient AIA proceedings when faced with meritless lawsuits by non-practicing entities.

Several of these factors are of particular importance to the Director's

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discretion and are addressed individually below.

A. The merits of the Petition are particularly strong, and POPR admits invalidity during at least some operating period(s).

The '085 patent should not have issued because it claims no more than well-known concepts related to the adaptive error correcting coding, or "ECC" described and claimed in the '085 patent. *See* Ex.1001, 48:47. The '085 patent is thus one of the patents Congress referred to when discussing the purpose of the America Invents Act—"improving patent quality and providing **a more efficient system for challenging patents that should not have issued.**" House Report (H.R. Rep. 112-98, 2011), 39-40.

As stated in the Petition, the '085 patent was allowed after amending the claims to cover the concept in which an adaptive ECC technique is applied to a region, where "the two or more flash memory pages of a region can be read simultaneously." Ex.1001, 61:1-3; Ex.1002, 693-705, 715-719; Petition, 9.

However, it was already known to apply adaptive ECC techniques in this manner. The Li reference describes "***adaptive ECC techniques*** for flash memory based data storage." Ex.1005, Title, [0131]; Pet. 13-14. And the Cideciyan reference shows that it was known to apply adaptive ECC technique to a region including a fixed number of pages accessible in parallel. Ex.1006, FIG. 2, 8:53-64, 11:44-46; Pet. 14-15. Such a well-known technique is further confirmed by Frost,

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which describes how data in a particular region accessible in parallel can be read

“at the same time.” Ex.1007, Title, 6:46-67; Pet. 16.

Patent Owner's merits arguments in its POPR do not hold up under scrutiny, and indeed, provide admission to support that the claimed method is invalid at least during some operating period(s) of a flash memory. See POPR, 5. Specifically, Patent Owner argues that the prior art may perform multiple operation periods, and *one* of the operation periods may not teach the claimed method. The petition showed that a single operating period of the prior art reads on the claims, so even if this argument were correct¹ (which is not and contradicts with prior art's express disclosure), this is Patent Owner's admission that the claimed method is invalid during at least other operating period(s) of a flash memory device. *Id.* That is, the Patent Owner admits that the claimed method is invalid at least during some

¹ Patent Owner's argument is indeed incorrect, and is conclusory and contradicts the prior art's express disclosure that memory pages may operate with the same cell version (e.g., single-level-cell (SLC)) during the entire life of the flash memory device. See *e.g.*, Ex.1005, Li, [0107] (“In various embodiments and/or usage scenarios, under particular circumstances a page is operated as an SLC page ***irrespective of*** error correcting code selection.”).

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operating period(s).

Thus, Petitioner respectfully requests that the Director pass this case to a merits panel and requests that the Board institute trial.

B. The Petition properly relies on expert testimony

The Petition's compliance with Federal Circuit precedent should not be a reason for discretionary denial. And Dr. Dolecek's opinions are fully supported by the evidence of record.

1. Federal Circuit precedent requires that the Petition rely on expert testimony.

Petitioner's reliance on expert testimony as required by Federal Circuit precedent should not be a reason for discretionary denial. The foundational decisions upon which patent law is based—*Phillips*, *KSR*, etc.—require the adjudicator to evaluate the patent and prior art from the perspective of a POSITA. That perspective is established with evidence, often in the form of expert declarations. Attorney argument is insufficient.

It is well established that patent claims are construed based on the understanding of a POSITA. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (“We have made clear, moreover, that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the

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effective filing date of the patent application.”) (*citing Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004) (“A court construing a patent claim seeks to accord a claim the meaning it would have to a person of ordinary skill in the art at the time of the invention.”)); *Home Diagnostics, Inc. v. LifeScan, Inc.*, 381 F.3d 1352, 1358 (Fed. Cir. 2004) (“customary meaning” refers to the “customary meaning in [the] art field”); *Ferguson Beauregard/Logic Controls v. Mega Sys., LLC*, 350 F.3d 1327, 1338 (Fed. Cir. 2003) (claim terms “are examined through the viewing glass of a person skilled in the art”); *see also PC Connector Solutions LLC v. SmartDisk Corp.*, 406 F.3d 1359, 1363 (Fed. Cir. 2005) (meaning of claim “must be interpreted as of [the] effective filing date” of the patent application); *Schering Corp. v. Amgen Inc.*, 222 F.3d 1347, 1353 (Fed. Cir. 2000) (same)).

Obviousness grounds are likewise evaluated from the perspective of a POSITA. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007) (“If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.”), 418 (“[I]t can be important to identify a reason that would have prompted a person of ordinary skill in the

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relevant field to combine the elements in the way the claimed new invention

does.”), 421 (“A person of ordinary skill is also a person of ordinary creativity, not an automaton.”).

The Federal Circuit has also made it clear that attorney argument alone is not evidence and should be given little weight. *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1043 (Fed. Cir. 2017) (“Attorney argument is not evidence.”) (citing *Gemtron Corp. v. Saint-Gobain Corp.*, 572 F.3d 1371, 1380 (Fed. Cir. 2009) (“[U]nsworn attorney argument . . . is not evidence and cannot rebut . . . other admitted evidence . . .”)); see also *Elbit Sys. Of Am., LLC, v. Thales Visionix, Inc.*, 881 F.3d 1354, 1359 (Fed. Cir. 2018) (“Elbit fails to present any evidence supporting this contention beyond attorney argument . . . and ‘[a]ttorney argument is not evidence’ and cannot rebut other admitted evidence.”).

Because attorney argument is not evidence, expert testimony is *necessary* to properly support a petition's claim construction and obviousness positions, which are evaluated from the perspective of a POSITA. This is precisely how the Petition presents and uses the testimony of Dr. Dolecek. See *generally* Petition, 13-84 (relying on testimony of Dr. Dolecek to support obviousness grounds). The unpatentability grounds set forth in the Petition are fully supported by the references themselves—Dr. Dolecek's testimony serves to confirm, support, and explain the disclosures of the references from the perspective of a POSITA. See

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generally Ex.1003. Patent Owner does not dispute that Dr. Dolecek was a POSITA as of the critical date of the '085 patent. Ex.1003, ¶¶6-18.

Further, Dr. Dolecek's testimony is supported by corroborating evidence in the form of the disclosure of the references relied upon in the unpatentability grounds (e.g., Ex.1005, Ex.1006, Ex.1007, Ex.1008) and many tertiary references (e.g., Ex.1009, Ex.1010, Ex.1011, Ex.1012, Ex.1013, Ex.1014, Ex.1018, Ex.1019, Ex.1020). *See generally*, Ex.1003. Further still, Dr. Dolecek repeatedly provides technical reasoning to support her statements and understandings of the references. *See generally*, Ex.1003.

Further, the Federal Circuit has recognized that "when the technology is complex and 'beyond the comprehension of laypersons,' expert testimony is 'sometimes essential.'" *Synopsys, Inc. v. Mentor Graphics Corp.*, 814 F.3d 1309, 1320 (Fed. Cir. 2016) (internal quotations removed); *see also Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1330 (Fed. Cir. 2009) ("If the relevant technology were complex, the court might require expert opinions."). This is precisely the situation here. Dr. Dolecek's expertise is utilized to explain the technical background of complicated concepts relevant to the '085 patent (*see, e.g.*, Ex.1003, ¶¶25-46). Dr. Dolecek also provides detailed explanations regarding how a POSITA would have understood the technical descriptions found in the '085 patent and the prior art references (*see, e.g.*, Ex.1003, ¶¶47-263). Dr. Dolecek's

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testimony serves these essential purposes and is a strength of the Petition.

2. Patent Owner's arguments based upon Xerox are misplaced.

Patent Owner argues that “Dr. Dolecek’s declaration merely repeats, verbatim, conclusory assertions in the petition.” PO Brief, 21 (citing *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15-17 (August 24, 2022) (precedential)). *Xerox*, however, does not stand for the proposition that a Petition and supporting declaration cannot be similar. *Xerox* instead focuses on whether the expert testimony cites to “supporting evidence or provide[s] any technical reasoning.” *Xerox*, 15. Expert testimony is only afforded less weight if it “adds little to the conclusory assertion for which it is offered to support.” *Id.* Here, Dr. Dolecek’s analysis is fully supported by evidence, and does not rely on improper gap filling. Accordingly, the Petition’s proper reliance on expert testimony to support the unpatentability grounds favors institution.

C. No “settled expectations.”

Patent Owner has no compelling interest or expectation sufficient to avoid PTAB review because they only acquired the ’085 patent three years ago and they appear to have done so solely for the purpose of litigation. The issue date of a patent should not be a reason for discretionary denial. Patent Owner notes that “the ’085 patent issued on November 10, 2015—over nine years ago.” PO Brief, 27. But as a non-practicing entity, Patent Owner cannot claim it has any settled

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expectations arising from practicing the '085 patent. Patent Owner appears to have acquired the '346 patent in 2022 solely for the purpose of attempting to monetize it through litigation, significantly decreasing any potential relevance of this factor. See Ex.1025, 1 (assignment showing transfer to Polaris in August of 2022).

Moreover, Patent Owner has not made any meaningful attempt at engaging with Petitioner for licensing discussions. Instead, Patent Owner filed a complaint asserting the '085 patent against Petitioner only seven days after sending a notice letter, which predictably triggered this IPR challenge. Ex.1037, ¶45. The '085 patent is not entitled to immunity from IPR review. And regarding expectations of validity, no tribunal has ever adjudicated the validity of the '085 patent after it issued.

Accordingly, the lack of settled expectations weighs strongly against denial.

D. The PTAB has sufficient resources to handle IPR proceedings and ex parte proceedings.

The Board's statutorily defined tasks of handling both *ex parte* appeals and post-grant proceedings should not be a reason for discretionary denial. Patent Owner argues that the Board's "limited resources are better spent on the growing backlog of *ex parte* appeals." PO Brief, 28. Patent Owner further notes that the *ex parte* appeal backlog has increased. *Id.*

But Patent Owner has not provided any evidence to show that the Board cannot handle both its *ex parte* appeal docket and its post-grant proceeding docket.

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Nor could they, given that the Board has recently publicly acknowledged that

“[w]e do have enough staff so we can handle both the appeals and the trials with the judges and staff on board.” Ex.1040, 1. Accordingly, the existence of an *ex parte* appeal docket (increasing or not) is not a reason to discretionarily deny this specific case.

E. Compelling economic and national security interests favor institution.

Petitioners Western Digital and Sandisk together play a multifaceted role in bolstering the US economy. As a leading provider of digital storage solutions, the companies drive significant revenue generation—with billions in annual sales that not only bolster its own financial health but also support a vast network of suppliers, service providers, and ancillary industries. Ex.1038, 4 (“Western Digital is a leading developer, manufacturer and provider of data storage devices and solutions based on both hard disk drive and NAND flash technologies. With a differentiated innovation engine driving advancements in storage and semiconductor technologies, our broad and ever-expanding portfolio delivers powerful hard disk drives (‘HDD’) and flash-based products (‘Flash’) storage solutions for everyone from students, gamers and home offices, to the largest enterprises and public clouds to capture, preserve, access and transform an ever-increasing diversity of data.”). This economic activity injects substantial funds into local communities through payrolls, tax revenues, and the multiplier effects that

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come with a robust manufacturing and technology ecosystem.

Moreover, Western Digital's and Sandisk's contributions extend to their impact on job creation and workforce development. With operations that span manufacturing, research and development, and engineering, the companies create skilled job opportunities and support local communities by fostering a demand for specialized talent. In doing so, they energize the broader US technology sector—promoting innovation in digital storage technologies that underpin critical infrastructure like data centers, cloud computing services, and enterprise IT systems. This technological backbone not only facilitates business operations nationwide but also reinforces American leadership in the rapidly evolving digital age. This type of advanced domestic engineering capacity is critical to U.S. economic interests.

The United States thus has a compelling economic and national security interest in providing Western Digital and Sandisk an opportunity to challenge the '968 patent under the more efficient IPR framework. As leading American technology companies, it is critical that Western Digital and Sandisk have the ability to invest and innovate without being encumbered by invalid patents. Petitioner's right to seek review of such patents by the U.S. Patent and Trademark Office is similarly critical.

It is vital that companies like Western Digital and Sandisk are provided an

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effective and efficient mechanism for challenging invalid patents asserted against them. Congress created the AIA for this purpose. 77 F. Reg. No. 157, 48612 (Aug. 14, 2012) (“The purpose of the AIA ... is to establish a more efficient and streamlined patent system that will improve patent quality and limit unnecessary and counterproductive litigation costs.”); *see also General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 16-17 (Sept. 6, 2017) (“[W]e recognize that an objective of the AIA is to provide an effective and efficient alternative to district court litigation.”). AIA proceedings create cost savings for its participants via “reductions in legal fees incurred and the greater probability of a settlement or early-stage resolution.” Ex.1041 (study of AIA economic benefits), 2, 8 (“[T]he total economic benefits of *inter partes* reviews resulting in stay of litigation in district court included **an increase in US business activity of \$1.87 billion in gross product and 8,530 job-years of employment**”; “In situations where an *inter partes* review was conducted parallel to a district court proceeding, the economic benefits of [*inter partes* reviews] include estimated **increases of \$135.4 million in US gross product and 617 person-years of employment**”).

Petitioners Western Digital and Sandisk are seeking review of the '085 patent consistent with the purpose of AIA post-grant proceedings: an efficient, technically reliable assessment of validity. And Petitioner's *Sotera* stipulation

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demonstrates that it desires a true district court alternative. Denying Petitioners access to IPR in this scenario would frustrate the purpose of the AIA and deny Petitioner the specific economic benefits envisioned by Congress.

These economic interests are particularly compelling as Petitioners have been accused of infringement by a non-practicing entity, Polaris. For these reasons, compelling economic and national security interests favor institution.

IV. The new Interim Process should not govern the decision to institute.

Petitioner respectfully requests that the USPTO Director maintain the standards for institution that were in place when this Petition was filed. While the briefing above addresses the new Interim Process as best understood by Petitioner, this IPR should be governed by the procedures that were in place when it was filed, as in the June 21, 2022 Interim Procedure for Discretionary Denials issued by the Office (the "June 2022 Procedures").

Since the Petition was filed, the USPTO rescinded the June 2022 Procedures through a short posting on the USPTO website. The Office then followed up with the March 24, 2025 Memorandum of Chief Administrative Patent Judge Scott Boalick (the "Boalick Memo"). Two days later, on March 26, Acting Director Stewart issued a Memorandum (the "Director Memo") introducing an entirely new "interim procedure" that bifurcates institution between "(i) discretionary considerations and (ii) merits and other non-discretionary statutory

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considerations.” Director Memo, 1. Three weeks after the Director Memo issued (and after approximately forty patent owners had filed briefs requesting discretionary denial), the USPTO held an oral webcast setting forth additional substantive details of the new interim procedure not found in the Director Memo. Then, eight days after the webcast, the USPTO posted on its website “FAQs for Interim Processes for PTAB Workload Management” with even more substantive details. The recission notice, the Boalick Memo, the Director Memo, the oral webcast, and the FAQs (together, the “Announcements”) fall short of satisfying the requisite statutory and constitutional obligations of the USPTO.

The Announcements make sweeping changes to PTAB procedures without going through notice-and-comment rulemaking. This is made more problematic given that the Office has represented to the public that they intend to make any further changes to the institution process through notice-and-comment rulemaking. *See* 88 Fed. Reg. 24,503 (April 21, 2023). The Announcements violate the notice-and-comment requirements under the APA and are arbitrary and capricious.

Moreover, the additional discretionary denial considerations proposed in the director memo are so broad and vague that they fail to set “forth the standards for the showing of sufficient grounds to institute a review.” 35 U.S.C. § 316(a). For example, it is unclear as to how the director will consider “[s]ettled expectations,” “reliance on expert testimony,” “workload,” and “[c]ompelling economic, public

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health, or national security interests.”

The Director's justification for these announcements similarly falls short of statutory and constitution obligations. The Supreme Court has held that an agency's change in position must be accompanied by sufficient reasons for doing so. *See Food & Drug Admin. v. Wages & White Lion Invs., L.L.C.*, 145 S. Ct. 898, 906 (2025) (explaining that when an agency changes position, it must “offer ‘good reasons for the new policy’”); *see also F.C.C. v. Fox Television Stations, Inc.*, 556 U.S. 502 (2009) (agency changing position must show “that the new policy is permissible under the statute, that there are good reasons for it, and that the agency believes it to be better, which the conscious change of course adequately indicates”).

The agency's purported justifications of “efficiency” and “workload management” do not hold up under scrutiny. Providing additional discretionary denial factors increases the Office's workload by investing their time in consideration of more issues other than the validity of the patents challenged in IPR. This additional workload becomes more problematic given that the Office appears to be voluntarily *reducing* the number of judges. Ex.1023 (Law 360 article). The Office cannot claim they are resource constrained and at the same time reducing the number of PTAB judges.

Applying the Announcements retroactively to petitions filed prior to

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issuance of the new policies unduly prejudices petitioners. Petitioner has based their district court and PTAB proceeding based on previously-in-place procedures in order to best seek review of the patents Petitioner believes to be invalid. In light of these and other deficiencies in the Announcements, Petitioner respectfully requests that the Board and Director consider whether to institute based on the standards articulated in the June 2022 Procedures until such time as the Board issues new regulations in accordance with 35 U.S.C. § 316 and the rulemaking procedures of the APA.

V. Conclusion

For the above reasons, Petitioner respectfully requests that the Director refrain from exercising her discretion to deny this petition, and instead pass it to a merits panel for consideration

Respectfully submitted,

Date: June 24, 2025

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Opposition to Patent Owner's Request for Discretionary Denial
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PETITIONER'S EXHIBIT LIST

Ex.1001	U.S. Patent No. 9,183,085 ("the '085 patent")
Ex.1002	Prosecution History of U.S. App. No. 13/477,600 (issued as '085 patent) ("'600 App")
Ex.1003	Declaration of Dr. Lara Dolecek ("Dolecek Decl.")
Ex.1004	CV of Dr. Lara Dolecek
Ex.1005	U.S. Pub. 2014/0136927 to Li, et al.
Ex.1006	U.S. 9,037,951 to Cideciyan, et al.
Ex.1007	U.S. Patent No. 8,176,360 to Frost et al.
Ex.1008	U.S. 2008/0222490 to Leung et al.
Ex.1009	Solid-State Drive (SSD) Requirements and Endurance Test Method, JESD218, JEDEC STANDARD, September 2010
Ex.1010	U.S. 7,823,043 to Lasser
Ex.1011	U.S. 8,042,029 to Alrod et al.
Ex.1012	Performance Impact and Interplay of SSD Parallelism through Advanced Commands, Allocation Strategy and Data Granularity, Hu et al., ICS '11: Proceedings of the international conference on Supercomputing, pp. 96 – 107 (https://doi.org/10.1145/1995896.1995912), May 31, 2011
Ex.1013	FTL Design Exploration in Reconfigurable High-Performance SSD for Server Applications, ICS '09: Proceedings of the 23rd international conference on Supercomputing, pp. 338 – 349 (https://doi.org/10.1145/1542275.1542324), June 8, 2009
Ex.1014	Flash Management – Why and How?, A Detailed Overview of Flash Management Techniques, SMART Modular Technologies, 2009
Ex.1015	Complaint, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)

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Ex.1016	District Court Trial Statistics
Ex.1017	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, June 22, 2022
Ex.1018	Solid State Drives 101, Cactus Technologies, available at https://www.cactus-tech.com/wp-content/uploads/2019/04/Solid-State-Drives-101-EBook.pdf
Ex.1019	Product Code Schemes for Error Correction in MLC NAND Flash Memories, Yang et al., December 29, 2011, available at: https://ieeexplore.ieee.org/document/6118315 .
Ex.1020	Error Control Coding Fundamentals and Applications, Lin et. al, 1983
Ex.1021	Scheduling and Case Management Order, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)
Ex.1022 (New)	Notice of Sotera Stipulations, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)
Ex.1023 (New)	"PTAB Judges Told To Get Ready For Layoffs," Law 360 (March 21, 2025). https://www.law360.com/articles/2314328/ptab-judges-told-to-get-ready-for-layoffs
Ex.1024 (New)	FAQs for Interim Processes for PTAB Workload Management, available at https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management (retrieved May 13, 2025).
Ex.1025 (New)	'085 Patent Assignment Recordation
Ex.1026 (New)	Plaintiff's Disclosure of Asserted Claims and Infringement Contentions, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA) (Served October 2, 2024)
Ex.1027-1035	RESERVED
Ex.1036 (New)	Order Granting Defendants' Motion to Stay, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA) (issued June 23, 2025)
Ex.1037 (New)	Complaint, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 1:24-cv-00101 (W.D. TX)

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Ex.1038 (New)	Western Digital Form 10-K, available at https://investor.wdc.com/static-files/e12da3e5-85f0-4176-968b-0dbf4a40dd0c
Ex.1039	RESERVED
Ex.1040 (New)	"Chief Patent Board Judge Waves Off Workforce Attrition Concerns," Bloomberg Law, May 7, 2025.
Ex.1041 (New)	"An Assessment of the Impact of the Inter Partes Review Process under the Patent Trial and Appeal Board on the US Economy," The Perryman Group, available at https://www.perrymangroup.com/publications/report/2021/9/23/an-assessment-of-the-potential-impact-of-expanding-inter-partes-review-ipr-under-the-america-invents-act-on-the-us-economy/

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CERTIFICATE OF SERVICE

The undersigned certifies, under 37 C.F.R. § 42.6, that service was made on the Patent Owner as detailed below.

Date of service June 24, 2025

Manner of service Electronic Email: dalberti@krameralberti.com; slim@krameralberti.com; lmcdonough@krameralberti.com; ahamill@krameralberti.com; jfitzsimmons-PTAB@sternekessler.com; rbemben-PTAB@sternekessler.com; mspecht-PTAB@sternekessler.com; tdutton-PTAB@sternekessler.com and PTAB@sternekessler.com.

Documents served **Petitioner's Opposition to Patent Owner's Request for Discretionary Denial; Exhibits Ex.1022-Ex.1026, Ex.1036-Ex.1038 and Ex.1040-Ex.1041.**

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND
WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner

Case IPR2025-00515
U.S. Patent No. 9,183,085

**PATENT OWNER POLARIS POWERLED TECHNOLOGIES, LLC'S
REPLY BRIEF ON DISCRETIONARY DENIAL**

Mail Stop "PATENT BOARD"
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450

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I. INTRODUCTION

The Director should exercise discretion to deny institution of this *inter partes* review (IPR). Settled expectations strongly favor denial for three reasons. First, the '085 patent issued almost *ten years* ago, and Polaris has owned it since April 2021. Second, Petitioners waited until Polaris relied on its property right before filing a challenge. And third, the patent has been licensed in Petitioners' technology space. Further, the *Fintiv* factors continue to favor discretionary denial. The district court is a better forum to resolve the parties' dispute.

II. POLARIS HAS SETTLED EXPECTATIONS TO ITS PROPERTY RIGHT IN THE '085 PATENT.

Petitioners' arguments on settled expectations miss the point—settled expectations are *not* based on when a patent was acquired. *Contra* Opp., 18-19. Rather, this factor is concerned with “the length of time the claims have been in force.” Interim Process Memo, 2. Indeed, “the longer the patent has been in force, the more settled expectations should be.” *Dabico Airport Solutions, v. AXA Power Aps*, IPR2025-00408, Paper 21 at 3 (P.T.A.B. June 18, 2025).

The '085 patent has been in force since November 10, 2015—almost ten years. And SanDisk was aware of it, having cited it in its own applications. *See e.g.*, EX2015.¹ Indeed, the patent has been publicly available and Petitioners—

¹ The '085 patent was also cited during the prosecution of U.S. 9,411,669.

large, sophisticated technology companies—could have availed themselves of resources to easily locate it from the time it issued. *See Dabico* at 3. Further, the patent has been licensed in Petitioners’ technology space. *Cf. Intel v. Proxense*, IPR2025-00327, Paper 12 (P.T.A.B. June 26, 2025). Petitioners failure to file an early challenge to a patent that issued in 2015, and instead wait until Polaris relied on its property right by filing a complaint to enforce its rights, strongly favors denying institution. *See iRhythm Tech. v. Welch Allyn, Inc.*, IPR2025-00363, Paper 10 (P.T.A.B. June 6, 2025) (denying institution based on settled expectations where Petitioner was aware of patent as early as 2013); *Dabico* (denying institution based on settled expectations; challenged patent in force for almost eight years).

Additionally, Polaris has settled expectations in the two other patents involved in the district court proceeding and challenged in related IPR2025-00516 and -00517. In the -516 IPR, the challenged patent has been in force since December 3, 2013. And in the -517 IPR, the challenged ’968 patent has been in force since November 10, 2015, and Western Digital was aware of it, having cited it in *ten* of its own applications. *See, e.g.*, -517 IPR, EX2017.² All three

² The ’968 patent was also cited during the prosecution of U.S. Patent Nos. 10,452,278; 10,466,903; 10,509,569; 10,719,267; 10,725,835; 10,817,182; 11,169,704; 11,487,434; and 11,635,898. And in the ’835 patent, the Examiner

proceedings warrant denial based on settled expectations.

III. THE *FINTIV* FACTORS FAVOR DENIAL.

Fintiv makes clear that the factors are evaluated holistically “in view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv* at 6. Here, the factors favor denial.

The district court’s issuance of a stay should not be weighed strongly against denial here. The parties have an obligation to notify the court “after the PTAB issues **any** rulings” as to the pending IPR within seven days. EX1036, 9. Because the district court has indicated that the stay will be lifted soon after a denial of institution decision, factor 1 weighs, at most, slightly against denial.³

The expected date of the discretionary decision in this IPR is July 27, 2025. If institution is denied, the district court has indicated the stay will be lifted soon after denial by ordering the parties to apprise the court within seven days of

identified the ’938 patent as “pertinent art” in an June 26, 2018 Office Action.

³ To the extent *Snap v. SRK Tech.*, IPR2020-00820, Paper 15 (P.T.A.B. Oct. 21, 2020) (precedential) dictates that a stay must always be weighed “strongly against” denial—making a “stay” an outcome determinative factor—Polaris requests the Director clarify or reconsider its designation. Weighing one factor as a “super factor” has no place in the balanced assessment. *Cf. Fintiv* at 5.

developments that warrant lifting the stay. *See* EX1036, 9. And prior to the stay, the case was moving faster than initially scheduled (*see* D.D. Br., 2-4), making it likely the litigation will resume quickly.

The original trial date was set for June 16, 2026—over 2 months before the FWD. Because it is highly likely the stay will be lifted immediately upon denial, the trial is still likely to occur before, or around, the FWD date of August 27, 2026. In fact, given the accelerated pace of the litigation prior to the stay, the original trial date could even remain in place. Thus, factor 2 weighs in favor of denial.

Factors 3-6 strongly favor denial for the reasons discussed in Polaris’s initial brief. *See* D.D. Br., 7-17. Although the district court noted there is more work ahead, that does not negate the substantial investment before the stay—including exchanging claim constructions and related expert reports. And Petitioners have no reasonable excuse here for waiting seven months to file the Petition.

Further, the *Sotera* stipulation should not be considered as Petitioners provide no reason it could not have been submitted earlier (e.g., with the Petition), but instead fault Polaris for filing its brief by the original deadline and not unnecessarily delaying the filing. *See* Opp., 6-7. And the *Sotera* stipulation does not mitigate concerns of duplicate effort because Western Digital relies on system art in its invalidity contentions. *See* D.D. Br., 14-15. Thus, even if this IPR is instituted, the district court will still have substantial overlap, and the district court

remains a better forum for adjudicating the priority issues of the '968 patent. *See* - 517 IPR, Paper 9 at 19-24.

Additionally, the merits remain weak. Despite having Polaris's POPR in hand (which Polaris continues to request the Director consider), Petitioners give short shrift to those arguments and do not even attempt to address most of the weaknesses pointed out by Polaris. *See Opp.*, 12-13. Specifically, Petitioners only falsely assert that Patent Owner admits the claim method is invalid (when there is no such admission in the POPR) and does not address the arguments in Sections III.A and III.B. *Compare Opp.*, 12-14 *with* POPR, 3-10.

Considered as a whole, the *Fintiv* factors weigh in favor of denial. Five factors strongly favor, or favor, denial; and only one factor slightly weighs against denial. Instituting this IPR would result in duplicative effort and cause additional cost to litigate in two forums. Accordingly, the Director should exercise discretion to deny institution in view of the parallel litigation.

IV. CONCLUSION

Polaris has strong settled expectations that its property right to the claims of the '346 patent—which have been in force for well over eleven years—are enforceable. And because the *Fintiv* factors favor denial, institution of this IPR would be duplicative and an inefficient use of the Board's limited resources. Thus, this proceeding, and the related IPRs, should not be instituted.

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Respectfully submitted,

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Date: June 30, 2025

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Case IPR2025-00515
U.S. Patent No. 9,183,085

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

I certify that the above-captioned **PATENT OWNER'S REPLY BRIEF**
ON DISCRETIONARY DENIAL was served in its entirety on June 30, 2025,
upon the following parties via electronic mail:

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Respectfully submitted,

KRAMER ALBERTI LIM & TONKOVICH, LLP

/DAVID ALBERTI/

David L. Alberti
Registration No. 43,465
Lead Attorney for Patent Owner

Date: June 30, 2025

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND
WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

POLARIS POWERLED TECHNOLOGIES, LLC,

Patent Owner.

IPR2025-00515
U.S. Patent No. 9,183,085

**PETITIONER'S SUR-REPLY BRIEF ON DISCRETIONARY
DENIAL**

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00515 (U.S. Patent 9,183,085)

I. Introduction.

The Director should *not* exercise discretion to deny. Patent Owner has *no* settled expectations because (i) **Patent Owner acquired the '085 patent in August 2022¹** solely for the purpose of litigation—which changes everything with respect to settled expectations; (ii) there is no actual evidence of commercialization, marking, or licensing of the '085 patent, let alone any such activities before the filing of the IPR petition; and (iii) the '085 patent had ***not*** been asserted for over 8 years after its issuance, and the IPR petition was filed within 1 year from its ***first*** assertion in 2024. Further and very importantly, the District Court in the parallel litigation has found that “[t]his case is still in early stages of litigation,” and stayed the case because of the benefits of PTAB review for the litigation. Ex.1036, 4, 5-6.

II. Polaris has *no* settled expectations.

Polaris repeatedly asserts that “the patent has been licensed in Petitioners’ technology space.” PO Reply, 1, 2. However, Polaris failed to provide any

¹ Polaris asserts ownership “since April 2021” without any supporting evidence, while the assignment record indicates transfer to Polaris in August 2022. Ex.1025, 1. Either way, the IPR petition was filed within 3-4 years from Polaris’ acquisition, and within 1 year of the first assertion.

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00515 (U.S. Patent 9,183,085)

supporting evidence of such a license, especially **when** the patent was licensed.

There is no public information of recordation of such licenses. There is, however, public information about a lawsuit over these patents between Polaris and Micron² that was filed after the present IPRs were filed, but has since settled. If this is the only license being referenced, it would actually weigh **against** discretionary denial because it happened **after** the filing of the IPR petition. As the Director stated in *Intel-Proxense*:

[P]ersuasive reasons why the Board should review challenged claims several years after their issue date [include as] example, a patent may have been in force for years but may not have been commercialized, asserted, marked, licensed, or otherwise applied in a petitioner's particular technology space, if at all.

IPR2025-00327, Paper 12, 2-3 (P.T.A.B. June 26, 2025).

This example of persuasive reasons applies to the present case: (i) there is no evidence of commercialization, licensing, and marking at all, much less any such activities **before** the filing of the present IPR petitions; and (ii) the first assertion of the '085 patent was over 8 years after its issuance, after Polaris acquired it in 2022, and the IPR petition was filed within 1 year from the **first** assertion in 2024.

² *Micron Tech. Inc et al. v. Polaris PowerLED Techs., LLC*, No. 1-25-cv-00073 (D. Idaho), filed February 7, 2025 and voluntarily dismissed April 4, 2025.

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00515 (U.S. Patent 9,183,085)

Additionally, Polaris argues that because “SanDisk ... cited [the ’085 patent] in its own applications,” they should have considered challenging it earlier. PO Reply, 1-2. This is incorrect. It was Examiner, not Sandisk, that cited the ’085 patent during the prosecution of applications. Ex.2015, 13; Ex.2016, 2. More importantly, what Polaris does not point out is that Western Digital and Sandisk combined have had over 10,000 U.S. patent issue since 2010. If on average each of these patents have 25 prior art patent citations, that would be over 250,000 citations. Filing IPRs for even 1/100 of these would be untenable, and in the present case, should have no bearing on settled expectations. In fact, and contrary to Polaris’ assertion, it would have been an inefficient use of the PTAB’s resources to challenge these patents back then, because there was no active litigation. *Google et al. v. Mullen*, IPR2025-00227, Paper 13, 4 (“it is an inefficient use of Board resources to review [a] patent that has been dismissed from the litigation.”).

Finally, Polaris’s comparison of the already-vacated previously scheduled trial date and a FWD date “upon denial” is non-sensical, because there would be no projected FWD date with denial. PO Reply, 4.

Respectfully submitted,

Date: July 3, 2025

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/David M. O’Dell/
David M. O’Dell
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Registration No. 42,044

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00515 (U.S. Patent 9,183,085)

PETITIONER'S EXHIBIT LIST

Ex.1001	U.S. Patent No. 9,183,085 ("the '085 patent")
Ex.1002	Prosecution History of U.S. App. No. 13/477,600 (issued as '085 patent) ("'600 App")
Ex.1003	Declaration of Dr. Lara Dolecek ("Dolecek Decl.")
Ex.1004	CV of Dr. Lara Dolecek
Ex.1005	U.S. Pub. 2014/0136927 to Li, et al.
Ex.1006	U.S. 9,037,951 to Cideciyan, et al.
Ex.1007	U.S. Patent No. 8,176,360 to Frost et al.
Ex.1008	U.S. 2008/0222490 to Leung et al.
Ex.1009	Solid-State Drive (SSD) Requirements and Endurance Test Method, JESD218, JEDEC STANDARD, September 2010
Ex.1010	U.S. 7,823,043 to Lasser
Ex.1011	U.S. 8,042,029 to Alrod et al.
Ex.1012	Performance Impact and Interplay of SSD Parallelism through Advanced Commands, Allocation Strategy and Data Granularity, Hu et al., ICS '11: Proceedings of the international conference on Supercomputing, pp. 96 – 107 (https://doi.org/10.1145/1995896.1995912), May 31, 2011
Ex.1013	FTL Design Exploration in Reconfigurable High-Performance SSD for Server Applications, ICS '09: Proceedings of the 23rd international conference on Supercomputing, pp. 338 – 349 (https://doi.org/10.1145/1542275.1542324), June 8, 2009
Ex.1014	Flash Management – Why and How?, A Detailed Overview of Flash Management Techniques, SMART Modular Technologies, 2009

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00515 (U.S. Patent 9,183,085)

Ex.1015	Complaint, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)
Ex.1016	District Court Trial Statistics
Ex.1017	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, June 22, 2022
Ex.1018	Solid State Drives 101, Cactus Technologies, available at https://www.cactus-tech.com/wp-content/uploads/2019/04/Solid-State-Drives-101-EBook.pdf
Ex.1019	Product Code Schemes for Error Correction in MLC NAND Flash Memories, Yang et al., December 29, 2011, available at: https://ieeexplore.ieee.org/document/6118315 .
Ex.1020	Error Control Coding Fundamentals and Applications, Lin et. al, 1983
Ex.1021	Scheduling and Case Management Order, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)
Ex.1022	Notice of Sotera Stipulations, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)
Ex.1023	"PTAB Judges Told To Get Ready For Layoffs," Law 360 (March 21, 2025). https://www.law360.com/articles/2314328/ptab-judges-told-to-get-ready-for-layoffs
Ex.1024	FAQs for Interim Processes for PTAB Workload Management, available at https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management (retrieved May 13, 2025).
Ex.1025	'085 Patent Assignment Recordation
Ex.1026	Plaintiff's Disclosure of Asserted Claims and Infringement Contentions, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00515 (U.S. Patent 9,183,085)

	(Served October 2, 2024)
Ex.1027-1035	RESERVED
Ex.1036	Order Granting Defendants' Motion to Stay, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA) (issued June 23, 2025)
Ex.1037	Complaint, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 1:24-cv-00101 (W.D. TX)
Ex.1038	Western Digital Form 10-K, available at https://investor.wdc.com/static-files/e12da3e5-85f0-4176-968b-0dbf4a40dd0c
Ex.1039	RESERVED
Ex.1040	"Chief Patent Board Judge Waves Off Workforce Attrition Concerns," Bloomberg Law, May 7, 2025.
Ex.1041	"An Assessment of the Impact of the Inter Partes Review Process under the Patent Trial and Appeal Board on the US Economy," The Perryman Group, available at https://www.perrymangroup.com/publications/report/2021/9/23/an-assessment-of-the-potential-impact-of-expanding-inter-partes-review-ipr-under-the-america-invents-act-on-the-us-economy/

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00515 (U.S. Patent 9,183,085)

CERTIFICATE OF SERVICE

The undersigned certifies, under 37 C.F.R. § 42.6, that service was made on the Patent Owner as detailed below.

Date of service July 3, 2025

Manner of service Electronic Email: dalberti@krameralberti.com; slim@krameralberti.com; lmcdonough@krameralberti.com; ahamill@krameralberti.com; jfitzsimmons-PTAB@sternekessler.com; rbemben-PTAB@sternekessler.com; mspecht-PTAB@sternekessler.com; tdutton-PTAB@sternekessler.com and PTAB@sternekessler.com.

Documents served **Petitioner's Sur-Reply Brief on Discretionary Denial.**

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Polaris PowerLED Technologies, LLC

UNITED STATES DISTRICT COURT
CENTRAL DISTRICT OF CALIFORNIA

POLARIS POWERLED
TECHNOLOGIES, LLC,

Plaintiff,

v.

WESTERN DIGITAL CORPORATION,
WESTERN DIGITAL TECHNOLOGIES,
INC., NEWEGG, INC., AVNET, INC.,
ZONES, LLC, and PRIVATE LABEL PC,
LLC,

Defendants.

Case No. 2:24-cv-02864

**COMPLAINT FOR PATENT
INFRINGEMENT**

DEMAND FOR JURY TRIAL

COMPLAINT FOR PATENT INFRINGEMENT

Ex.1015 / Page 1 of 60

Sandisk Technologies, Inc. et al

Appx248

1 Plaintiff Polaris PowerLED Technologies, LLC (“Plaintiff” or “Polaris”)
2 brings this patent infringement action against Defendants Western Digital
3 Corporation; Western Digital Technologies, Inc.; Newegg, Inc.; Avnet, Inc.; Zones,
4 LLC; and Private Label PC, LLC (collectively, “Defendants”) as follows:

5 **NATURE OF THE ACTION**

6 1. This is a civil action for infringement of U.S. Patent Nos. 8,554,968
7 (“the ’968 Patent”), 9,183,085 (“the ’085 Patent”), and 8,601,346 (“the ’346 Patent”)
8 (collectively, “Asserted Patents”), and under the patent laws of the United States, 35
9 U.S.C. § 1 *et seq.*

10 2. The technology in this case involves flash memory. Flash memory is
11 used in, among other things, computing, gaming, data storage, and e-commerce. The
12 ability of solid-state flash memory to hold electric charges without moving parts has
13 revolutionized how information is stored and has resulted in great improvements over
14 older memory technologies. These electrical charges, held in miniscule transistors,
15 are used to read, store, and write enormous amounts of information in small,
16 lightweight memory products that have transformed the daily lives of consumers.

17 3. Defendants’ infringing devices are its solid-state drive (“SSD”)
18 products (“the Accused Products” or “the infringing devices”).

19 4. Western Digital is among the largest manufacturers of memory products
20 in the United States.

21 5. Plaintiff brings this patent infringement action to protect its valuable
22 patented technology specifically relating to (1) nonvolatile memory controllers
23 (NVMCs) and SSDs; (2) interrupt techniques used in NVMCs and SSDs; (3) how
24 NVMCs and SSDs adaptively select among error correction coding (ECC) schemes;
25 and (4) how NVMCs and SSDs generate parity data using a distributed processing
26 technique.

27 6. The Defendants control, participate in the commission of, and have a
28 direct financial interest in the infringing acts set forth herein.

1 **THE PARTIES**

2 **Polaris**

3 7. Polaris is a California limited liability company having its address at
4 5150 E. Pacific Coast Highway, Suite 200, Long Beach, California 90804.

5 **Western Digital**

6 8. As used in this Complaint, Defendants Western Digital Corporation and
7 Western Digital Technologies, Inc. are collectively referred to as “Western Digital.”

8 9. On information and belief, Defendant Western Digital Corporation is a
9 Delaware corporation having offices in this District at 3355 Michelson Drive, Suite
10 100, Irvine, California 92612. Western Digital Corporation is registered with the
11 California Secretary of State to do business in California and can be served through
12 its registered agent, CSC - Lawyers Incorporating Service, 2710 Gateway Oaks
13 Drive, Sacramento, California 95833.

14 10. On information and belief, Defendant Western Digital Technologies,
15 Inc. is a subsidiary of Western Digital Corporation. Western Digital Technologies,
16 Inc. is a Delaware corporation having offices in this District at 3355 Michelson Drive,
17 Suite 100, Irvine, California 92612. Western Digital Technologies, Inc. is registered
18 with the California Secretary of State to do business in California and can be served
19 through its registered agent, CSC - Lawyers Incorporating Service, 2710 Gateway
20 Oaks Drive, Sacramento, California 95833.

21 **Newegg**

22 11. On information and belief, Defendant Newegg, Inc. (“Newegg”) is a
23 corporation formed under the laws of Delaware, with its principal place of business
24 at 17560 Rowland Street, City of Industry, California 91748, which is located in this
25 District.

26 12. Western Digital advertises Newegg as a “preferred Western Digital
27 authorized partner.” See <https://www.westerndigital.com/company/distributors>.

28 13. On information and belief, Newegg sells and offers for sale the Accused

1 Products. On information and belief, Newegg provides services that help customers
2 in this District build computers that contain the Accused Products, including
3 providing a service called “PC Builder” on its website. See
4 <https://www.newegg.com/tools/custom-pc-builder>.

5 **Avnet**

6 14. On information and belief, Defendant Avnet, Inc. (“Avnet”) is a
7 corporation formed under the laws of New York, with offices at 21155 Califa Street,
8 Woodland Hills, California 91367, which is located in this District. Avnet is
9 registered with the California Secretary of State to do business in California and can
10 be served through its registered agent, CSC - Lawyers Incorporating Service, 2710
11 Gateway Oaks Drive, Sacramento, California 95833.

12 15. Western Digital advertises Avnet as a “preferred Western Digital
13 authorized partner.” See <https://www.westerndigital.com/company/distributors>.

14 16. On information and belief, Avnet sells and offers for sale the Accused
15 Products. On information and belief, Avnet provides services that help customers in
16 this District implement infringing functionality in the Accused Products. For
17 instance, Zones describes itself as follows: “As a global technology solutions
18 company, our ecosystem enables us to help professional engineers, entrepreneurs and
19 startups take their tech projects from idea to design and from prototype to production.
20 ...With this end-to-end approach, we help reduce time, cost and complexities of
21 bringing products to market. Avnet’s culture was founded on new ideas and emerging
22 technology. With more than 15,000 employees globally, we support business for our
23 customers in 140 countries across North America, Europe and Asia. That’s why
24 customers around the world turn to Avnet – for our know-how, integrity, experience
25 and global reach. Our engineers are on the front lines of innovation, supported by
26 sales, supply-chain, design-chain and service teams with deep expertise – making
27 Avnet the go-to guide for innovators who set the pace for technological change.” See
28 <https://news.avnet.com/about-us/default.aspx>.

Zones

17. On information and belief, Defendant Zones, LLC (“Zones”) is a corporation formed under the laws of the State of Washington, with offices at 13915 Cerritos Corporate Drive, Cerritos, California 90703, which is located in this District. Zones is registered with the California Secretary of State to do business in California and can be served through its registered agent, CSC - Lawyers Incorporating Service, 2710 Gateway Oaks Drive, Sacramento, California 95833.

18. Western Digital advertises Zones as a “preferred Western Digital authorized partner.” See <https://www.westerndigital.com/company/distributors>.

19. On information and belief, Zones sells and offers for sale the Accused Products. On information and belief, Zones provides services that help customers in this District implement infringing functionality in the Accused Products. For instance, Zones describes itself as follows: “We’re a global provider of comprehensive IT services and solutions, reaching 100-plus countries and employing 2,000-plus people worldwide. ... We help organizations of all sizes succeed with custom IT services and solutions for business, healthcare, government, and education, plus market verticals like retail, utilities, and financial services, to name a few. ... We architect solutions that simplify the complex and meet your individual business needs and goals.” See https://www.zones.com/site/statics/static_page.html?name=about-us.

PLPC

20. On information and belief, Defendant Private Label PC, LLC (“PLPC”) is a corporation formed under the laws of the State of California with its principal place of business at 748 Epperson Drive, City of Industry, California 91748, which is located in this District. PLPC is registered with the California Secretary of State to do business in California and can be served through its registered agent, Jonathan Wang, 748 Epperson Drive, City of Industry, California 91748.

21. Western Digital advertises PLPC as a “preferred Western Digital

1 authorized partner.” See <https://www.westerndigital.com/company/distributors>.

2 22. On information and belief, PLPC sells and offers for sale the Accused
3 Products. On information and belief, PLPC provides services that help customers in
4 this District implement infringing functionality in the Accused Products. For
5 instance, PLPC describes itself as follows: “PLPC delivers the most efficient
6 technology solutions to the Gaming, Cloud, HPC, Security & Surveillance, and
7 Consumer Electronics markets. PLPC distributes technology products from many of
8 the world’s leading manufacturers and provides solutions to value-added resellers,
9 DMR, retailers, and thousands of integrators for PC, surveillance, platform enterprise
10 in the U.S., and Latin America. PLPC has successfully penetrated 18 countries in
11 Latin America with in-country sales support. *As part of their value-added services,*
12 *PLPC provides a variety of integration, including product lifecycle support, contract*
13 *design, and assembly.* In addition, PLPC provides a wide range of financial options
14 to ensure that our partners always have the resources in place to win business.” See
15 <https://www.plpc.com/company> (emphasis added).

16 **JURISDICTION AND VENUE**

17 23. Plaintiff incorporates by reference and re-alleges the foregoing
18 paragraphs as fully set forth herein.

19 24. This action arises under the patent laws of the United States, Title 35 of
20 the United States Code. Accordingly, this Court has subject matter jurisdiction under
21 28 U.S.C. §§ 1331 and 1338(a).

22 **Western Digital**

23 25. On information and belief, Western Digital transacts and conducts
24 business in this District and the State of California and is subject to the personal
25 jurisdiction of this Court. On information and belief, Western Digital has minimum
26 contacts within the State of California and this District and has purposefully availed
27 itself of the privileges of conducting business in the State of California and in this
28 District. Polaris’ causes of action arise directly from Western Digital’s business

1 contacts and other activities in the State of California and in this District.

2 26. On information and belief, Western Digital has committed acts of
3 infringement within this District and the State of California by, *inter alia*, making,
4 importing, using, selling, and/or offering for sale Accused Products that infringe one
5 or more claims of the Asserted Patents. More specifically, Western Digital, directly
6 and/or through intermediaries or agents, makes, imports, uses, sells, ships,
7 distributes, offers for sale, advertises, and/or otherwise promotes infringing Accused
8 Products in the United States, the State of California, and this District.

9 27. Venue is proper in this District under 28 U.S.C. §§ 1391(b), (c) and
10 1400(b), including based on Western Digital's physical presence in this District
11 and/or Western Digital's transaction of business in this District directly and/or
12 through its affiliates and customers and/or acts of patent infringement in this District.

13 **Newegg**

14 28. On information and belief, Newegg, Inc. ("Newegg") transacts and
15 conducts business in this District and the State of California and is subject to the
16 personal jurisdiction of this Court. On information and belief, Newegg has minimum
17 contacts within the State of California and this District and has purposefully availed
18 itself of the privileges of conducting business in the State of California and in this
19 District. Polaris' causes of action arise directly from Newegg's business contacts and
20 other activities in the State of California and in this District.

21 29. On information and belief, Newegg has committed acts of infringement
22 within this District and the State of California by, *inter alia*, making, importing,
23 using, selling, and/or offering for sale Accused Products that infringe one or more
24 claims of the Asserted Patents. More specifically, on information and belief, Newegg,
25 directly and/or through intermediaries or agents, makes, imports, uses, sells, ships,
26 distributes, offers for sale, advertises, and/or otherwise promotes infringing Accused
27 Products in the United States, the State of California, and this District.

28 30. Venue is proper in this District under 28 U.S.C. §§ 1391(b), (c) and

1 1400(b), including based on Newegg's physical presence and the location of its
2 offices and headquarters in this District and/or Newegg's transaction of business in
3 this District directly and/or through its affiliates and customers and/or acts of patent
4 infringement in this District.

5 **Avnet**

6 31. On information and belief, Avnet transacts and conducts business in this
7 District and the State of California and is subject to the personal jurisdiction of this
8 Court. On information and belief, Avnet has minimum contacts within the State of
9 California and this District and has purposefully availed itself of the privileges of
10 conducting business in the State of California and in this District. Polaris' causes of
11 action arise directly from Avnet's business contacts and other activities in the State
12 of California and in this District.

13 32. On information and belief, Avnet has committed acts of infringement
14 within this District and the State of California by, *inter alia*, making, importing,
15 using, selling, and/or offering for sale Accused Products that infringe one or more
16 claims of the Asserted Patents. More specifically, on information and belief, Avnet,
17 directly and/or through intermediaries or agents, makes, imports, uses, sells, ships,
18 distributes, offers for sale, advertises, and/or otherwise promotes infringing Accused
19 Products in the United States, the State of California, and this District.

20 33. Venue is proper in this District under 28 U.S.C. §§ 1391(b), (c) and
21 1400(b), including based on Avnet's physical presence in this District and/or Avnet's
22 transaction of business in this District directly and/or through its affiliates and
23 customers and/or acts of patent infringement in this District.

24 **Zones**

25 34. On information and belief, Zones transacts and conducts business in this
26 District and the State of California and is subject to the personal jurisdiction of this
27 Court. On information and belief, Zones has minimum contacts within the State of
28 California and this District and has purposefully availed itself of the privileges of

1 conducting business in the State of California and in this District. Polaris' causes of
2 action arise directly from Zones' business contacts and other activities in the State of
3 California and in this District.

4 35. On information and belief, Zones has committed acts of infringement
5 within this District and the State of California by, *inter alia*, making, importing,
6 using, selling, and/or offering for sale Accused Products that infringe one or more
7 claims of the Asserted Patents. More specifically, on information and belief, Zones,
8 directly and/or through intermediaries or agents, makes, imports, uses, sells, ships,
9 distributes, offers for sale, advertises, and/or otherwise promotes infringing Accused
10 Products in the United States, the State of California, and this District.

11 36. Venue is proper in this District under 28 U.S.C. §§ 1391(b), (c) and
12 1400(b), including based on Zones' physical presence in this District and/or Zones'
13 transaction of business in this District directly and/or through its affiliates and
14 customers and/or acts of patent infringement in this District.

15 **PLPC**

16 37. On information and belief, PLPC transacts and conducts business in this
17 District and the State of California and is subject to the personal jurisdiction of this
18 Court. On information and belief, PLPC has minimum contacts within the State of
19 California and this District and has purposefully availed itself of the privileges of
20 conducting business in the State of California and in this District. Polaris' causes of
21 action arise directly from PLPC's business contacts and other activities in the State
22 of California and in this District.

23 38. On information and belief, PLPC has committed acts of infringement
24 within this District and the State of California by, *inter alia*, making, importing,
25 using, selling, and/or offering for sale Accused Products that infringe one or more
26 claims of the Asserted Patents. More specifically, on information and belief, PLPC,
27 directly and/or through intermediaries or agents, makes, imports, uses, sells, ships,
28 distributes, offers for sale, advertises, and/or otherwise promotes infringing Accused

1 Products in the United States, the State of California, and this District.

2 39. Venue is proper in this District under 28 U.S.C. §§ 1391(b), (c) and
3 1400(b), including based on PLPC's physical presence and the location of its
4 headquarters in this District and/or PLPC's transaction of business in this District
5 directly and/or through its affiliates and customers and/or acts of patent infringement
6 in this District.

7 **PATENTS-IN-SUIT**

8 40. Plaintiff owns the entire right, title, and interest in U.S. Patent No.
9 8,554,968 titled "Interrupt Technique for a Nonvolatile Memory Controller,"
10 including the right to assert all causes of action arising under said patent and to seek
11 damages and all other remedies for the infringement thereof. The '968 Patent issued
12 on October 8, 2013 to inventors Peter Z. Onufryk, Jayesh Patel and Ihab Jaser from
13 the U.S. Patent Application No. 13/052,388 filed on March 21, 2011. A true and
14 correct copy of the '968 Patent is attached as Exhibit A to this Complaint.

15 41. Plaintiff owns the entire right, title, and interest in U.S. Patent No.
16 9,183,085 titled "Systems and Methods for Adaptively Selecting from among a
17 Plurality of Error Correction Coding Schemes in a Flash Drive for Robustness and
18 Low Latency," including the right to assert all causes of action arising under said
19 patent and to seek damages and all other remedies for the infringement thereof. The
20 '085 Patent issued on November 10, 2015, to inventor Philip L. Northcott from the
21 U.S. Patent Application No. 13/477,600, filed on May 22, 2012. A true and correct
22 copy of the '085 Patent is attached as Exhibit B to this Complaint.

23 42. Plaintiff owns the entire right, title, and interest in U.S. Patent No.
24 8,601,346 titled "System and Method for Generating Parity Data in a Nonvolatile
25 Memory Controller by Using a Distributed Processing Technique," including the
26 right to assert all causes of action arising under said patent and to seek damages and
27 all other remedies for the infringement thereof. The '346 Patent issued on December
28 3, 2013, to inventors Peter Z. Onufryk and Inna Levit from the U.S. Patent

1 Application 13/052,835, filed on March 21, 2011. A true and correct copy of the '346
2 Patent is attached as Exhibit C to this Complaint.

3 **'968 PATENT BACKGROUND**

4 43. The '968 Patent relates generally to improvements to nonvolatile
5 memory controllers, including the processing of memory commands and the
6 generation of a completion status for such commands. The inventive nonvolatile
7 memory controller transmits the completion status to a host processing unit for
8 storage in a completion queue of the host processing unit. An interrupt manager in
9 the nonvolatile memory controller determines whether the completion queue contains
10 an unprocessed completion status and generates an interrupt message packet. The
11 nonvolatile memory controller transmits the interrupt message packet to the host
12 processing unit for triggering an interrupt in the host processing unit and alerting the
13 host processing unit to the unprocessed completion status.

14 **'085 PATENT BACKGROUND**

15 44. The '085 Patent relates generally to disclosed techniques providing
16 relatively low uncorrectable bit error rates (BER) for flash memory; low write
17 amplification; long life, fast and efficient retrieval; and efficient storage density such
18 that a solid-state drive (SSD) or flash drive can be implemented using relatively
19 inexpensive MLC flash for enterprise storage application.

20 **'346 PATENT BACKGROUND**

21 45. The '346 Patent relates generally to a nonvolatile memory controller
22 performing a data-stripe operation by processing a collection of commands. The
23 collection of commands includes data update commands and a parity write command.
24 The nonvolatile memory controller includes a number of command processing units,
25 each of which receives a command in the collection of commands. Each of the
26 command processing units receiving a data update command requests a data block
27 from a controller memory; receives the data block from the controller memory
28 through a data path in response to the request; and writes the data block to a

1 nonvolatile memory device.

2 **COUNT I**

3 (INFRINGEMENT OF U.S. PATENT NO. 8,554,968)

4 46. Plaintiff incorporates by reference and re-alleges the foregoing
5 paragraphs as fully set forth herein.

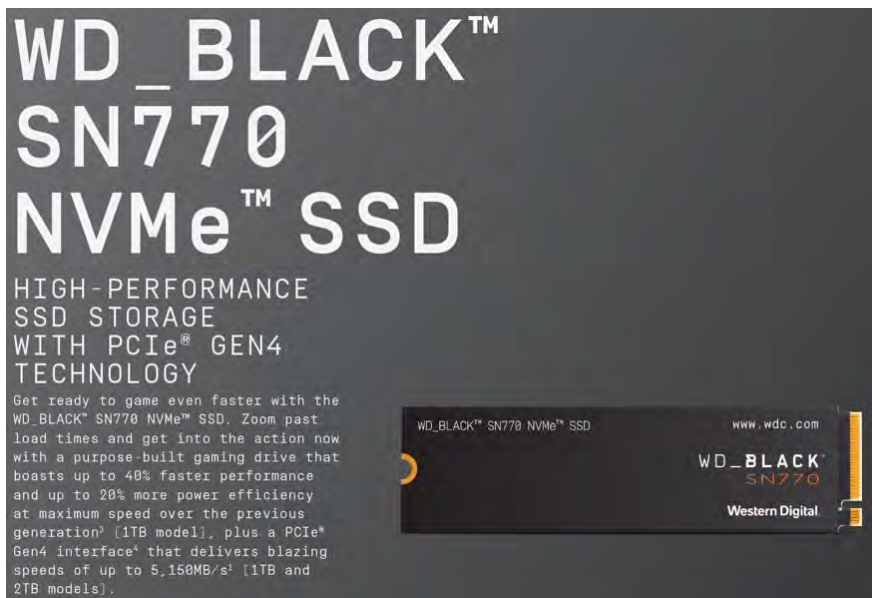
6 47. Defendants have directly infringed, and continue to directly infringe,
7 one or more claims of the '968 Patent, including at least claim 1 of the '968 Patent,
8 literally and/or under the doctrine of equivalents, by or through making, using,
9 offering for sale, selling within the United States and/or importing into the United
10 States its SSD products that support NVMe.

11 48. Claim 1 of the '968 Patent, for example, reads as follows:

12 1. A nonvolatile memory controller for alerting a host
13 processing unit to an unprocessed completion status
14 contained in a completion queue of the host processing
unit, the nonvolatile memory controller comprising:

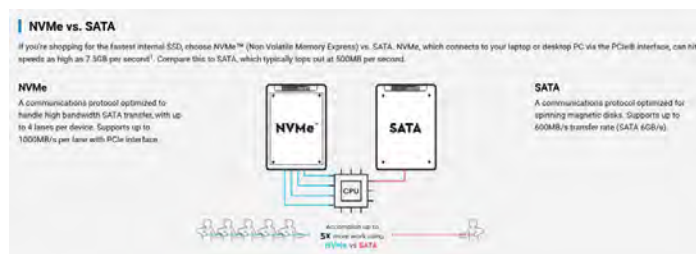
15 an interrupt manager configured to generate a completion
queue state for indicating the occurrence of a completion
16 queue event associated with the completion queue,
generate an interrupt vector state based on the completion
17 queue state, determine the completion queue of the host
processing unit contains an unprocessed completion status
18 based on the interrupt vector state, and generate an
interrupt message packet for triggering an interrupt in the
19 host processing unit to alert the host processing unit of the
unprocessed completion status in the completion queue,
20 and wherein the completion queue state includes a doorbell
update status indicating whether the host processing unit
21 has performed a doorbell update event in which the host
processing unit updates a head pointer stored in the
22 nonvolatile memory controller for the completion queue.

49. Defendants make, use, sell, offer for sale and import SSD products that support the NVMe standard and that include a nonvolatile memory controller configured for alerting a host processing unit to an unprocessed completion status contained in a completion queue of the host processing unit. For example, as shown below, WD Black-branded SSDs, which are used for gaming consoles and gaming PCs, Blue- and Green-branded SSDs, which are used for everyday PCs, Red-branded SSDs, which are used for Network Attached Storage (NAS), and Gold- and Ultrastar SSDs, which are used for data centers, all support NVMe:



WD_BLACK SN770 NVMe SSD, Western Digital (Jan. 2022), https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/product/internal-drives/wd-black-ssd/product-brief-wd-black-sn770-nvme-ssd.pdf [hereinafter “WD_BLACK SN770 NVMe SSD”].

50. The image below shows the benefits and improvements of NVMe over SATA:



Internal SSD, Western Digital, <https://www.westerndigital.com/solutions/internal-ssd> (last visited Jan. 2, 2024) [hereinafter “Internal SSD”].

51. The following describes how NVMe functions:

1.4 Theory of Operation

The NVM Express scalable interface is designed to address the needs of Enterprise and Client systems that utilize PCI Express based solid state drives or fabric connected devices. The interface provides optimized command submission and completion paths. It includes support for parallel operation by supporting up to 65,535 I/O Queues with up to 64 KiB - 1 outstanding commands per I/O Queue. Additionally, support has been added for many Enterprise capabilities like end-to-end data protection (compatible with SCSI Protection Information, commonly known as T10 DIF, and SNIA DIX standards), enhanced error reporting, and virtualization.

The interface has the following key attributes:

- Does not require uncachable / MMIO register reads in the command submission or completion path;
- A maximum of one MMIO register write is necessary in the command submission path;
- Support for up to 65,535 I/O Queues, with each I/O Queue supporting up to 65,535 outstanding commands;
- Priority associated with each I/O Queue with well-defined arbitration mechanism;
- All information to complete a 4 KiB read request is included in the 64B command itself, ensuring efficient small I/O operation;
- Efficient and streamlined command set;
- Support for MSI/MSI-X and interrupt aggregation;
- Support for multiple namespaces;
- Efficient support for I/O virtualization architectures like SR-IOV;
- Robust error reporting and management capabilities; and
- Support for multi-path I/O and namespace sharing.

This specification defines a streamlined set of registers whose functionality includes:

- Indication of controller capabilities;
- Status for controller failures (command status is processed via CQ directly);
- Admin Queue configuration (I/O Queue configuration processed via Admin commands); and
- Doorbell registers for scalable number of Submission and Completion Queues.

The NVM Express interface is based on a paired Submission and Completion Queue mechanism. Commands are placed by host software into a Submission Queue. Completions are placed into the associated Completion Queue by the controller. Multiple Submission Queues may utilize the same Completion Queue. Submission and Completion Queues are allocated in memory.

An Admin Submission and associated Completion Queue exist for the purpose of controller management and control (e.g., creation and deletion of I/O Submission and Completion Queues, aborting commands, etc.). Only commands that are part of the Admin Command Set may be submitted to the Admin Submission Queue.

NVM Express, Inc., *NVM Express Base Specification, Revision 1.4*, (June 10, 2019), https://nvmexpress.org/wp-content/uploads/NVM-Express-1_4-2019.06.10-Ratified.pdf [hereinafter “NVM Express Specification”].

Host software submits commands to a controller through pre-allocated Submission Queues. A controller is alerted to newly submitted commands through SQ Tail Doorbell register writes. The difference between the previous doorbell register value and the current register write indicates the number of commands that were submitted.

Upon completion of the command execution by the NVM subsystem, the controller presents completion queue entries to the host through the appropriate Completion Queues. If MSI-X or multiple message MSI is in use, then the interrupt vector indicates the Completion Queue(s) with possible new command completions for the host to process. If pin-based interrupts or single message MSI interrupts are used, host software interrogates the Completion Queue(s) for new completion queue entries. The host updates the CQ Head doorbell register to release Completion Queue entries to the controller and to clear the associated interrupt.

[Express Specification](#) at 274.

52. Defendants' SSD products with NVMe support include an interrupt manager configured to generate a complete queue state for indicating occurrence of a completion queue event associated with the completion queue, as shown below:

1.6.9 controller

A controller is the interface between a host and an NVM subsystem. There are three types of controllers:

- a) I/O controllers;
- b) discovery controllers; and
- c) administrative controllers.

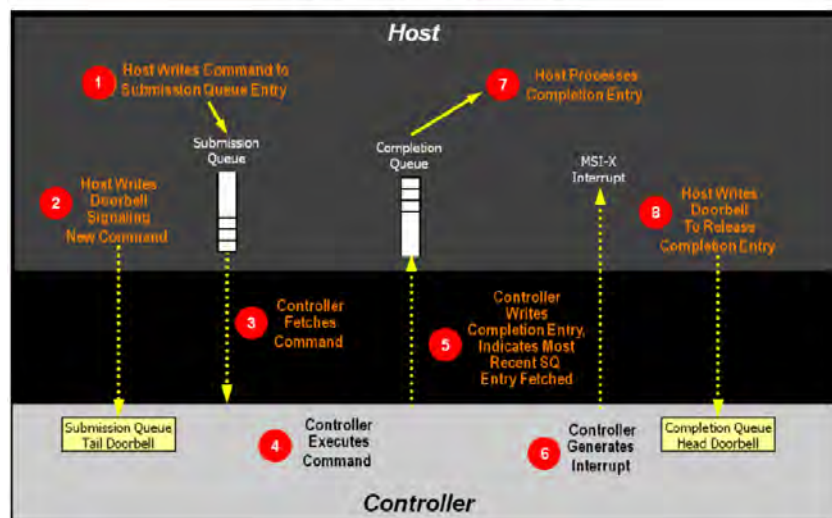
A controller executes commands submitted by a host on a Submission Queue and posts a completion on a Completion Queue. All controllers implement one Admin Submission Queue and one Admin Completion

[NVM Express Specification](#) at 14.

5. After a command has completed execution, the controller places a completion queue entry in the next free slot in the associated Completion Queue. As part of the completion queue entry, the controller indicates the most recent Submission Queue entry that has been consumed by advancing the Submission Queue Head pointer in the completion entry. Each new completion queue entry has a Phase Tag inverted from the previous entry to indicate to the host that this completion queue entry is a new entry;
6. The controller optionally generates an interrupt to the host to indicate that there is a new completion queue entry to consume and process. In the figure, this is shown as an MSI-X interrupt, however, it could also be a pin-based or MSI interrupt. Note that based on interrupt coalescing settings, an interrupt may or may not be generated for each new completion queue entry;
7. The host consumes and then processes the new completion queue entries in the Completion Queue. This includes taking any actions based on error conditions indicated. The host continues consuming and processing completion queue entries until a previously consumed entry with a Phase Tag inverted from the value of the current completion queue entries is encountered; and
8. The host writes the Completion Queue Head Doorbell register to indicate that the completion queue entry has been consumed. The host may consume many entries before updating the associated Completion Queue Head Doorbell register.

[NVM Express Specification](#) at 283.

Figure 432: Command Processing



[NVM Express Specification](#) at 284.

53. Defendants' SSD products with NVMe support include an interrupt manager configured to generate an interrupt vector state based on the complete queue state, which is shown below:

Figure 151: Create I/O Completion Queue – Command Dword 11

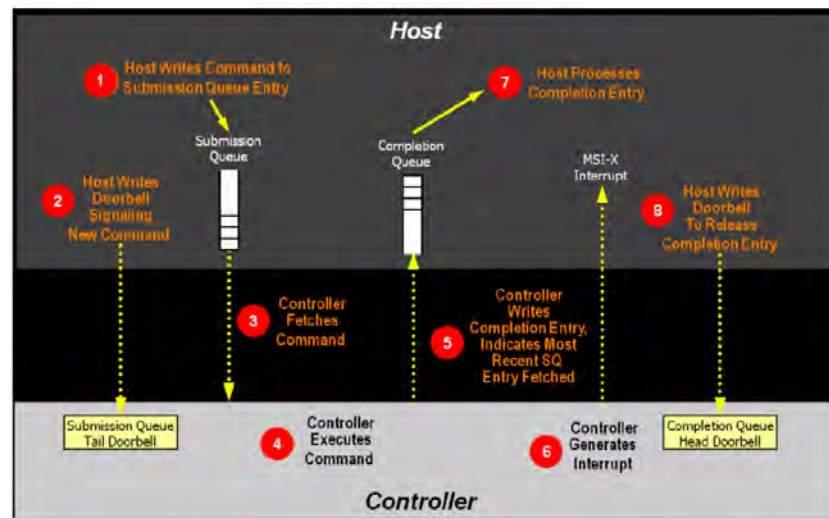
Bits	Description
31:16	Interrupt Vector (IV): This field indicates interrupt vector to use for this Completion Queue. This corresponds to the MSI-X or multiple message MSI vector to use. If using single message MSI or pin-based interrupts, then this field shall be cleared to 0h. In MSI-X, a maximum of 2,048 vectors are used. This value shall not be set to a value greater than the number of messages the controller supports (refer to MSICAP.MC.MME or MSIXCAP.MXC.TS). If the value is greater than the number of messages the controller supports, the controller should return an error of Invalid Interrupt Vector.

[NVM Express Specification](#) at 102.

- After a command has completed execution, the controller places a completion queue entry in the next free slot in the associated Completion Queue. As part of the completion queue entry, the controller indicates the most recent Submission Queue entry that has been consumed by advancing the Submission Queue Head pointer in the completion entry. Each new completion queue entry has a Phase Tag inverted from the previous entry to indicate to the host that this completion queue entry is a new entry.
- The controller optionally generates an interrupt to the host to indicate that there is a new completion queue entry to consume and process. In the figure, this is shown as an MSI-X interrupt, however, it could also be a pin-based or MSI interrupt. Note that based on interrupt coalescing settings, an interrupt may or may not be generated for each new completion queue entry.
- The host consumes and then processes the new completion queue entries in the Completion Queue. This includes taking any actions based on error conditions indicated. The host continues consuming and processing completion queue entries until a previously consumed entry with a Phase Tag inverted from the value of the current completion queue entries is encountered; and
- The host writes the Completion Queue Head Doorbell register to indicate that the completion queue entry has been consumed. The host may consume many entries before updating the associated Completion Queue Head Doorbell register.

[NVM Express Specification](#) at 283.

Figure 432: Command Processing

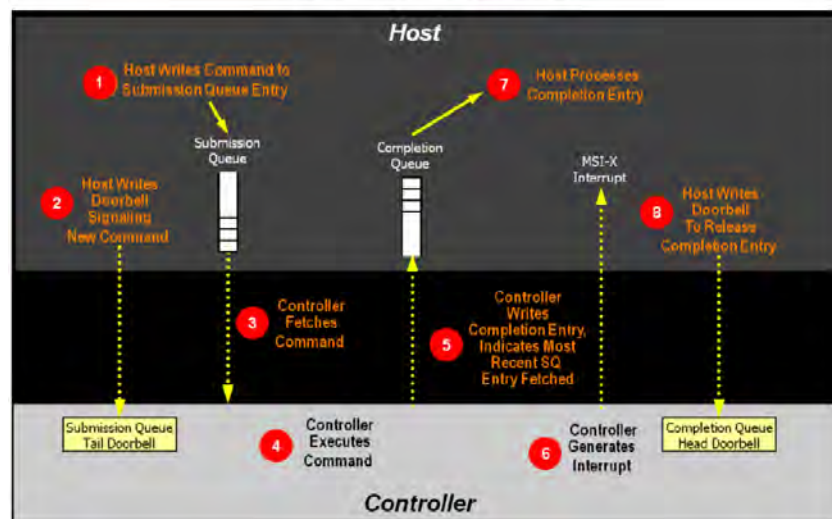


[NVM Express Specification](#) at 284.

54. The Accused Products with NVMe support include an interrupt manager configured to determine whether the completion queue of the host processing unit contains an unprocessed completion state based on the interrupt vector state. The interrupt manager is further configured to generate an interrupt message packet for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue. This is shown in the images below:

- The controller optionally generates an interrupt to the host to indicate that there is a new completion queue entry to consume and process. In the figure, this is shown as an **MSI-X interrupt**, however, it could also be a pin-based or MSI interrupt. Note that based on interrupt coalescing settings, an interrupt may or may not be generated for each new completion queue entry;
- The host consumes and then processes the new completion queue entries in the Completion Queue. This includes taking any actions based on error conditions indicated. The host continues consuming and processing completion queue entries until a previously consumed entry with a Phase Tag inverted from the value of the current completion queue entries is encountered; and
- The host writes the Completion Queue Head Doorbell register to indicate that the completion queue entry has been consumed. The host may consume many entries before updating the associated Completion Queue Head Doorbell register.

Figure 432: Command Processing



[NVM Express Specification](#) at 283-284.

55. The nonvolatile memory controller, which generates an MSI-X interrupt, is transmitted as a PCIe message packet. This is demonstrated in the quote below:

NVMe, which connects to your laptop or desktop PC via the PCIe® interface, can hit speeds as high as 7.5GB per second. Compare this to SATA, which typically tops out at 500MB per second.

[Internal SSD.](#)

PCI Express Base Specification Revision 2.1 (March 4, 2009), [hereinafter “PCIe v2.1”].

Message Signaled Interrupt (MSI/MSI-X) Two similar but separate mechanisms that enable a Function to request service by writing a system-specified DWORD of data to a system-specified address, using a Memory Write Request. Compared to MSI, MSI-X supports a larger maximum number of vectors and independent message address and data for each vector.

Packet A fundamental unit of information transfer consisting of a header that, in some cases, is followed by a data payload.

PCIe v2.1 at 31.

Transaction Layer The Layer that operates at the level of transactions (for example, read, write).

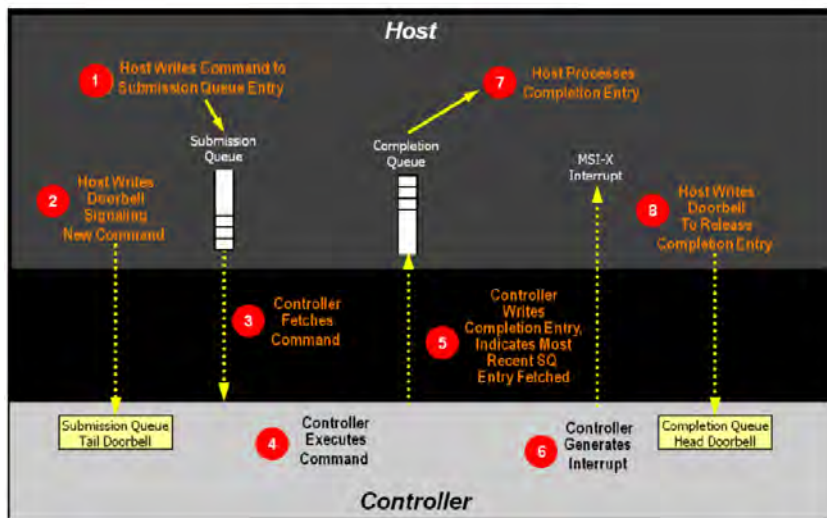
Transaction Layer Packet, TLP A Packet generated in the Transaction Layer to convey a Request or Completion.

PCIe v2.1 at 33.

56. The image below shows a completion queue state includes a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue.

6. The controller optionally generates an interrupt to the host to indicate that there is a new completion queue entry to consume and process. In the figure, this is shown as an MSI-X interrupt, however, it could also be a pin-based or MSI interrupt. Note that based on interrupt coalescing settings, an interrupt may or may not be generated for each new completion queue entry;
7. The host consumes and then processes the new completion queue entries in the Completion Queue. This includes taking any actions based on error conditions indicated. The host continues consuming and processing completion queue entries until a previously consumed entry with a Phase Tag inverted from the value of the current completion queue entries is encountered; and
8. The host writes the Completion Queue Head Doorbell register to indicate that the completion queue entry has been consumed. The host may consume many entries before updating the associated Completion Queue Head Doorbell register.

Figure 432: Command Processing



[NVM Express Specification](#) at 283-284.

57. Defendants have directly infringed, and continue to infringe, the claims of the '968 Patent in the United States, by making, using, offering for sale, selling, and/or importing the Accused Products in violation of 35 U.S.C. § 271(a). For example, Defendants provide SSD products configured with the hardware and software that satisfy the limitations of at least claim 1. Defendants further directly infringe the '968 Patent when its SSD products with NVMe are installed and operated

1 by its employees in a computer system, such as for gaming, personal computing, or
2 data centers. Direct infringement further occurs when Defendants' employees use
3 and test the hardware and software.

4 58. Defendants also have infringed, and continue to infringe the claims of
5 the '968 Patent by actively inducing others to use the Accused Products. Defendants'
6 users, customers, agents or other third parties who use the Accused Products in
7 accordance with Defendants' instructions infringe the claims of the '968 Patent, in
8 violation of 35 U.S.C. § 271(a). Defendants induce its customers to use its SSD
9 products with NVMe for the benefits of higher performance, reduced size and power,
10 and increased reliability compared to SSD products with other interfaces, such as
11 SATA. Defendants are thereby liable for infringement of the '968 Patent under 35
12 U.S.C. § 271(b).

13 59. Defendants' users, customers, agents or other third parties who use the
14 Accused Products in accordance with Defendants' instructions infringe the claims of
15 the '968 Patent, in violation of 35 U.S.C. § 271(b). Defendants intentionally instruct
16 its customers to infringe through support information, demonstrations, brochures,
17 videos, and user guides, such as those located at:

18 <https://www.westerndigital.com/support;>

19 <https://support.wdc.com/contact.aspx?lang=en;>

20 <https://www.westerndigital.com/support/category-selection;>

21 https://www.youtube.com/channel/UC_M0BIntDVSblWg6ggUa7UQ;

22 <https://www.youtube.com/watch?v=L0zZtwRFj0E;>

23 <https://www.youtube.com/westerndigital>; and

24 [https://www.youtube.com/c/westerndigitalcorporation.](https://www.youtube.com/c/westerndigitalcorporation)

25 60. Defendants are on notice of its infringement by no later than the filing
26 and service of this Complaint. By the time of trial, Defendants will have known and
27 intended (since receiving such notice) that its continued actions would actively
28

1 induce to the infringement of the '968 Patent. Defendants were further aware of the
2 '968 Patent because it was cited as prior art by Western Digital in U.S. Patent Nos.
3 10,725,835, 10,296,249, 10,452,278, 10,466,903, and 10,509,569, which are all
4 assigned to Western Digital.

5 61. On January 23, 2024, Plaintiff sent a notice letter to Western Digital,
6 notifying them that they were infringing the Asserted Patents. Western Digital's
7 infringement of the '968 Patent has been willful and intentional under the standard
8 announced in *Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 579 U.S. 93 (2016). Western
9 Digital has not replied to this letter.

10 62. Western Digital has willfully infringed the '968 Patent by refusing to
11 take a license and continuing to make, use, test, sell, license, and/or offer for
12 sale/license the '968 Patent Accused Products. Instead of taking a license, Western
13 Digital has opted to make the business decision to "efficiently infringe" the '968
14 Patent. In doing so, Western Digital willfully infringes the '968 Patent.

15 63. Defendants are liable as contributory infringers of the '968 Patent under
16 35 U.S.C. § 271(c) by having offered to sell, sold and imported and continuing to
17 offer to sell, selling, and importing into the United States its SSD products that
18 support NVMe, to be especially made or adapted for use in an infringement of the
19 '968 Patent. Defendants' SSD products are key components in gaming consoles and
20 gaming PCs, computers, everyday PCs, Network Attached Storage (NAS) devices,
21 servers and data centers. These SSD products are material components for use in
22 practicing the '968 Patent and are specifically made and are not a staple article of
23 commerce suitable for substantial noninfringing use. Defendants supplied these
24 components with knowledge of the '968 Patent and with knowledge that these
25 components constitute material parts of the claimed inventions of the '968 Patent.

26 64. As a result of Defendants' infringement of the '968 Patent, Plaintiff has
27 suffered monetary damages and is entitled to no less than a reasonable royalty for
28 Defendants' use of the claimed inventions of the '968 Patent, together with interest

1 and costs as determined by the Court. Plaintiff will continue to suffer damages in the
2 future.

3 65. Defendants' acts of direct and indirect infringement have caused and
4 continue to cause damage to Plaintiff. Plaintiff is entitled to damages in accordance
5 with 35 U.S.C. §§ 271 and 281 sustained as a result of Defendants' wrongful acts in
6 an amount to be proven at trial.

7 **COUNT II**

8 (INFRINGEMENT OF U.S. PATENT NO. 9,183,085)

9 66. Plaintiff incorporates by reference and re-alleges the foregoing
10 paragraphs as fully set forth herein.

11 67. Defendants have directly infringed and continue to directly infringe the
12 '085 Patent, literally and/or under the doctrine of equivalents, by making, using,
13 offering for sale, selling, and/or importing into the United States its SSD products.
14 Defendants directly infringe claim 1 of the '085 Patent when its SSD products are
15 installed and operated by its employees in a computer system, such as for gaming,
16 personal computing, or data centers. Defendants directly infringe claim 1 when
17 Defendants' employees use and test its SSD products.

18 68. Claim 1 of the '085 Patent reads as follows:

19 1. A method of selecting an error correction coding (ECC)
20 scheme, the method comprising:

21 determining a bit error rate associated with a region
22 comprising a fixed number of two or more flash memory
23 pages or integer fractions thereof, wherein the two or more
24 flash memory pages of a region can be read
simultaneously, wherein the region stores at least data
payload and primary and secondary ECC parity symbols
corresponding to the data payload of the region;

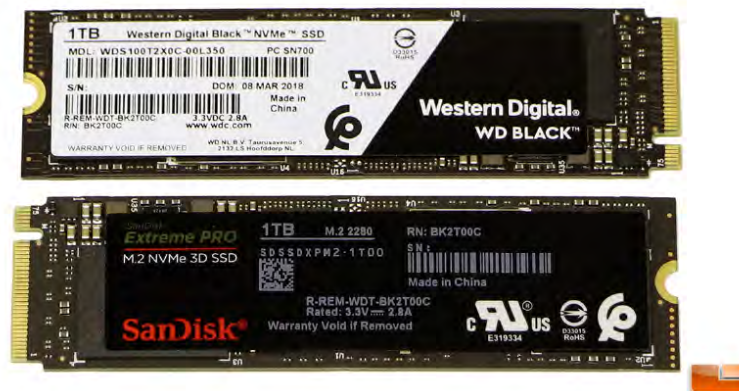
25 comparing the determined bit error rate to one or more
26 predetermined thresholds corresponding to a set of
27 predefined gears comprising at least a first gear and a
28 second gear, wherein the predefined gears correspond to
different predefined ECC schemes, wherein the first gear
has a different data payload size and correction capability
than the second gear, wherein the amount of memory space
allocated for the storage of data payload within the region

varies between the first gear and the second gear to accommodate a varying number of parity symbols between the first gear and the second gear; and

selecting a gear from the set for the region based at least partly on the comparisons to the one or more predetermined thresholds;

wherein determining, comparing, and selecting are performed by an integrated circuit.

69. Defendants' SSD products perform a method of selecting an error correction coding (ECC) scheme. For example, WD Black-branded SSDs, which are used for gaming consoles and gaming PCs, Blue- and Green-branded SSDs, which are used for everyday PCs, Red-branded SSDs, which are used for Network Attached Storage (NAS), and Gold- and Ultrastar SSDs, which are used for data centers, all perform a method of selecting an error correction coding (ECC) scheme, as shown below:



Western Digital's new controller architecture means that the company has in-house development from the controller to the NAND. This gives WD tremendous design flexibility and they believe this new PCIe Gen 3 x4 controller is scalable and future-ready (think QLC NAND). Since WD designed everything they were able to design for low power and low latency as well as general performance. WD's new controller has three cores, is built on the 28nm process, features nCache 3.0 (marketing term for SLC Cache) for enhanced burst speeds, multi-gear LDPC (low-density parity-check) and hardware ECC to provide full SRAM and DRAM bit correction.

[WD Black and SanDisk Review.](#)

The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read

ECC/DSP White Paper at 5.

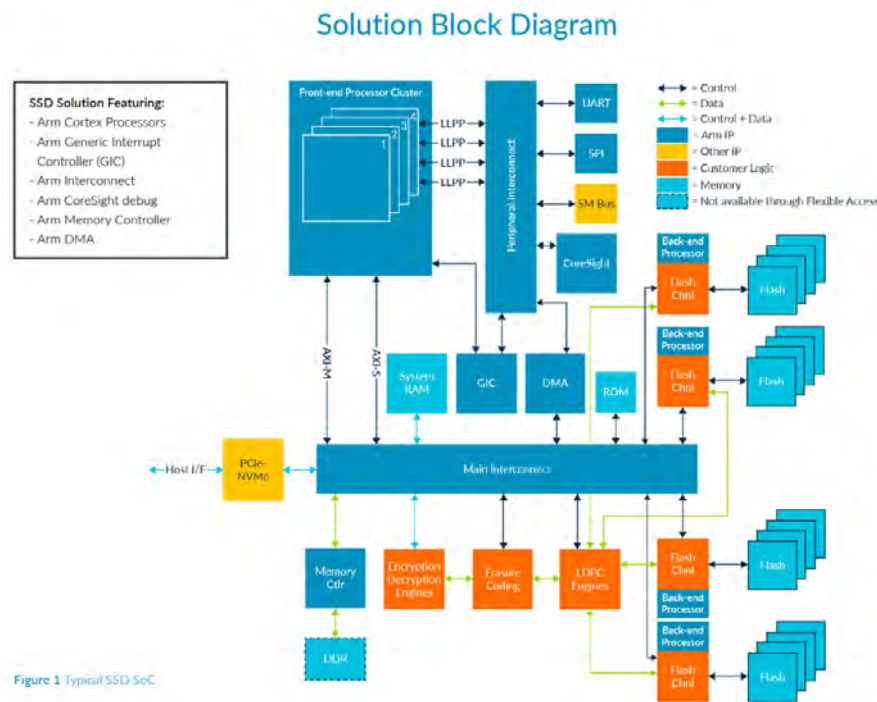
70. The Accused Products determine a bit error rate (BER) associated with a region comprising a fixed number of two or more flash memory pages or integer fractions thereof, as demonstrated in the images below:

The Sentinel ECC&DSP LDPC engine is generic and can support different memory types (SLC, MLC, TLC, QLC) in terms of the page size and ECC redundancy. The Sentinel ECC&DSP LDPC codes provide near Shannon limit correction capability and therefore maximize the supported operational specs (endurance, retention, disturb resilience, quality of service, etc.) for a given ECC overprovisioning in the NAND. The Sentinel ECC&DSP LDPC decoder is based on a proprietary multi-gear architecture, which optimizes the power consumption under variable BER observed across memory pages, operational conditions and memory lifetime. It supports multiple read

Idan Alrod et al., *The Application of ECC/DSP to Flash Memory* (Mar. 2021), Western Digital, https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-the-application-of-ecc-dsp-to-flash-memory.pdf [hereinafter “ECC/DSP White Paper”].

To power the SSD, Western Digital uses a proprietary Arm-based multi-core eight-channel PCIe 4.0 x4 NVMe SSD controller that leverages a Micron DDR4 DRAM chip to deliver responsive performance. Western Digital references the controller as its WD_BLACK G2. Outfitting the WD Black SN850 with a faster Gen4 PHY is great for performance, but with such fast bandwidth, power draw and heat output were a concern at 28 nm. Thus, WD_BLACK G2 on a newer process node to better control those variables with TSMC’s 16nm FinFET technology.

WD Black SN850 Review.



Front-end processors are usually Cortex-R processors but can sometimes be Cortex-A processors, to support more intensive wear-levelling algorithms.

Wear-levelling is the process of systematically erasing and writing all NAND flash locations, to ensure all locations wear out at about the same time. It may require moving unchanging data (cold data) already stored so a block can be erased and rewritten with rapidly changing data (hot data).

Flash Translation Layer (FTL)

The **front-end processors** are responsible for maintaining the FTL tables that map logical addresses to physical addresses. As part of the FTL, the front-end processors also handle wear-levelling algorithms to determine where the data should be written, which data should move, and which locations require garbage collection.

Read Requests and Write Requests

Read and write requests arrive from the host over the **PCIe/NVMe** interface. The requests arrive in the form of descriptors that describe the parameters of a transfer. Write requests also carry the data to be written. These descriptors are written to either the DDR memory or a system RAM using a **DMA** operation from the host. For write requests, the user data is transferred to the controller DDR using a separate DMA operation.

Arm Storage Solution for SSD Controllers at 4.

1 A front-end processor is notified about the arrival of this descriptor. It then parses the
2 descriptor to modify some of the parameters. In particular, the Logical Block Address (LBA)
3 provided by the host must be modified to the physical address in the NAND where the
4 read data is stored. With the correct physical address, the descriptor can be dispatched
5 to the appropriate **flash channel** using a DMA.

6 For read requests, the flash channel issues a read operation to the appropriate NAND
7 die. When the data is available, it is moved from the NAND die buffer to the flash channel
8 and then to the LDPC engines, as space is available. The **LDPC engines** perform ECC
9 correction and data recovery from the media. If necessary, erasure coding operations
10 are performed to recover data lost due to a block or page failure. Encrypted data is
11 decrypted and stored in controller DDR. Finally, the user data is moved to host memory
12 using a DMA operation to write into the DDR of the host, and then the host is notified
13 that the data transfer completed.

14 For write requests, the user data in DDR is sent to the SSD data path of encryption,
15 erasure coding, and LDPC encoding. When the encoded user data reaches the flash channel,
16 the flash channel issues an operation to write the data to the NAND buffers. When all
17 the data is in the NAND buffer, a program operation is issued to program the NAND. A
18 completion response is generated by the flash channel that is sent back to the host.

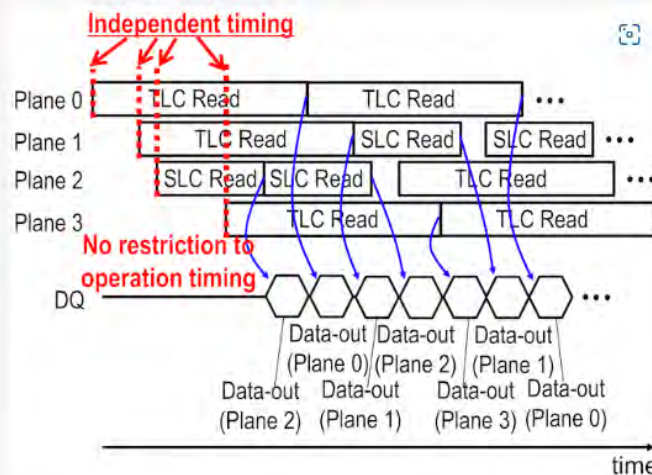
19 [Arm Storage Solution for SSD Controllers](#) at 5.

20 71. The highlighted text below shows The Accused Products support
21 reading two or more memory pages of a region simultaneously.

22 Another important aspect, especially for enterprise grade solutions, is to maintain quality of service (QoS). This
23 means that the delay of providing the host with response for any command falls under tight profile of probabilities
24 it is allowed to exceed certain latency numbers. In order to meet such harsh requirements the ECC engine in gears
25 1,2,3 is segregated in a manner that it can serve separate requests in separate gears simultaneously. In case a single
26 command requires higher latency gear-3 decoding, a different command can be attended simultaneously with
27 Gear-1 engine. Together with out of order processing and host PCIe™ interface using NVMe protocol the Sentinel
28 ECC&DSP technology is tailored to serve QoS in near optimal manner.

[ECC/DSP White Paper](#) at 7.

Now, another restriction on multi-plane operations is being relaxed: the timing of read operations in different planes doesn't need to line up. This makes it possible for one plane to perform multiple reads from SLC pages while another plane is performing a single slower read from TLC or QLC pages. This capability is called Asynchronous Independent (Multi-)Plane Read. The practical effect is that for read operations, a large 4-plane die can now match the performance of four smaller 1-plane dies. This mitigates many of the performance downsides that higher per-die capacity brings to SSDs that only have one or two dies per channel.



Billy Tallis, *2021 NAND Flash Updates from ISSCC: The Leaning Towers of TLC and QLC*, AnandTech (Feb. 19, 2021), <https://www.anandtech.com/show/16491/flash-memory-at-isscc-2021>.

72. The Accused Products can store in a region at least data payload and primary and secondary ECC parity symbols corresponding to the data payload of the region, as shown in the highlighted text below:

Error Detection and Correction

One of the key factors to increase flash reliability as well as write endurance is the implementation of an Error Detection and Correction mechanism. The three most popular Error Correction algorithms used with NAND flash technology today are:

- BCH (Bose, Ray-Chaudhuri, Hocquenghem): BCH codes were invented in 1959 by Hocquenghem, and independently in 1960 by Bose and Ray Chaudhuri.
- LDPC (Low Density Parity Codes) invented by Gallager in 1961.

The maximum number of errors that can be detected and corrected is determined by the algorithm. No matter what algorithm is used within the ECC engine of a NAND flash controller, the method of error detection and correction remains the same:

1. Every time a page of data is written to the flash, data is passed through the controller's ECC Engine to create a unique ECC signature.
2. The data and ECC signature are stored together on the flash; the data in the page area, the ECC signature in the spare area.
3. When reading the data back, both data and stored ECC signature are read into the controller. A new ECC signature is generated, based upon the read-back data.
4. The newly created ECC signature is then compared to the original stored ECC signature. If both signatures are the same, no errors have occurred, and the data will be provided to the host. If the two signatures differ, the data will be corrected by the controller before being provided to the host.

Some flash controllers will write the corrected data back to the flash to optimize reliability, while others will not, since there is no guarantee that the data will not show errors again in the future. For 4KB page flash, typically 8 ECC signatures are created when writing data to the flash; one for each 512 bytes of data, as shown in Figure 10.

Western Digital, *Flash 101 and Flash Management* (Sep. 2023), https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-sandisk-flash101-management.pdf [hereinafter "Flash 101 White Paper"].

The figure shows a 4KB page with data payload of 4096 data payload and an associated spare area of 128 bytes of ECC bytes containing both primary and

secondary ECC bits.



Figure 10: Four ECC signatures for 4KB page

[Flash 101 White Paper](#) at 7.

73. The image below shows how The Accused Products compare the determined bit error rate (BER) to one or more predetermined thresholds corresponding to a set of predefined gears comprising at least a first gear and a second gear, wherein the predefined gears correspond to different predefined ECC schemes.

In this example, three decoding gears are used. The color-coding is used to show the BER regions where each gear is likely to succeed the decoding.

Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear-1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in.

The blue curve in Figure 5 indicates the throughput of the system. Naturally, once NAND approaches the BER point where the 2nd gear kicks in, the throughput declines rapidly assuming constant power consumption is maintained.

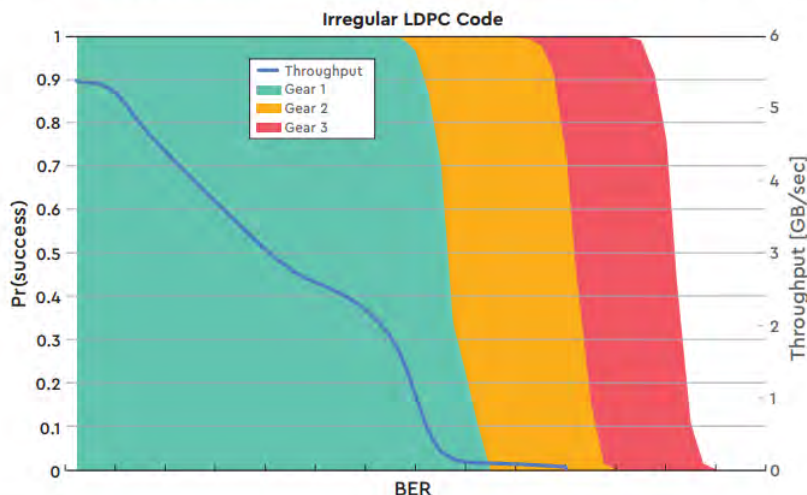
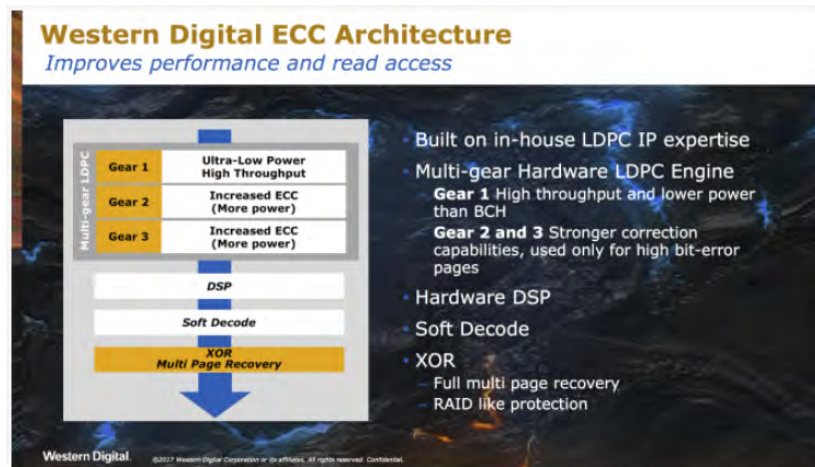


Figure 5: Example of various decoding gears correction capability and overall performance

When the BER is high, there is no point in spending decoder time trying to decode with lower gears, as this would only degrade performance by adding unnecessary latency to the decoding sequence. Consequently, the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear.

[ECC/DSP White Paper](#) at 6.

74. The Accused Products include a first gear with a different data payload size and correction capability than a second gear. For example, Gear 1 corresponds to a high throughput and a ECC level while Gear 2 corresponds to a lower throughput and an increased ECC level (i.e., different payload size and correction capability), as shown in the image below:



Ganesh T S & Billy Tallis, The Western Digital NVMe Architecture - NAND & Controller, *The Western Digital WD Black 3D NAND SSD Review: EVO Meets Its Match*, AnandTech (Apr. 5, 2018), <https://www.anandtech.com/show/12543/the-western-digital-wd-black-3d-nand-ssd-review/2> [hereinafter “WD Black 3D Review”].

See also U.S. Patent No. 11,527,300, *Level Dependent Error Correction Code Protection in Multi-Level Non-Volatile Memory*, by Yang et al., assigned to Western Digital [hereinafter “Yang”], describing the adjustment of payload size and ECC parity size (correction capability) based on BER, corresponding to the criteria for selecting the “gear”.

FIG. 12 illustrates an ECC codeword 1200 and a dynamic or variable size of Components of the ECC codeword in accordance with one embodiment. The ECC codeword 1200 may comprise a payload and a parity section as introduced in FIG. 6A through FIG. 6C. The payload size 1202 and parity size 1204 of the ECC codeword 1200 may vary as indicated by the dotted lines. “Payload size” refers to a size measured in data storage units for a payload of an

1 ECC codeword. In one embodiment, a data storage unit is
2 equal in size to a data sector. “Parity size” refers to a size
3 measured in bits or bytes, or some other data storage
4 measurement unit, for a parity section. The unit of measure
5 for a parity size may depend on the ECC method being used
6 to encode and decode the ECC codewords.

7 Yang at 33:12-39.

8 Determining the coding rate may comprise increasing the
9 payload size 1202 in response to an attribute indicating a
10 greater data integrity for data stored on the multi-level page
11 that is assigned to the ECC codeword 1200. In particular,
12 the payload size 1202 may be increased, and the parity size
13 1204 decreased, based on the data integrity of the ECC
14 codeword 1200 being higher in relation to other multi-level
15 pages that will be stored on the same multi-level storage
16 cells. Alternatively, or in addition, the payload size 1202
17 may be decreased, and the parity size 1204 increased, based
18 on the data integrity of the ECC codeword 1200 being
19 lower in relation to other multi-level pages that will be
20 stored on the same multi-level storage cells.

21 Yang at 34:4-16.

22 75. The image below shows how The Accused Products allocate memory
23 space for the storage of data payload within the region varies between the first gear
24 and the second gear to accommodate a varying number of parity symbols between
25 the first gear and the second gear. The memory space allocated for the storage of data
26 payload is reduced as the flash controller transitions into a higher gear. The reduction
27 of storage for data payload is caused by the increased of parity bits required by a
28 more complex ECC used in higher gears.

The blue curve in Figure 5 indicates the throughput of the system. Naturally, once NAND approaches the BER point where the 2nd gear kicks in, the throughput declines rapidly assuming constant power consumption is maintained.

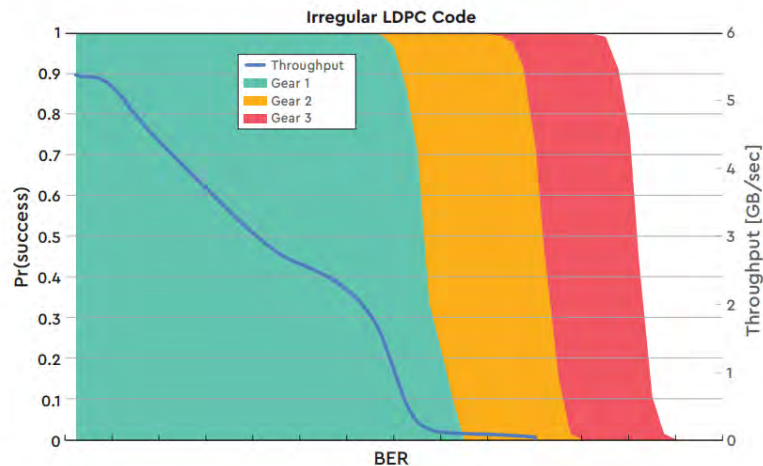
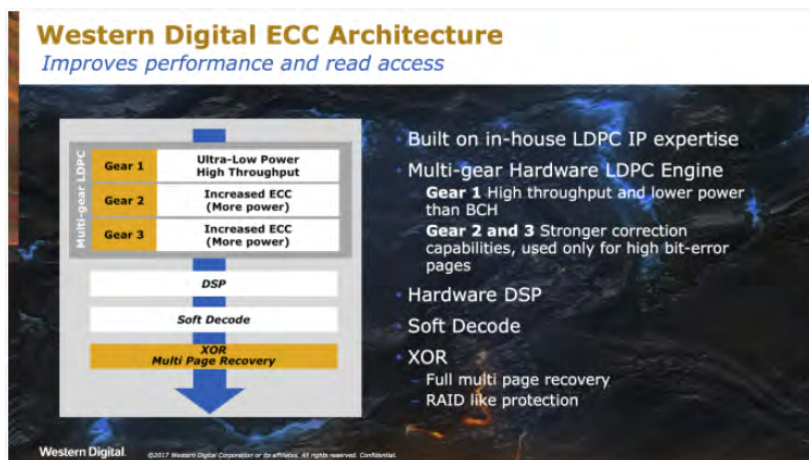


Figure 5: Example of various decoding gears correction capability and overall performance

When the BER is high, there is no point in spending decoder time trying to decode with lower gears, as this would only degrade performance by adding unnecessary latency to the decoding sequence. Consequently, the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear.

[ECC/DSP White Paper](#) at 6.



[WD Black 3D Review](#).

See also [ECC/DSP White Paper](#) at 11 ("This feature is set to accommodate full usage of the available NAND cells in the physical page while enabling flexibility in code rate for numerous applications / scenarios.").

See also [Yang](#), assigned to Western Digital.

1 In certain embodiments, the payload size 1202 and parity
2 size 1204 may be adjusted based on a data integrity
3 attribute for a particular non-volatile storage media, storage
4 cell, set of storage cells or the like. "Data integrity" refers
5 to an attribute or measure of data, or a data sample,
6 indicating whether the data is accurate, not erroneous, and
7 unchanged from a prior transmission or recording of the
8 data. In certain embodiments, data integrity is an objective
9 characteristic. In other embodiments, data integrity may be
10 expressed in relation to a spectrum in which one end
11 represents no, or very low data integrity and the opposite
12 end represents perfect, or very high data integrity.

13 [Yang](#) at 33:45-56.

14 The receiver 1304 may coordinate with the address
15 allocator 1306 to determine where the write data 1312 will
16 be stored. The address allocator 1306 may determine a
17 multilevel page to store a set of data blocks associated with
18 a set of write commands 1310. "Address allocator" refers
19 to any circuit, sub-circuit, electronic component, hardware,
20 software, firmware, module, logic, device, or apparatus
21 configured, programmed, designed, arranged, or
22 engineered to determine, assign and/or allocate a physical
23 block address for a particular logical block address.

24 The packetizer 1308 may coordinate with the receiver 1304
25 and address allocator 1306 to prepare the write data 1312
26 for storage on the non-volatile storage media. "Packetizer"
27 refers to any hardware, software, firmware, circuit,
28 component, module, logic, device, or apparatus
configured, programmed, designed, arranged, or
engineered to organize a set of source data into one or more
data packets. In one embodiment, the source data may
comprise user data for one or more storage operations. The
packetizer may be configured to include a header, footer
and/or redundancy data in each data packet. The packetizer
may be configured to include padding data or filler data to
combine with a remainder of the source data that does not
completely fill a data packet.

The packetizer 1308 may combine the write data 1312 for
the set of data blocks into a payload for an ECC codeword.
The packetizer 1308 may coordinate with the address
allocator 1306 to determine which multi-level page a
particular ECC codeword is assigned to be stored on. Based
on a determined multi-level page for the particular ECC
codeword, the packetizer 1308 may change a payload size
for the payload of the particular ECC codeword in response
to a reliability attribute of the determined multi-level page
satisfying a threshold.

[Yang](#) at 34:62-35:28.

76. The Accused Products select a gear from the set for the region based at least partly on the comparisons to the one or more predetermined thresholds, as shown in the image and highlighted text below:

In this example, three decoding gears are used. The color-coding is used to show the BER regions where each gear is likely to succeed the decoding.

Gear 1 (the green region in Figure 5 below) is based on the bit-flipping decoder mentioned above. Said Gear 1 is characterized by high-energy efficiency (low J/GB/sec). However, as the BER goes up, it fails at some point to decode with high probability. At that point, the higher resolution decoding gears kicks in.

The blue curve in Figure 5 indicates the throughput of the system. Naturally, once NAND approaches the BER point where the 2nd gear kicks in, the throughput declines rapidly assuming constant power consumption is maintained.

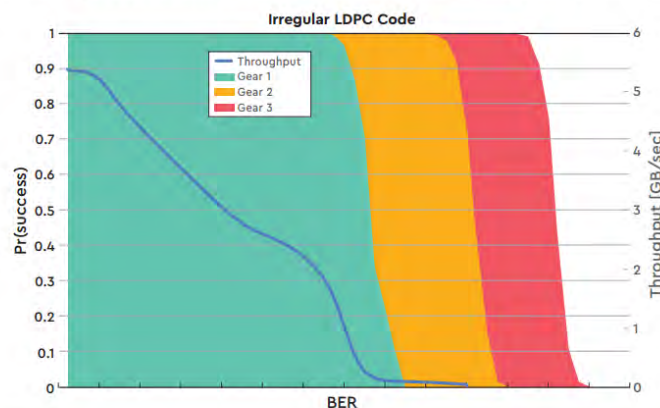


Figure 5: Example of various decoding gears correction capability and overall performance

When the BER is high, there is no point in spending decoder time trying to decode with lower gears, as this would only degrade performance by adding unnecessary latency to the decoding sequence. Consequently, the LDPC engine estimates the BER of the noisy page as part of its initialization process by counting the number of unsatisfied parity checks. This forms the basis on which it automatically chooses the appropriate decoding gear.

[ECC/DSP White Paper](#) at 6.

77. The Accused Products determine, compare and select using an integrated circuit.

Furthermore, the parallelism of each decoding gear is dimensioned according to its usage probability (given the memory BER distribution) and the overall required decoding throughput. Thus, the number of costly high-resolution processing units instantiated for the full resolution BP decoder, which is rarely used ("safety net"), could be much lower than the number of simple BF processing units. This approach significantly reduces the ASIC footprint with a negligible impact on overall sustained decoding throughput.

[ECC/DSP White Paper](#) at 7.

78. Defendants have infringed, and continue to infringe, the claims of the '085 Patent in the United States, by making, using, offering for sale, selling, and/or importing the Accused Products in violation of 35 U.S.C. § 271(a). For example, Defendants directly infringe at least claim 1 of the '085 Patent when its SSD products are installed and operated by its employees in a computer system, such

1 as for gaming, personal computing, or data centers, and when Defendants' employees
2 use and test its SSD products.

3 79. On January 23, 2024, Plaintiff sent a notice letter to Western Digital,
4 notifying them that they were infringing the Asserted Patents. Western Digital's
5 infringement of the '085 Patent has been willful and intentional under the standard
6 announced in *Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 579 U.S. 93 (2016). Western
7 Digital did not reply to that letter.

8 80. Western Digital has willfully infringed the '085 Patent by refusing to
9 take a license and continuing to make, use, test, sell, license, and/or offer for
10 sale/license the '085 Patent Accused Products. Instead of taking a license, Western
11 Digital has opted to make the business decision to "efficiently infringe" the '085
12 Patent. In doing so, Western Digital willfully infringes the '085 Patent.

13 81. Defendants also have infringed, and continue to infringe the claims of
14 the '085 Patent by actively inducing others to use the Accused Products. Defendants'
15 users, customers, agents or other third parties who use the Accused Products in
16 accordance with Defendants' instructions infringe the claims of the '085 Patent, in
17 violation of 35 U.S.C. § 271(a). Defendants induce its customers to use its SSD
18 products for the benefits of higher performance, reduced size and power, and
19 increased reliability compared to other SSD products. Defendants are thereby liable
20 for infringement of the '085 Patent under 35 U.S.C. § 271(b).

21 82. Defendants' users, customers, agents or other third parties who use the
22 Accused Products in accordance with Defendants' instructions infringe the claims of
23 the '085 Patent, in violation of 35 U.S.C. § 271(b). Defendants intentionally instruct
24 its customers to infringe through support information, demonstrations, brochures,
25 videos, and user guides, such as those located at:

26 <https://www.westerndigital.com/support>;

27 <https://support.wdc.com/contact.aspx?lang=en>;

28 <https://www.westerndigital.com/support/category-selection>;

1 https://www.youtube.com/channel/UC_M0BlntDVSblWg6ggUa7UQ;
2 <https://www.youtube.com/watch?v=L0zZtwRFj0E;>
3 <https://www.youtube.com/westerndigital>; and
4 <https://www.youtube.com/c/westerndigitalcorporation>.

5 83. Defendants are liable as contributory infringers of the '085 Patent under
6 35 U.S.C. 271(c) by having offered to sell, sold and imported and continuing to offer
7 to sell, selling, and importing into the United States its SSD products, to be especially
8 made or adapted for use in an infringement of the '085 Patent. Defendants' SSD
9 products are key components in gaming consoles and gaming PCs, computers,
10 everyday PCs, Network Attached Storage (NAS) devices, servers and data centers.
11 These SSD products are material components for use in practicing the '085 Patent
12 and are specifically made and are not a staple article of commerce suitable for
13 substantial noninfringing use. Defendants supplied these components with
14 knowledge of the '085 Patent and with knowledge that these components constitute
15 material parts of the claimed inventions of the '085 Patent.

16 84. As a result of Defendants' infringement of the '085 Patent, Plaintiff has
17 suffered monetary damages and is entitled to no less than a reasonable royalty for
18 Defendants' use of the claimed inventions of the '085 Patent, together with interest
19 and costs as determined by the Court. Plaintiff will continue to suffer damages in the
20 future.

21 85. Defendants are on notice of its infringement by no later than the filing
22 and service of this Complaint. By the time of trial, Defendants will have known and
23 intended (since receiving such notice) that their continued actions would actively
24 induce the infringement of the '085 Patent.

25 86. Defendants' acts of direct and indirect infringement have caused and
26 continue to cause damage to Plaintiff. Plaintiff is entitled to damages in accordance
27 with 35 U.S.C. §§ 271 and 281 sustained as a result of Defendants' wrongful acts in
28 an amount to be proven at trial.

COUNT III

(INFRINGEMENT OF U.S. PATENT NO. 8,601,346)

87. Plaintiff incorporates by reference and re-alleges the foregoing paragraphs as fully set forth herein.

88. Defendants have directly infringed, and continue to directly infringe, one or more claims of the '346 Patent, including at least claim 1 of the '346 Patent, literally and/or under the doctrine of equivalents, by or through making, using, offering for sale, selling within the United States and/or importing into the United States its SSD products.

89. Claim 1 of the '346 Patent reads as follows:

1. A nonvolatile memory controller for performing a data stripe operation on a plurality of data blocks, the nonvolatile memory controller comprising:

a plurality of command processing units, each command processing unit of the plurality of command processing units configured to receive a command of a plurality of commands for performing the data stripe operation, the plurality of commands including a plurality of data update commands and a parity write command, each command processing unit of the plurality of command processing units receiving a data update command of the plurality of data update commands configured to request a data block of the plurality of data blocks based on the data update command, receive the data block in response to the request, and write the data block to a nonvolatile memory device; and

a parity calculator coupled to the plurality of command processing units, the parity calculator further comprising a context memory including a page frame, the parity calculator configured to receive the plurality of data blocks as a sequence of data blocks, to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer, the command processing unit receiving the parity write command configured to write the parity block to a nonvolatile memory based on the parity write command.

90. Defendants make, use, sell, offer for sale and import SSD products that include a nonvolatile memory controller for performing a data stripe operation on a plurality of data blocks. For example, WD Black-branded SSDs, which are used for gaming consoles and gaming PCs, Blue- and Green-branded SSDs, which are used for everyday PCs, Red-branded SSDs, which are used for Network Attached Storage (NAS), and Gold- and Ultrastar SSDs, which are used for data centers, all include a nonvolatile memory controller for performing a data stripe operation on a plurality of data blocks, as shown below:



Western Digital's new controller architecture means that the company has in-house development from the controller to the NAND. This gives WD tremendous design flexibility and they believe this new PCIe Gen 3 x4 controller is scalable and future-ready (think QLC NAND). Since WD designed everything they were able to design for low power and low latency as well as general performance. WD's new controller has three cores, is built on the 28nm process, features nCache 3.0 (marketing term for SLC Cache) for enhanced burst speeds, multi-gear LDPC (low-density parity-check) and hardware ECC to provide full SRAM and DRAM bit correction.



1 Nathan Kirsch, *WD Black NVMe 3D and SanDisk Extreme PRO NVMe 3D 1TB*
 2 *SSD Review*, Legit Reviews (Apr. 5, 2018), [https://www.legitreviews.com/wd-](https://www.legitreviews.com/wd-black-nvme-3d-sandisk-extreme-pro-nvme-3d-1tb-ssd-review_204268)
 3 [black-nvme-3d-sandisk-extreme-pro-nvme-3d-1tb-ssd-review_204268](https://www.legitreviews.com/wd-black-nvme-3d-sandisk-extreme-pro-nvme-3d-1tb-ssd-review_204268) [hereinafter
 4 “WD Black and SanDisk Review”].

5 91. The images and quotes below show how The Accused Products include
 6 command processing units, such as ARM processor cores. The processing units
 7 receive commands, including a command to perform a data stripe operation. For
 8 example:

9 The new controller has a tri-core architecture (probably
 10 using Arm Cortex-cores Fabricated in a 28nm process. It is
 11 designed to be scalable – the current controller can
 12 interface with the host using a PCIe 3.0 x4 link, or an x2
 13 link as in the Western Digital SN520. The architecture of
 14 the controller also allows future products using variants to
 15 come to market faster and with newer features. It also
 16 allows Western Digital to segment their NVMe product
 stack. The controller in the Western Digital Black 3D
 NAND SSD is optimized for client workloads including
 PC gaming and high-performance commercial
 applications. Western Digital expects this new controller
 architecture to last at least until NVMe SSDs move beyond
 PCIe 3 x4 interfaces.

17 [WD Black 3D Review.](#)

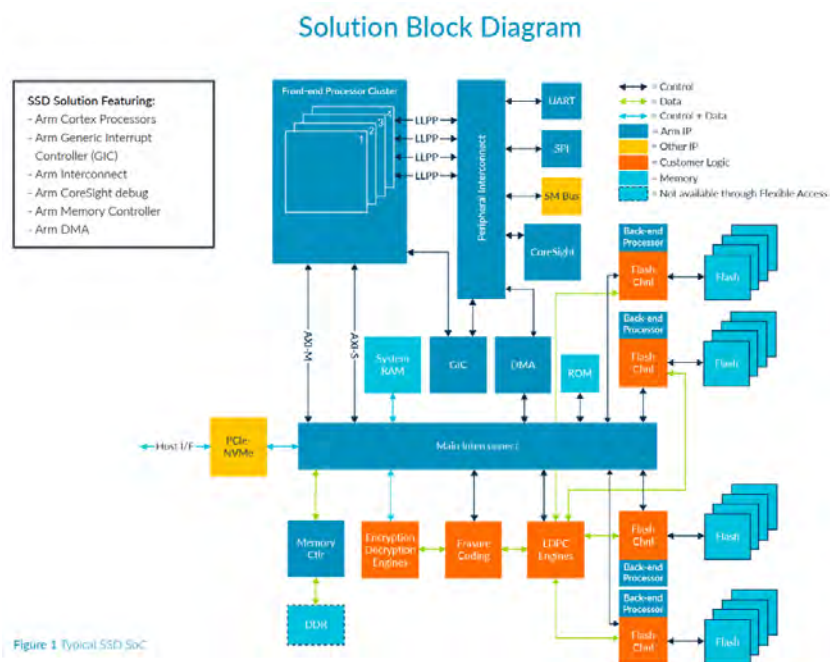
18 WD’s new controller has three cores, is built on the 28nm
 19 process, ...

20 [WD Black and SanDisk Review.](#)

21 To power the SSD, WD uses a proprietary Arm-based
 22 multi-core eight-channel PCIe 4.0 x4 NVMe SSD
 23 controller that leverages a Micron DDR4 DRAM chip to
 24 deliver responsive performance. Western Digital
 25 references the controller as its WD BLACK G2. Outfitting
 26 the Western Digital Black SN850 with a faster Gen4 PHY
 is great for performance, but with such fast bandwidth,
 power draw and heat output were a concern at 28nm. Thus,
 like the controllers from competing manufacturers,
 Western Digital opted to build the WD BLACK G2 on a
 newer process node to better control those variables with
 TSMC’s 16nm FinFET technology.

27 Sean Webster, *WD Black SN850 M.2 NVMe SSD Review: Top-Tier Storage for*
 28 *Gamers and Pros (Updated)*, Tom’s Hardware (Apr. 1, 2021),

<https://www.tomshardware.com/reviews/wd-black-sn850-m-2-nvme-ssd-review>
[hereinafter “WD Black SN850 Review”].



Front-end processors are usually Cortex-R processors but can sometimes be Cortex-A processors to support more intensive wear-leveling algorithms.

Wear-leveling is the process of systematically erasing and writing all NAND flash locations to ensure all locations wear out at about the same time. It may require moving unchanging data (cold data) already stored so a block can be erased and rewritten with rapidly-changing data (hot data).

Flash Translation Layer (FTL)

The front-end processors are responsible for maintaining the FTL tables that map logical addresses to physical addresses. As part of the FTL, the front-end processors also handle wear-leveling algorithms to determine where the data should be written, which data should move, and which locations require garbage collection.

Read Requests and Write Requests

Read and write requests arrive from the host over the PCIe/NVMe interface. The requests arrive in the form of descriptors that describe the parameters of a transfer. Write requests also carry the data to be written. These descriptors are written to either the DDR memory or a system RAM using a DMA operation from the host. For write requests, the user data is transferred to the controller DDR using a separate DMA operation.

Arm Ltd., *Arm Storage Solution for SSD Controllers* at 4 (Sept. 2020),
<https://www.arm.com/-/media/global/solutions/storage/arm-storage-solution-for-ssd-solutions-brief.pdf?rev=3530e7536aae437aa2d7acf1704fe25b&revision=3530e753-6aae-437a-a2d7-acf1704fe25b> [hereinafter “Arm Storage Solution for SSD Controllers”].

1 A front-end processor is notified about the arrival of this descriptor. It then parses the
2 descriptor to modify some of the parameters. In particular, the Logical Block Address (LBA)
3 provided by the host must be modified to the physical address in the NAND where the
4 read data is stored. With the correct physical address, the descriptor can be dispatched
to the appropriate flash channel using a DMA.

5 For read requests, the flash channel issues a read operation to the appropriate NAND
6 die. When the data is available, it is moved from the NAND die buffer to the flash channel
7 and then to the LDPC engines, as space is available. The LDPC engines perform ECC
8 correction and data recovery from the media. If necessary, erasure coding operations
9 are performed to recover data lost due to a block or page failure. Encrypted data is
decrypted and stored in controller DDR. Finally, the user data is moved to host memory
using a DMA operation to write into the DDR of the host, and then the host is notified
that the data transfer completed.

10 For write requests, the user data in DDR is sent to the SSD data path of encryption,
11 erasure coding, and LDPC encoding. When the encoded user data reaches the flash channel,
12 the flash channel issues an operation to write the data to the NAND buffers. When all
13 the data is in the NAND buffer, a program operation is issued to program the NAND. A
completion response is generated by the flash channel that is sent back to the host.

14 Arm Storage Solution for SSD Controllers at 5.

15 Defendants' nonvolatile memory controllers include RAID scheme support, which
16 inherently includes stripe operations.

17 The Sentinel ECC&DSP error correction is based on state-of-the-art Low Density Parity Check (LDPC) coding and
18 provides a full suite of NAND DSP (Digital Signal Processing) services, including data randomization or shaping,
NAND health metering via Bit Error Rate (BER) estimation, ECC-based read thresholds calibration, and NAND defect
protection and recovery via XOR based RAID scheme support.

19 Idan Alrod et al., *The Application of ECC/DSP to Flash Memory* (Mar. 2021),
20 Western Digital, [https://documents.westerndigital.com/content/dam/doc-](https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-the-application-of-ecc-dsp-to-flash-memory.pdf)
21 [library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-the-](https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-the-application-of-ecc-dsp-to-flash-memory.pdf)
22 [application-of-ecc-dsp-to-flash-memory.pdf](https://documents.westerndigital.com/content/dam/doc-library/en_us/assets/public/western-digital/collateral/white-paper/white-paper-the-application-of-ecc-dsp-to-flash-memory.pdf) [hereinafter "ECC/DSP White Paper"]
23 at 5.
24
25
26
27
28

Joint LDPC and RAID Decoding for Enterprise SSD

Certain flash applications, such as enterprise SSD, require an exceptionally high level of data reliability. In these applications, the probability of losing data – no matter what caused it – must be exceptionally low. More specifically, the system must be able to cope with flash failure modes that do not only include random errors, but failures of entire pages. These might include word line failures of various sorts, block failures, or even die-level faults.

One existing strategy is to use RAID parity. This method has many variants depending on reliability requirements (how many failed sectors can the system recover from), locality of recovery (how many read and transfer operations required for a single recovery), and other system tradeoffs. The simplest of such schemes is the plain-vanilla variant, where recovery from a single sector failure is possible. This requires one parity sector, which holds the RAID parity of all other sectors. Upon failure of one of the sectors, reconstruction is possible by performing RAID recovery on all the non-failing sectors. Of course, this simple scheme is equally effective if the failing sector is due to a large number of random errors, which is not correctable by the ECC. The following two are simple observations on this scheme:

[ECC/DSP White Paper](#) at 11.

Appendix – Case Study [FMS 2016, Patent Application US20170255518A1]

Let's assume a standard RAID stripe of length 32. This means that 31 sectors are protected by an additional parity sector. The over-provisioning used by this RAID scheme is around 3%. Next, let's assume an LDPC-based ECC solution that has approximately 10% over-provisioning.

If the LDPC and RAID layers were to be combined, one could observe that the result is a code with extra 3% overprovisioning and a code word size that is x32 larger than the original. A Tanner graph representing a unified LDPC-RAID code is shown in Figure 13 below. It shows a Tanner graph of a combined LDPC-RAID scheme. The smaller graphs $G_0, G_1, \dots, G_{30}$ represent the information sectors and G_{31} is the parity sector.

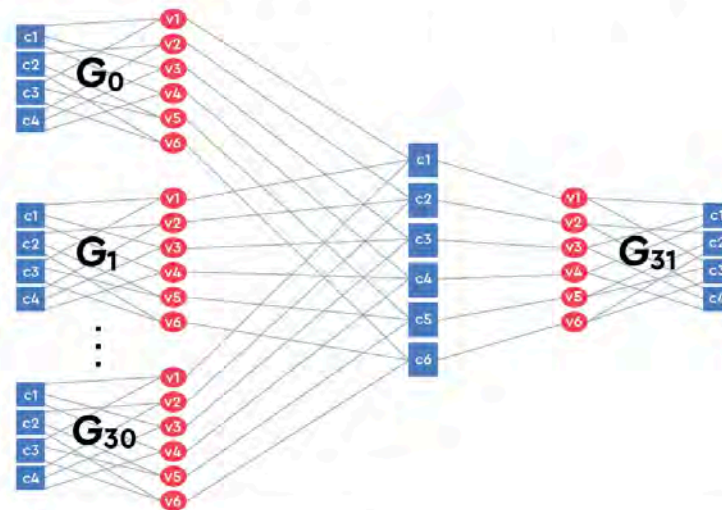


Figure 13: Tanner graph of a combined LDPC-RAID scheme

[ECC/DSP White Paper](#) at 12.

What are RAID 50 and 60? I see you have a product that supports them. —

RAID 50 and 60 are very similar to RAID 10, as they are all “nested” RAIDs. The first number in the type — 5 and 6, respectively — represents what subset they are built with, either RAID 5 arrays or RAID 6 arrays. The second number represents the RAID type the first one is “nested” into; in this case, it’s RAID 0.

Let’s dive a bit deeper.

So, with RAID 50:

- Two RAID 5 subsets stripe across each other in RAID 0.
- With eight drives, four drives act as RAID 5 with their own parity. Another four do the same with data split between two sets.
- Any one of the four drives in each set could fail. That’s one to two drives — two if they’re not within the same subset.

So, with RAID 60:

- Two RAID 6 subsets stripe across each other in RAID 0.
- With eight drives, any one of the four drives in each set could fail. That’s two to four drives — four if two are from one subset and two are from the other subset.

RAID 50 vs. RAID 60:

- RAID 50 will have faster performance than RAID 60.
- RAID 60, like RAID 6, has parity for all data written twice. That’s why you “lose” two disks of capacity per RAID 6 subset.
- With RAID 50, it’s one disk per subset.

Western Digital, *What is RAID Storage?*,

<https://www.westerndigital.com/solutions/raid> [hereinafter “RAID Storage Guide”].

92. The Accused Products include a plurality of data update commands, which write data to a nonvolatile controller to update the contents of nonvolatile memory, and a parity write command, as shown below:

6.15 Write command

The Write command writes data and metadata, if applicable, to the I/O controller for the logical blocks indicated.

[NVMe Express Specification](#) v1.4 at 268.

The Sentinel ECC&DSP error correction is based on state-of-the-art Low Density Parity Check (LDPC) coding and provides a full suite of NAND DSP (Digital Signal Processing) services, including data randomization or shaping, NAND health metering via Bit Error Rate (BER) estimation, ECC-based read thresholds calibration, and NAND defect protection and recovery via XOR based RAID scheme support.

[ECC/DSP White Paper](#) at 5.

Joint LDPC and RAID Decoding for Enterprise SSD

Certain flash applications, such as enterprise SSD, require an exceptionally high level of data reliability. In these applications, the probability of losing data – no matter what caused it – must be exceptionally low. More specifically, the system must be able to cope with flash failure modes that do not only include random errors, but failures of entire pages. These might include word line failures of various sorts, block failures, or even die-level faults.

One existing strategy is to use RAID parity. This method has many variants depending on reliability requirements (how many failed sectors can the system recover from), locality of recovery (how many read and transfer operations required for a single recovery), and other system tradeoffs. The simplest of such schemes is the plain-vanilla variant, where recovery from a single sector failure is possible. This requires one parity sector, which holds the RAID parity of all other sectors. Upon failure of one of the sectors, reconstruction is possible by performing RAID recovery on all the non-failing sectors. Of course, this simple scheme is equally effective if the failing sector is due to a large number of random errors, which is not correctable by the ECC. The following two are simple observations on this scheme:

[ECC/DSP White Paper](#) at 11.

Appendix – Case Study [FMS 2016, Patent Application US2017025518A1]

Let's assume a standard RAID stripe of length 32. This means that 31 sectors are protected by an additional parity sector. The over-provisioning used by this RAID scheme is around 3%. Next, let's assume an LDPC-based ECC solution that has approximately 10% over-provisioning.

If the LDPC and RAID layers were to be combined, one could observe that the result is a code with extra 3% overprovisioning and a code word size that is x32 larger than the original. A Tanner graph representing a unified LDPC-RAID code is shown in Figure 13 below. It shows a Tanner graph of a combined LDPC-RAID scheme. The smaller graphs $G_0, G_1, \dots, G_{30}$ represent the information sectors and G_{31} is the parity sector.

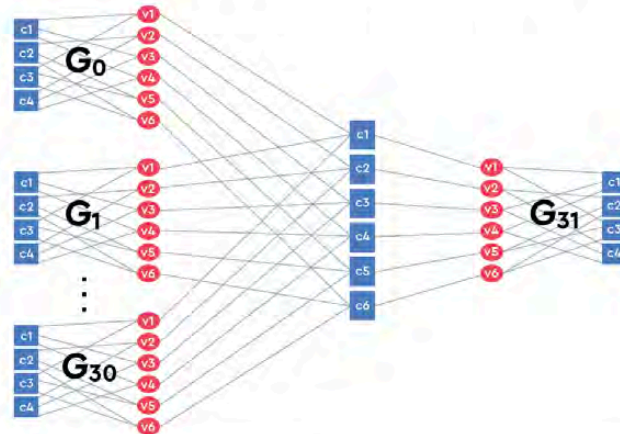


Figure 13: Tanner graph of a combined LDPC-RAID scheme

[ECC/DSP White Paper](#) at 12.

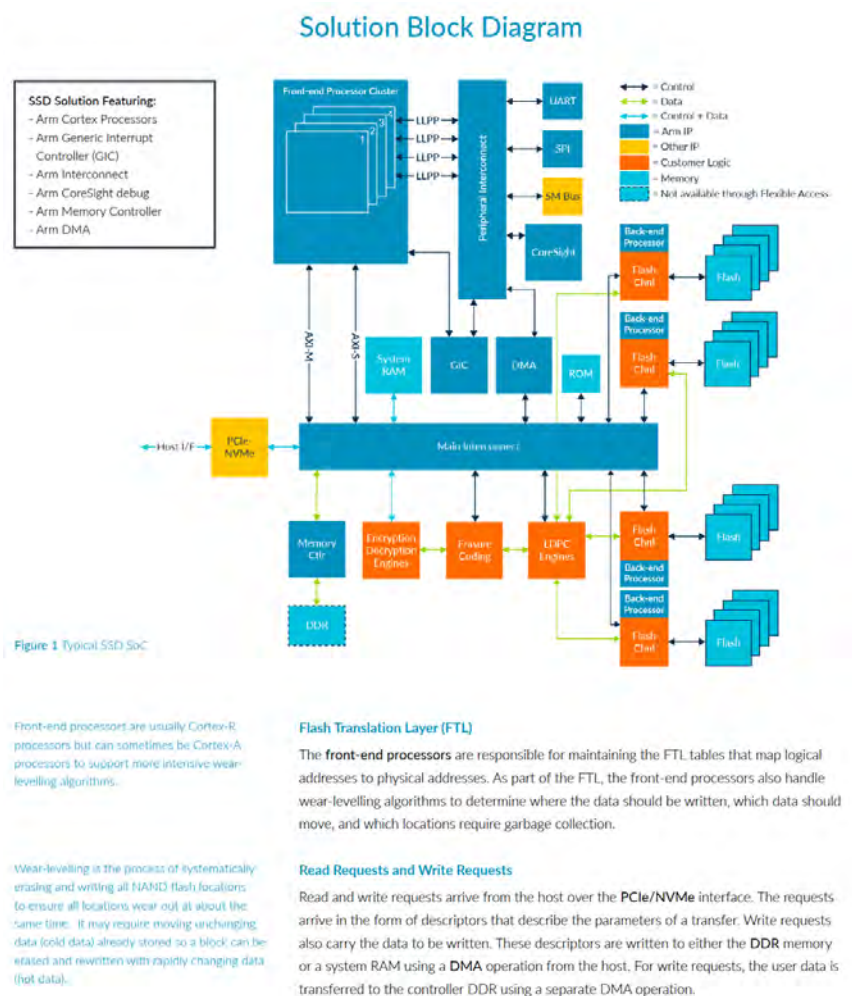
93. For The Accused Products, each command processing unit of the plurality of command processing units receiving a data update command of the plurality of data update commands configured to request a data block of the plurality of data blocks based on the data update command, receive the data block in response

to the request, and write the data block to a nonvolatile memory device, as shown in the quotes and pictures below:

6.15 Write command

The Write command writes data and metadata, if applicable, to the I/O controller for the logical blocks indicated.

[NVMe Express Specification](#) at 268.



[Arm Storage Solution for SSD Controllers](#) at 4.

1 A front-end processor is notified about the arrival of this descriptor. It then parses the
2 descriptor to modify some of the parameters. In particular, the Logical Block Address (LBA)
3 provided by the host must be modified to the physical address in the NAND where the
4 read data is stored. With the correct physical address, the descriptor can be dispatched
5 to the appropriate **flash channel** using a DMA.

6 For read requests, the flash channel issues a read operation to the appropriate NAND
7 die. When the data is available, it is moved from the NAND die buffer to the flash channel
8 and then to the LDPC engines, as space is available. The **LDPC engines** perform ECC
9 correction and data recovery from the media. If necessary, erasure coding operations
10 are performed to recover data lost due to a block or page failure. Encrypted data is
11 decrypted and stored in controller DDR. Finally, the user data is moved to host memory
12 using a DMA operation to write into the DDR of the host, and then the host is notified
13 that the data transfer completed.

14 For write requests, the user data in DDR is sent to the SSD data path of encryption,
15 erasure coding, and LDPC encoding. When the encoded user data reaches the flash channel,
16 the flash channel issues an operation to write the data to the NAND buffers. When all
17 the data is in the NAND buffer, a program operation is issued to program the NAND. A
18 completion response is generated by the flash channel that is sent back to the host.

14 [Arm Storage Solution for SSD Controllers](#) at 5.

15 94. The Accused Products include a parity calculator coupled to the
16 plurality of command processing units. The Accused Products rely on LDPC (Low
17 Density Parity Calculation) Error Correcting Code (ECC) to quickly correct a limited
18 number of random bit errors within an SSD. A RAID scheme is additionally used to
19 recover more slowly when ECC does not allow data to be read reliably (for example,
20 NAND defect protection or a sector or drive failure) by storing redundant data for a
21 stripe. As shown in the text below, a parity calculator is used to create one or more
22 redundant data blocks for RAID storage.

23 The Sentinel ECC&DSP error correction is based on state-of-the-art Low Density Parity Check (LDPC) coding and
24 provides a full suite of NAND DSP (Digital Signal Processing) services, including data randomization or shaping,
25 NAND health metering via Bit Error Rate (BER) estimation, ECC-based read thresholds calibration, and NAND defect
26 protection and recovery via XOR based RAID scheme support.

27 [ECC/DSP White Paper](#) at 5.

Joint LDPC and RAID Decoding for Enterprise SSD

Certain flash applications, such as enterprise SSD, require an exceptionally high level of data reliability. In these applications, the probability of losing data – no matter what caused it – must be exceptionally low. More specifically, the system must be able to cope with flash failure modes that do not only include random errors, but failures of entire pages. These might include word line failures of various sorts, block failures, or even die-level faults.

One existing strategy is to use RAID parity. This method has many variants depending on reliability requirements (how many failed sectors can the system recover from), locality of recovery (how many read and transfer operations required for a single recovery), and other system tradeoffs. The simplest of such schemes is the plain-vanilla variant, where recovery from a single sector failure is possible. This requires one parity sector, which holds the RAID parity of all other sectors. Upon failure of one of the sectors, reconstruction is possible by performing RAID recovery on all the non-failing sectors. Of course, this simple scheme is equally effective if the failing sector is due to a large number of random errors, which is not correctable by the ECC. The following two are simple observations on this scheme:

[ECC/DSP White Paper](#) at 11.

Appendix – Case Study [FMS 2016, Patent Application US2017025518A1]

Let's assume a standard RAID stripe of length 32. This means that 31 sectors are protected by an additional parity sector. The over-provisioning used by this RAID scheme is around 3%. Next, let's assume an LDPC-based ECC solution that has approximately 10% over-provisioning.

If the LDPC and RAID layers were to be combined, one could observe that the result is a code with extra 3% overprovisioning and a code word size that is x32 larger than the original. A Tanner graph representing a unified LDPC-RAID code is shown in Figure 13 below. It shows a Tanner graph of a combined LDPC-RAID scheme. The smaller graphs $G_0, G_1, \dots, G_{30}$ represent the information sectors and G_{31} is the parity sector.

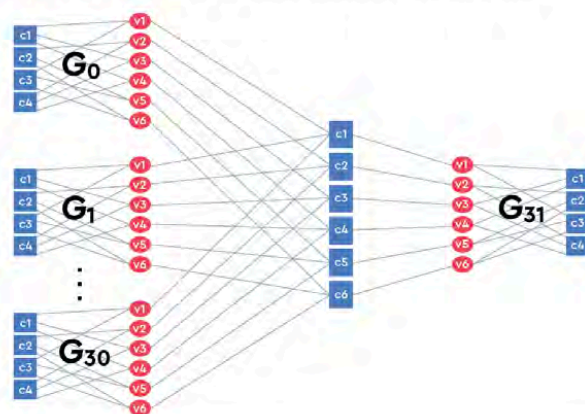


Figure 13: Tanner graph of a combined LDPC-RAID scheme

[ECC/DSP White Paper](#) at 12.

95. As Western Digital (WD) describes in a patent issued from the patent application cited in the ECC/DSP white paper:

Error correction coding (ECC) is often used to correct errors that occur in data read from a memory device. Prior to storage, data may be encoded by an ECC encoder to generate redundant information (e.g., “parity bits”) that may be stored with the data as an ECC codeword. As more parity bits are used, an error correction capacity of the ECC

1 increases and a number of bits required to store the encoded
2 data also increases. Using a sufficient number of parity bits
3 to provide “worst-case” error correction capability for all
4 data stored in a memory device reduces the storage density
of the memory device in order to protect against an amount
of data corruption that is statistically unlikely to occur
before the memory device reaches the end of its useful life.

5 SSD devices may also incorporate a redundant array of
6 independent dies (RAID)- type storage scheme that may
7 use parity bits to enable data recovery in case of memory
8 defects and device failures, which cannot be recovered by
9 the ECC which is aimed at handling random errors (e.g.,
10 due to program disturb, read disturb, charge loss due to data
retention, etc.). ECC may not be able to recover the data in
case of memory defects or complete failure, which may
result in very high error rates that exceed the ECC
capability. Hence, additional RAID-type protection may be
required for protecting against such memory defects.

11 U.S. Patent No. 9,940,194 of Achtenberg et al. at 1:32-55, *ECC Decoding Using*
12 *RAID-Type Parity* available at [https://patentimag-](https://patentimages.storage.googleapis.com/bf/90/8b/dec1bb4115b581/US9940194.pdf)
13 [es.storage.googleapis.com/bf/90/8b/dec1bb4115b581/US9940194.pdf](https://patentimages.storage.googleapis.com/bf/90/8b/dec1bb4115b581/US9940194.pdf) [hereinafter
“Achtenberg”].

14 The two protection levels, ECC for random errors and
15 RAID for memory defects and failures, may require
16 memory overprovisioning for storing the ECC and RAID
parity.

17 [Achtenberg](#) at 2:8-10.

18 In a particular implementation, the stripe correction
19 scheme corresponds to a redundant array of independent
20 disks (RAID)-type exclusive-OR (XOR) scheme, and the
first correction scheme corresponds to a low density parity
check (LDPC) scheme.

21 [Achtenberg](#) at 14:47-51.

22 See also [WD Black 3D Review](#).



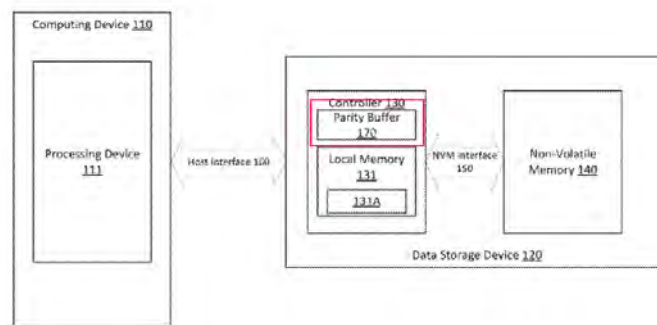
[WD Black 3D Review.](#)

96. Furthermore, other Defendants' patent filings indicate that its RAID parity calculations are performed by a parity calculator that performs a partial parity calculation on blocks received for writing to a stripe. The following image is from U.S. Patent No. 11,106,534:

(57) **ABSTRACT**

An apparatus is disclosed having a parity buffer having a plurality of parity pages and one or more dies, each die having a plurality of layers in which data may be written. The apparatus also includes a storage controller configured to write a stripe of data across two or more layers of the one or more dies, the stripe having one or more data values and a parity value. When a first data value of the stripe is written, it is stored as a current value in a parity page of the parity buffer, the parity page corresponding to the stripe. For each subsequent data value that is written, an XOR operation is performed with the subsequent data value and the current value of the corresponding parity page and the result of the XOR operation is stored as the current value of the corresponding parity page.

U.S. Patent No. 11,106,534, Sun et al., *3-Dimensional Nand Flash Layer Variation Aware SSD RAID*,
<https://patentimages.storage.googleapis.com/0a/c7/53/8923ad3f4269e8/US11106534.pdf> [hereinafter “Sun”].



Sun at Fig. 1, annotation added.

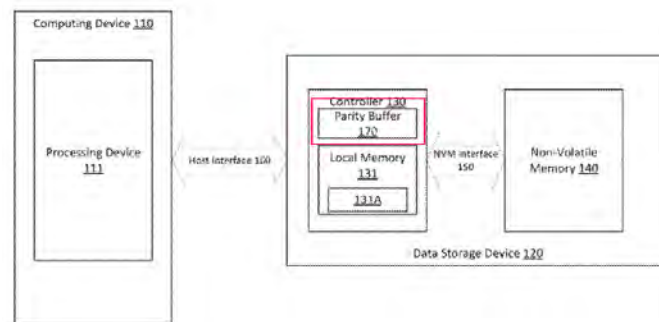
97. The Accused Products include a context memory including a page frame. For example, Defendants’ patent filings, such as Sun, describes a memory system for storing its partial parity RAID data calculation and associated metadata. This system includes features for indicating updated blocks within a data stripe and for converting logical pages to their physical counterparts.

(57)

ABSTRACT

An apparatus is disclosed having a parity buffer having a plurality of parity pages and one or more dies, each die having a plurality of layers in which data may be written. The apparatus also includes a storage controller configured to write a stripe of data across two or more layers of the one or more dies, the stripe having one or more data values and a parity value. When a first data value of the stripe is written, it is stored as a current value in a parity page of the parity buffer, the parity page corresponding to the stripe. For each subsequent data value that is written, an XOR operation is performed with the subsequent data value and the current value of the corresponding parity page and the result of the XOR operation is stored as the current value of the corresponding parity page.

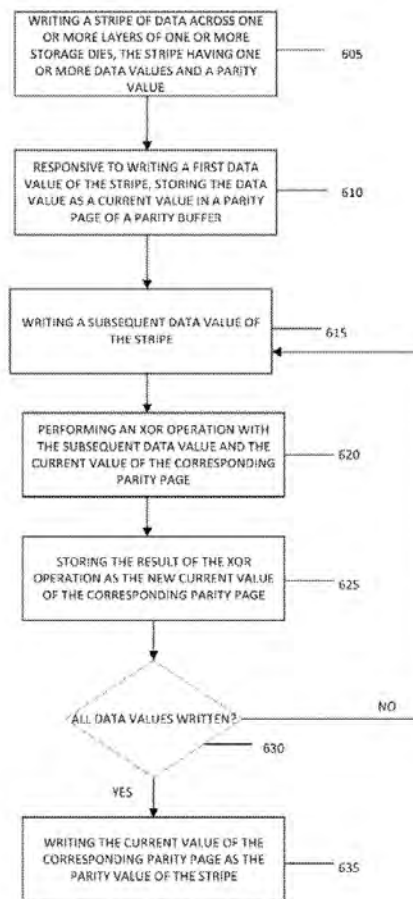
[Sun](#) at Abstract.



[Sun](#) at Fig. 1, annotation added.

The logical interface may present to the computing device memory a set of logical addresses (e.g., sequential/contiguous addresses) where data may be stored. Internally, the controller 130 may map logical addresses to various physical memory addresses in the non volatile memory arrays and or other memory module(s).

[Sun](#) at 5:21-26.



[Sun](#) Fig. 6.

At block 630, the controller may determine whether all the data values are written. If there are still data values to be written, the controller returns to block 615. If all data values are written, then at block 635 the controller writes the current value of the corresponding parity page to the parity value of the stripe.

[Sun](#) at 9:52-58.

98. The Accused Products include a parity calculator configured to receive the plurality of data blocks as a sequence of data blocks. For example, U.S. Patent No. 9,940,194, assigned to WD and cited in WD's White Paper, The Application of ECC/DSP to Flash Memory, describes writing a sequence of data blocks for RAID parity calculation, as shown in the quote and image below:

Achtenberg at 8:31-40.



COMPLAINT FOR PATENT INFRINGEMENT

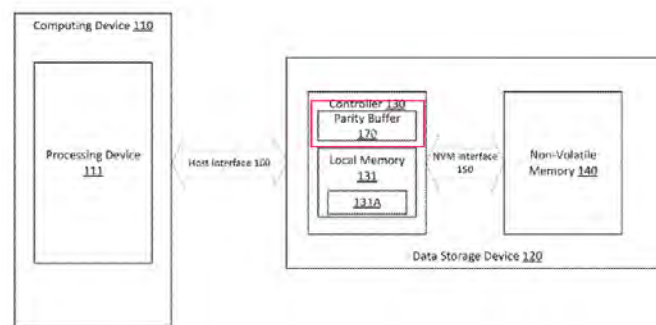
99. Furthermore, Sun describes a buffer for storing parity information, e.g., parity cache or “partial parity Cache (PPC)”, which stores a parity block for a stripe that is updated for each data block written for the stripe.

(57)

ABSTRACT

An apparatus is disclosed having a parity buffer having a plurality of parity pages and one or more dies, each die having a plurality of layers in which data may be written. The apparatus also includes a storage controller configured to write a stripe of data across two or more layers of the one or more dies, the stripe having one or more data values and a parity value. When a first data value of the stripe is written, it is stored as a current value in a parity page of the parity buffer, the parity page corresponding to the stripe. For each subsequent data value that is written, an XOR operation is performed with the subsequent data value and the current value of the corresponding parity page and the result of the XOR operation is stored as the current value of the corresponding parity page.

[Sun](#) at Abstract.



[Sun](#) at Fig. 1, annotation added; *see also* Fig. 6.

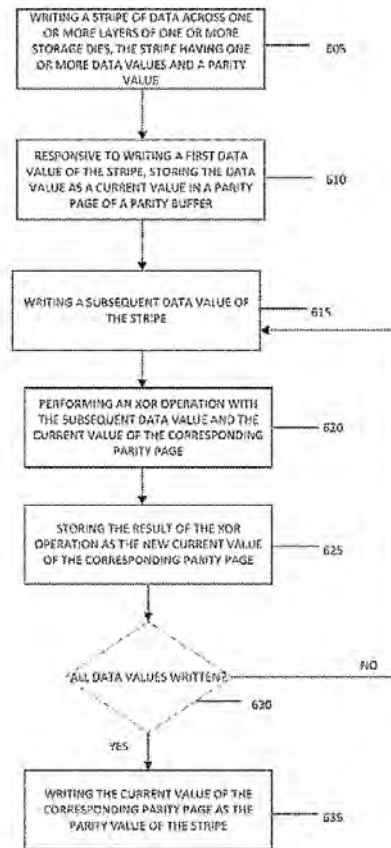
100. The Accused Products generate a parity block storing the first data block of the sequence of data blocks into the page frame and update the parity buffer with the first block written to the stripe. For example, in Sun, WD describes generating and updating the parity block.

(57)

ABSTRACT

An apparatus is disclosed having a parity buffer having a plurality of parity pages and one or more dies, each die having a plurality of layers in which data may be written. The apparatus also includes a storage controller configured to write a stripe of data across two or more layers of the one or more dies, the stripe having one or more data values and a parity value. When a first data value of the stripe is written, it is stored as a current value in a parity page of the parity buffer, the parity page corresponding to the stripe. For each subsequent data value that is written, an XOR operation is performed with the subsequent data value and the current value of the corresponding parity page and the result of the XOR operation is stored as the current value of the corresponding parity page.

[Sun](#) at Abstract.

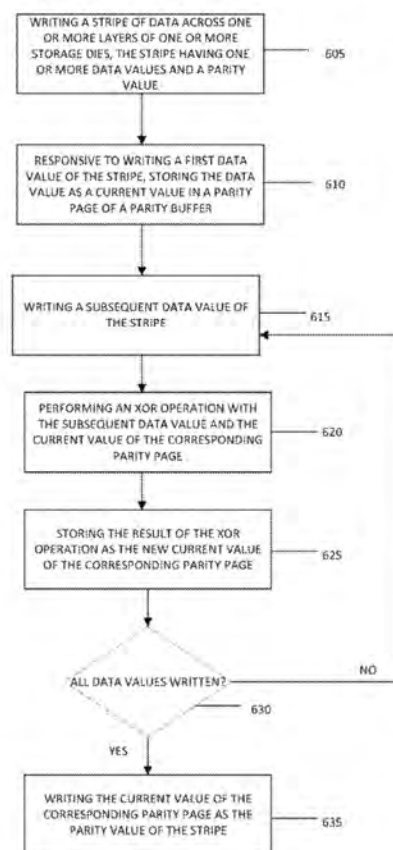


[Sun](#) at Fig. 6.

At block 610, responsive to writing a first data value of the stripe, the controller may store the first data value as a current value in a parity page of a parity buffer. The parity page may correspond to the stripe being written. At block 615, the controller may write a subsequent data value. At block 620, the controller may perform an XOR operation with the subsequent data value and the current value of the corresponding parity page. At block 625, the controller may store the result of the XOR operation as the new current value of the corresponding parity page.

[Sun](#) at 9:43-52.

101. In The Accused Products, the command processing unit that receives the parity write command is configured to write the parity block to a nonvolatile memory based on the parity write command. For example, in Sun, WD describes writing the parity to nonvolatile memory.



[Sun](#) at Fig. 6.

At block 630, the controller may determine whether all the data values are written. If there are still data values to be

1 written, the controller returns to block 615. If all data
2 values are written, then at block 635 the controller writes
3 the current value of the corresponding parity page to the
4 parity value of the stripe.

[Sun](#) at 9:52-58.

5 102. For example, Defendants provide SSD products configured with the
6 hardware and software that satisfy the limitations of at least claim 1. Defendants
7 further directly infringe the '346 Patent when its SSD products with NVMe are
8 installed and operated by its employees in a computer system, such as for gaming,
9 personal computing, or data centers. Direct infringement further occurs when
10 Defendants' employees use and test the hardware and software.

11 103. On January 23, 2024, Plaintiff sent a notice letter to Western Digital,
12 notifying them that they were infringing the Asserted Patents. Western Digital's
13 infringement of the '346 Patent has been willful and intentional under the standard
14 announced in *Halo Elecs., Inc. v. Pulse Elecs., Inc.*, 579 U.S. 93 (2016). Western
15 Digital did not reply to that letter.

16 104. Western Digital has willfully infringed the '346 Patent by refusing to
17 take a license and continuing to make, use, test, sell, license, and/or offer for
18 sale/license the '346 Patent Accused Products. Instead of taking a license, Western
19 Digital has opted to make the business decision to "efficiently infringe" the '346
20 Patent. In doing so, Western Digital willfully infringes the '346 Patent.

21 105. Defendants also have infringed, and continue to infringe the claims of
22 the '346 Patent by actively inducing others to use the Accused Products. Defendants'
23 users, customers, agents or other third parties who use the Accused Products in
24 accordance with Defendants' instructions infringe the claims of the '346 Patent, in
25 violation of 35 U.S.C. § 271(a). Defendants induce its customers to use its SSD
26 products for the benefits of higher performance, reduced size and power, and
27 increased reliability compared to other SSD products. Defendants are thereby liable
28 for infringement of the '346 Patent under 35 U.S.C. § 271(b).

106. Defendants' users, customers, agents or other third parties who use the Accused Products in accordance with Defendants' instructions infringe the claims of the '346 Patent, in violation of 35 U.S.C. § 271(b). Defendants intentionally instruct its customers to infringe through support information, demonstrations, brochures, videos, and user guides, such as those located at:

<https://www.westerndigital.com/support;>

<https://support.wdc.com/contact.aspx?lang=en;>

<https://www.westerndigital.com/support/category-selection;>

https://www.youtube.com/channel/UC_M0BIntDVSblWg6ggUa7UQ;

<https://www.youtube.com/watch?v=L0zZtwRFj0E;>

<https://www.youtube.com/westerndigital>; and

<https://www.youtube.com/c/westerndigitalcorporation>.

107. Defendants are liable as contributory infringers of the '346 Patent under 35 U.S.C. § 271(c) by having offered to sell, sold and imported and continuing to offer to sell, selling, and importing into the United States its SSD products, to be especially made or adapted for use in an infringement of the '346 Patent. Defendants' SSD products are key components in gaming consoles and gaming PCs, computers, everyday PCs, Network Attached Storage (NAS) devices, servers and data centers. These SSD products are material components for use in practicing the '346 Patent and are specifically made and are not a staple article of commerce suitable for substantial noninfringing use. Defendants supplied these components with knowledge of the '346 Patent and with knowledge that these components constitute material parts of the claimed inventions of the '346 Patent.

108. As a result of Defendants' infringement of the '346 Patent, Plaintiff has suffered monetary damages and is entitled to no less than a reasonable royalty for Defendants' use of the claimed inventions of the '346 Patent, together with interest and costs as determined by the Court. Plaintiff will continue to suffer damages in the future.

1 109. Defendants are on notice of their infringement by no later than the filing
2 and service of this Complaint. By the time of trial, Defendants will have known and
3 intended (since receiving such notice) that its continued actions would actively
4 induce to the infringement of the '346 Patent.

5 110. Defendants' acts of direct and indirect infringement have caused and
6 continue to cause damage to Plaintiff. Plaintiff is entitled to damages in accordance
7 with 35 U.S.C. §§ 271 and 281 sustained as a result of Defendants' wrongful acts in
8 an amount to be proven at trial.

9 **PRAYER FOR RELIEF**

10 WHEREFORE, Plaintiff requests the following relief from this Court:

11 A. A judgment that each defendant is liable for infringement of one or more
12 claims of the '968 Patent, the '346 Patent, and the '085 Patent;

13 B. Compensatory damages in an amount according to proof, and in any
14 event no less than a reasonable royalty, including all pre-judgment and post-judgment
15 interest at the maximum rate allowed by law;

16 C. A judgment granting Plaintiff such further relief as the Court may deem
17 just and proper; and

18 D. That the Court declare this an exceptional case and award Plaintiff its
19 attorneys' fees, as provided by 35 U.S.C. § 285 and that Plaintiff be awarded
20 enhanced damages up to treble damages for willful infringement as provided by 35
21 U.S.C. § 284.

22 **DEMAND FOR JURY TRIAL**

23 Pursuant to Rule 38(b) of the Federal Rules of Civil Procedure, Plaintiff
24 demands a trial by jury for all issues so triable.

1 Dated: April 9, 2024

By: /s/ Robert F. Kramer

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*Admitted Pro Hac Vice
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Attorneys for Defendants
12 *WESTERN DIGITAL CORPORATION and*
13 *WESTERN DIGITAL TECHNOLOGIES, INC.*

14 **UNITED STATES DISTRICT COURT**
15 **CENTRAL DISTRICT OF CALIFORNIA**
16

17 POLARIS POWERLED
18 TECHNOLOGIES, LLC,

19 Plaintiff,

20 v.

21 WESTERN DIGITAL
CORPORATION, WESTERN
22 DIGITAL TECHNOLOGIES, INC.,
NEWEGG, INC., ZONES, LLC, AND
23 PRIVATE LABEL PC, LLC,

24 Defendants,
25
26
27
28

CASE NO. 2:24-cv-02864-ODW-MAR

**NOTICE OF SOTERA
STIPULATION OF WESTERN
DIGITAL**

Hon. Otis D. Wright

NOTICE OF SOTERA STIPULATION OF WESTERN DIGITAL

On January 23, 24, and 29, 2025, Western Digital Technologies Inc. (“Western Digital”) and Sandisk Technologies Inc. (“Sandisk”) together as co-petitioners filed petitions for *Inter Partes* Review (“IPR”) of the patents asserted in this lawsuit – U.S. Patent Nos. 9,183,085, 8,601,346, and 8,554,968 – with the Patent Trial and Appeal Board of the United States Patent and Trademark Office (the “PTAB”). Western Digital and Sandisk (“Petitioners”) were listed as real parties-in-interest in each IPR proceeding. The table below indicates the IPR number, challenged patent number, and challenged claims of the respective petitions filed before the PTAB.

IPR No.	Asserted Patent	Challenged Claims
IPR2025-00515	9,183,085	1-2, 4-7, 14-18, 22-25, and 29-33
IPR2025-00516	8,601,346	1-11 and 13-18
IPR2025-00517	8,554,968	1-18

The claims challenged in these IPR petitions include all the claims of the above respective asserted patents that Plaintiff Polaris PowerLED Technologies, LLC (“Plaintiff”) has asserted against Defendant Western Digital in this litigation.

Defendant Western Digital hereby notifies the Court and Plaintiff that Defendant Western Digital is submitting the following “*Sotera* stipulations” in connection with the petitions in IPR2025-00515, IPR2025-00516, and IPR2025-00517. *See Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020- 01019, Paper 12 at 18–19 (PTAB Dec. 1, 2020) (“*Sotera*”). Defendant Western Digital Corp., who is not a named petitioner, also agrees to be bound by the following stipulations. Further, co-petitioner Sandisk agrees that, if added as a party to this litigation, it will also abide by the terms of the following stipulations.

Defendant Western Digital hereby stipulates, consistent with the stipulation made by the Petitioner in *Sotera* that, if the PTAB institutes an IPR in response to

1 Defendant's petition against Plaintiff's U.S. Patent No. 9,183,085 (IPR2025-
2 00515), Defendant will not pursue in this litigation against the claims challenged
3 in IPR2025-00515, (i) the specific grounds raised in IPR2025-00515, or (ii) any
4 other grounds that could have reasonably been raised before the PTAB in that
5 instituted proceeding (*i.e.*, any ground that could have reasonably been raised under
6 §§ 102 or 103 on the basis of prior art patents or printed publications).

7 Defendant Western Digital hereby stipulates, consistent with the stipulation
8 made by the Petitioner in *Sotera* that, if the PTAB institutes an IPR in response to
9 Defendant's petition against Plaintiff's U.S. Patent No. 8,601,346 (IPR2025-
10 00516), Defendant will not pursue in this litigation against the claims challenged
11 in IPR2025-00516, (i) the specific grounds raised in IPR2025-00516, or (ii) any
12 other grounds that could have reasonably been raised before the PTAB in that
13 instituted proceeding (*i.e.*, any ground that could have reasonably been raised under
14 §§ 102 or 103 on the basis of prior art patents or printed publications).

15 Defendant Western Digital hereby stipulates, consistent with the stipulation
16 made by the Petitioner in *Sotera* that, if the PTAB institutes an IPR in response to
17 Defendant's petition against Plaintiff's U.S. Patent No. 8,554,968 (IPR2025-
18 00517), Defendant will not pursue in this litigation against the claims challenged
19 in IPR2025-00517, (i) the specific grounds raised in IPR2025-00517, or (ii) any
20 other grounds that could have reasonably been raised before the PTAB in that
21 instituted proceeding (*i.e.*, any ground that could have reasonably been raised under
22 §§ 102 or 103 on the basis of prior art patents or printed publications).

23 However, if the PTAB declines institution as to any ground in any of these IPR
24 proceedings, or if institution is denied through Rehearing or Director Review,
25 Petitioners reserve the right to pursue any non-instituted ground in this action.

26 Defendant's *Sotera* stipulations above are not intended and should not be
27 construed to limit Defendant's ability to assert invalidity of any claims of the patents-
28 at-issue in this lawsuit based on any other ground.

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Date: April 28, 2025

HAYNES AND BOONE, LLP

/s/David B. Clark
Kenneth G. Parker
David B. Clark
Stephanie N. Sivinski
Caroline W. Fox
Marron E. Frith
WESTERN DIGITAL
CORPORATION and WESTERN
DIGITAL TECHNOLOGIES, INC.

CERTIFICATE OF SERVICE

I hereby certify pursuant to the Federal Rules of Civil Procedure and LR 5-3 and 5-4 that the above document was served upon the attorney(s) of record for each party through the ECF system.

/s/David B. Clark

David B. Clark

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8 **United States District Court**
9 **Central District of California**
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11 POLARIS POWERLED
12 TECHNOLOGIES, LLC,

13 Plaintiffs,

14 v.
15 WESTERN DIGITAL CORPORATION
16 et al.,

17 Defendants.

Case № 2:24-cv-02864-ODW (MARx)

ORDER GRANTING
DEFENDANTS' MOTION TO STAY
[58]

18 **I. INTRODUCTION**

19 Plaintiff Polaris PowerLED Technologies, LLC (“Polaris”) brings this
20 patent-infringement suit against Defendants Western Digital Corporation and Western
21 Digital Technologies, Inc. (collectively, “Western Digital”). (First Am. Compl.
22 (“FAC”), ECF No. 40.) Western Digital moves to stay this action pending *inter partes*
23 review of three patents Polaris alleges Western Digital infringed: U.S. Patent
24 Nos. 8,554,968 (the “’968 Patent”), 9,183,085 (the “’085 Patent”), and 8,601,346 (the
25 “’346 Patent”). (Mot. Stay. (“Mot.”), ECF No. 58.) For the reasons below, the Court
26 **GRANTS** the Motion.¹
27

28 ¹ Having carefully considered the papers filed in connection with the Motion, the Court deemed the
matter appropriate for decision without oral argument. Fed. R. Civ. P. 78; C.D. Cal. L.R. 7-15.

II. BACKGROUND

Polaris is a California limited liability company that “owns the entire right, title, and interest” in the ’968 Patent, ’085 Patent, and ’346 Patent. (FAC ¶¶ 7, 34–36.) The three patents-in-suit relate to memory controllers, flash memory, and data-stripe operation systems. (*Id.* ¶¶ 37, 42, 56.)

On April 9, 2024, Polaris initiated this patent infringement action against Western Digital; Newegg, Inc., Zones, LLC, and Private Label PC, LLC (collectively, “Customer Defendants”); and Avnet Inc. (Compl., ECF No. 1.) On April 19, 2024, pursuant to Polaris’s notice of voluntary dismissal, the Court dismissed Avnet, Inc. without prejudice. (Min. Order, ECF No. 24.)

On June 21, 2024, Polaris filed the operative First Amended Complaint. (FAC.) Polaris asserts three patent infringement claims against Western Digital and Customer Defendants for “making, using, offering for sale, selling . . . and/or importing into the United States” solid-state drive (“SSD”) products that infringed the three patents-in-suit. (*Id.* ¶¶ 68, 89, 111.) On Polaris’s motion, the Court subsequently severed the claims against Customer Defendants and dismissed Customer Defendants from this action without prejudice. (Order Mot. Sever, ECF No. 50.) Accordingly, Western Digital Corporation and Western Digital Technologies, Inc. are the only remaining defendants in this action.

Between January 23 and January 29, 2025, Western Digital filed three petitions for *inter partes* review (the “IPRs”) with the Patent Trial and Appeal Board (“PTAB”), one for each of the three patents-in-suit, “challenging all claims that Polaris currently asserts in this litigation.” (Decl. David B. Clark ISO Mot. (“Clark Decl.”) ¶¶ 2–4, ECF No. 58-1; *see id.* Exs. A–C (“IPR Submission Receipts”), ECF Nos. 58-2 to 58-4.) In the meantime, on January 27, 2025, the Court issued a Scheduling and Case Management Order (“Scheduling Order”), setting the trial on June 16, 2026, and fact discovery deadline on February 18, 2026. (Scheduling

1 Order 25, ECF No. 54.) On June 3, 2025, the parties filed a Joint Claim Construction
2 and Prehearing Statement. (ECF No. 67.)

3 Western Digital now seeks to stay this action pending resolution of the IPRs.
4 (Mot.) The Motion is fully briefed. (Opp’n, ECF No. 60; Reply, ECF No. 62.)

5 III. LEGAL STANDARD

6 “[T]he power to stay proceedings is incidental to the power inherent in every
7 court to control the disposition of the causes on its docket with economy of time and
8 effort for itself, for counsel, and for litigants.” *Landis v. N. Am. Co.*, 299 U.S. 248,
9 254 (1936); *Dietz v. Bouldin*, 579 U.S. 40, 47 (2016) (“[D]istrict courts have the
10 inherent authority to manage their dockets and courtrooms with a view toward the
11 efficient and expedient resolution of cases.”).

12 Courts in this district consider the following three factors to determine whether
13 to grant a stay pending *inter partes* review proceedings: “(1) whether discovery is
14 complete and whether a trial date has been set; (2) whether a stay will simplify the
15 issues in question and trial of the case; and (3) whether a stay would unduly prejudice
16 or present a clear tactical disadvantage to the nonmoving party.” *Universal Elecs.,*
17 *Inc. v. Universal Remote Control, Inc.*, 943 F. Supp. 2d 1028, 1030–31 (C.D. Cal.
18 2013). The inquiry, however, “is not limited to these three factors” but based on “the
19 totality of circumstances.” *Id.* at 1031. “There is a liberal policy in favor of granting
20 motions to stay proceedings pending the outcome of re-examination, especially in
21 cases that are still in the initial stages of litigation and where there has been little or no
22 discovery.” *Id.* (internal quotation marks omitted).

23 IV. DISCUSSION

24 Western Digital argues that the three factors favor a stay. (Mot. 6–13.) As
25 discussed below, the Court agrees.

26 A. Factor One: Stage of Proceedings

27 The first factor looks to the stage of the proceeding and “whether discovery is
28 complete and whether a trial date has been set.” *Universal Elecs.*, 943 F. Supp. 2d

1 at 1031. This analysis “consider[s] the general time line of patent litigation, [and
2 whether] there is more work ahead of the parties and the Court than behind the parties
3 and the Court.” *Semiconductor Energy Lab’y Co., Ltd. v. Chimei Innolux Corp.*,
4 No. 8:12-cv-00021-JLS (JPRx), 2012 WL 7170593, at *2 (C.D. Cal. Dec. 19, 2012).

5 Courts in this district weigh this factor in favor of a stay when, as here, the
6 parties have not engaged in substantial discovery and the Court has not spent time
7 construing the claims. *See e.g., MicroPairing Techs. LLC v. Am. Honda Motor Co.,*
8 *Inc.*, No. 2:21-cv-04034-JVS (KESx), 2022 WL 17219084, at *1 (C.D. Cal. June 24,
9 2022) (weighing this factor in favor of a stay when “months remain for fact discovery,
10 expert discovery has not yet started, . . . no depositions have been conducted[,
11 and] . . . there has been no *Markman* hearing.”); *Realtime Data LLC v. Teradata*
12 *Operations, Inc.*, No. 8:16-cv-02743-AG (FFMx), 2017 WL 3453295, at *2 (C.D. Cal.
13 Feb. 27, 2017) (same); *c.f. Universal Elecs.*, 943 F. Supp. 2d at 1031 (weighing this
14 factor against a stay when plaintiff already served written discovery and the court
15 already held a *Markman* hearing and issued a claim construction ruling).

16 This case is still in early stages of litigation. Trial is set for June 16, 2026, and
17 fact discovery closes on February 18, 2026. (Scheduling Order 25.) On June 3, 2025,
18 the parties filed a Joint Claim Construction Statement, but the Court has not held or
19 scheduled a *Markman* hearing. (*See id.* at 26 (setting August 22, 2025, as deadline for
20 *Markman* hearing).) Polaris asserts that the parties performed substantial work
21 serving document requests, interrogatories, responses, and preparing infringement and
22 invalidity contentions. (Opp’n 15.) While Polaris has undoubtedly expended time
23 and resources, that does not diminish that the case is in its early stages and there is
24 still “more work ahead of the parties and the Court than behind” them. *Chimei*
25 *Innolux*, 2012 WL 7170593, at *2; *see also Wonderland Nursery Goods Co., Ltd. v.*
26 *Baby Trend, Inc.*, No. 5-14-cv-01153-JWH (SPx), 2015 WL 1809309, at *3 (C.D. Cal.
27 Apr. 20, 2015) (granting stay when parties submitted claim construction briefs, but no
28 *Markman* hearing had occurred). Thus, the first factor weighs in favor of a stay.

B. Factor Two: Simplification of Issues and Trial

The second factor considers “whether a stay will simplify the issues in question and trial of the case.” *Universal Elecs.*, 943 F. Supp. 2d at 1032. Western Digital contends that the pending IPRs will likely simplify the issues in this case because they challenge all asserted claims of the three patents-in-suit. (Mot. 3, 7.) Polaris, in turn, argues that a stay would not simplify the issues for several reasons. (Opp’n 7–12.)

First, Polaris contends that the district court “would provide the most simplification of the issues” by resolving the parties’ invalidity contentions and “render the entire IPR proceeding moot.” (Opp’n 10–11.) Polaris asserts that it “would be an enormous waste of the PTAB’s judicial resources and the parties’ financial resources” to stay the case. (*Id.* at 11.) But this argument turns the factor on its head—this factor looks to how a stay pending the IPRs can simplify the issues in the case before this Court, not how this Court can simplify the IPR proceedings before the PTAB.

Second, Polaris contends that any simplification is “purely speculative” because “even if the IPRs are instituted, half of the 30 asserted claims in this case are likely . . . to be litigated in this Court.” (Opp’n 7–8.) However, simplification does not require resolution of all claims. If the PTAB “cancels or narrows a portion of the asserted claims, the scope of this litigation may be significantly reduced.” *Core Optical Techs., LLC v. Fujitsu Network Commc’ns, Inc.*, No. 8:16-cv-00437-AG (JPRx), 2016 WL 7507760, at *2 (C.D. Cal. Sept. 12, 2016); *see Aire Tech., Ltd. v. Garmin Int’l, Inc.*, No. 8:22-cv-01027-JVS (KESx), 2022 WL 19076660, at *3 (C.D. Cal. Aug. 16, 2022) (finding simplification factor weighed in favor of stay “[e]ven if the PTAB institutes review but does not cancel some asserted claims”). Given that this case is still in the early stages of litigation, “the risk of delay attending an unnecessary stay is minimal relative to the risk of unnecessary expenditure of resources should the stay be denied and an IPR subsequently commence.” *Wonderland Nursery Goods*,

1 2015 WL 1809309, at *3. Therefore, there is still a likelihood of simplification even
2 if the PTAB only institutes some of the IPRs.

3 Third, Polaris argues that the IPRs will not affect claim construction in this case
4 because it does not anticipate arguing any of the claim terms in the IPRs. (Opp’n 11–
5 12.) While the IPRs may have little effect on the claim construction in this case, there
6 is still a likelihood that “the outcome of the reexamination could eliminate the need
7 for trial if the claims are cancelled or, if the claims survive, facilitate trial by providing
8 the court with expert opinion of the [Patent and Trial Office] and clarifying the scope
9 of the claims.” *Universal Elecs.*, 943 F. Supp. 2d at 1032. This argument is therefore
10 unpersuasive.

11 Lastly, Polaris argues there is no real simplification of the issues because
12 Western Digital Corporation—which is not a real party in interest to the IPRs and
13 therefore not subject to the estoppel provisions of 35 U.S.C. § 315(e)(2)²—can “raise
14 any invalidity ground in the district court, including the exact same grounds
15 adjudicated in the IPRs.” (Opp’n 9.) “[T]he Court can alleviate [Polaris’s] estoppel
16 concerns by using its inherent power to condition a stay on [Western Digital
17 Corporation’s] agreement to be bound as if it itself had filed the IPR petition.” *Vivint,*
18 *Inc. v. SkyBell Techs., Inc.* No. 2:21-cv-09472-GW (GJSx), 2022 WL 18587113, at *4
19 (C.D. Cal. Nov. 9, 2022). Western Digital Corporation agrees to be bound by
20 estoppel to the same extent as Western Digital Technologies, Inc. (Reply 4–5.) In
21 light of Western Digital Corporation’s expressed agreement to be bound by estoppel,
22 the Court finds it appropriate to condition the stay on Western Digital Corporation’s
23 agreement to be bound by estoppel to the same extent as Western Digital
24 Technologies Inc., which alleviates Polaris’s concerns and simplifies the issues. See
25 e.g., *Aire Tech.*, 2022 WL 19076660, at *3 (finding defendant’s agreement to be
26

27
28 ² Pursuant to 35 U.S.C. § 315(e)(2), a petitioner or real party in interest to an IPR cannot assert in a
civil action that the claim is invalid on any ground that it could have raised or did raise in the IPR.

1 bound by estoppel “will simplify the issues in the event the PTAB grants institution
2 and therefore favors a stay”).

3 Accordingly, on balance, the second factor weighs in favor of a stay.

4 **C. Factor Three: Undue Prejudice and Tactical Concerns³**

5 The final factor considers “whether a stay would unduly prejudice or present a
6 clear tactical disadvantage to the nonmoving party.” *Universal Elecs.*, 943 F. Supp.
7 2d at 1033. Courts consider the following four sub-factors in weighing potential
8 prejudice to the non-moving party: “(1) the timing of the petition for review; (2) the
9 timing of the request for the stay; (3) the status of the review proceedings; and (4) the
10 relationship of the parties.” *Aire Tech.*, 2022 WL 19076660, at *3.

11 The first two sub-factors consider the timing of the IPR and Motion filing. This
12 action was initially filed on January 30, 2024, in the Western District of Texas before
13 Polaris refiled the case in this District. (Opp’n 1 n.1.) Western Digital filed the IPRs
14 between January 23 to January 29, 2025, days before the end of the one-year statutory
15 period to file its IPRs. *See* 35 U.S.C. § 315(b) (requiring IPR petitions to be filed
16 within one year of the date on which the petitioner is served with a complaint alleging
17 patent infringement). On February 3, 2025, four days after it filed the IPRs, Western
18 Digital moved to stay the action. (Mot.) That Western Digital waited until days
19 before the deadline to file the IPRs tips the first sub-factor in favor of undue prejudice.
20 But Western Digital also promptly moved to stay the action, which tips the second
21 sub-factor against undue prejudice. Therefore, on balance, the first two sub-factors
22 are neutral.

23 The third sub-factor looks to the status of the IPR proceedings. Western Digital
24 filed the IPRs in January 2025. (*See* IPR Submission Receipts.) The parties
25 anticipate an institution decision by August 2025, and a final decision by
26

27 ³ Polaris makes several arguments under this factor that were also raised under the first two factors:
28 (1) Western Digital Corporation gains a “tactical advantage” as is it is not bound by estoppel and
(2) the IPRs are not dispositive on the claim construction issues. (Opp’n 16–17.) As the Court
already addressed these arguments, it need not reach them again.

1 August 2026. (Mot. 3; Opp’n 1, 4.) Polaris argues that litigating the IPRs and any
2 appeals could last two to three years and that Western Digital’s late-filed IPRs
3 evidence gamesmanship to delay this litigation. (Opp’n 1, 4, 18.) Polaris does not
4 raise any facts, other than the possibility of delay, to support its assertion that Western
5 Digital engaged in gamesmanship. (*See id.* at 1.) “The mere possibility of delay,
6 inherent in all proceedings, is insufficient to constitute undue prejudice.” *Purecircle*
7 *USA Inc. v. SweeGen, Inc.*, No. 8:18-cv-01679-JVS (JDEx), 2019 WL 3220021, at *3
8 (C.D. Cal. June 3, 2019); *Wonderland Nursery Goods*, 2015 WL 1809309, at *4 (“The
9 general prejudice of having to wait for resolution is not a persuasive reason to deny
10 the motion for stay.”). Polaris also raises a general concern that evidence may be lost
11 during a stay because “[w]itnesses, like the third-party inventors and developers of the
12 accused products, could become unavailable and their memories could fade.”
13 (Opp’n 8.) Polaris’s “[s]peculative assertions that evidence may be lost as a result of a
14 stay pending reexamination are insufficient.” *Aire Tech.*, 2022 WL 19076660, at *4
15 (finding plaintiff’s assertion that “witnesses may become [un]available, their
16 memories may fade, and evidence may be lost” did not pose undue prejudice
17 (alteration in original)). Accordingly, this sub-factor weighs against undue prejudice.

18 The last sub-factor deals with the relationship of the parties. Western Digital
19 contends that Polaris is a non-practicing entity that does not risk losing sales, as
20 Polaris “does not manufacture or sell products that embody any of the asserted
21 claims” of the patents-in-suit. (Mot. 9.) Polaris does not dispute this. (*See generally*
22 Opp’n.) Thus, Polaris’s “status as a non-practicing entity weighs in favor of a stay,”
23 as it will not lose sales or market shares as a result of the stay. *Core Optical*,
24 2016 WL 7507760, at *3. Accordingly, this sub-factor weighs against prejudice.

25 Considering all four subfactors together, the third factor weighs in favor of a
26 stay. Therefore, collectively and under the totality of the circumstances, all three
27 factors weigh in favor of a stay in this case.
28

1 **V. CONCLUSION**

2 For the reasons discussed above, the Court **GRANTS** Defendants' Motion to
3 Stay. (ECF No. 58.) This action is hereby **STAYED** pending final exhaustion of all
4 pending *inter partes* review proceedings, including any appeals, conditioned on
5 Western Digital Corporation's agreement to be bound by 35 U.S.C. § 315(e)(2) as if it
6 were a party to the IPRs.

7 The parties are **ORDERED** to file a joint status report every **ninety (90) days**,
8 beginning ninety days from the date of this Order, informing the Court of the status of
9 the *inter partes* review proceedings. The parties are also **ORDERED** to file a joint
10 statement **by no later than seven (7) days** after the PTAB issues **any** rulings as to the
11 pending *inter partes* review proceedings, stating the parties' respective and/or
12 collective views as to the status of the IPRs and whether any development in those
13 proceedings warrant lifting the stay. All other dates and deadlines in this action are
14 **VACATED** and taken off the calendar.

15
16 **IT IS SO ORDERED.**

17
18 June 23, 2025



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21 **OTIS D. WRIGHT, II**
22 **UNITED STATES DISTRICT JUDGE**
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND WESTERN DIGITAL
TECHNOLOGIES, INC.,
Petitioner

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner.

IPR2025-00516
U.S. Patent No. 8,601,346

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

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IPR2025-00516 Petition
Inter Partes Review of 8,601,346

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IPR2025-00516 Petition
Inter Partes Review of 8,601,346

PETITIONER’S EXHIBIT LIST

Ex.1001	U.S. Patent No. 8,601,346
Ex.1002	Prosecution History of U.S. 8,601,346
Ex.1003	Declaration of Paul Min under 37 C.F.R. § 1.68
Ex.1004	Curriculum Vitae of Paul Min
Ex.1005	U.S. Patent Publication No. 2011/0078496A1 to Jeddeloh (“Jeddeloh”)
Ex.1006	U.S. Patent No. 5,950,225 to Kleiman (“Kleiman”)
Ex.1007	U.S. Patent No. 8,341,332 to Ma et al. (“Ma”)
Ex.1008	U.S. Patent No. 5,787,460 to Yashiro et al. (“Yashiro”)
Ex.1009	U.S. Patent No. 6,161,165 to Solomon et al. (“Solomon”)
Ex.1010	Reserved
Ex.1011	The Authoritative Dictionary of IEEE Standards Terms: Seventh Edition; (“IEEE”)
Ex.1012	U.S. Patent No. 8,074,149 to Stolowitz (“Stolowitz”)
Ex.1013	U.S. Patent No. 8,819,699 to Cota-Robles (“Cota-Robles”)
Ex.1014	U.S. Patent No. 6,092,215 to Hodges et al. (“Hodges”)
Ex.1015	Complaint, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)
Ex.1016	District Court Trial Statistics
Ex.1017	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, June 22, 2022

I. INTRODUCTION

The prior art presented in this Petition describes the same parity calculation techniques that are claimed in U.S. Patent No. 8,601,346 (“the ’346 patent”). The ’346 patent relates to a “method for generating parity data” that includes “distributing commands for performing a data stripe operation among a number of command processing units.” Ex.1001, 2:65-3:1. The ’346 patent was allowed after amending the claims to cover the concept in which “the parity calculator generates the parity block **on the fly** as the command processing units and the parity calculator are receiving the data blocks for the data stripe operation.” Ex.1001, 4:7-11; Ex.1002, 146.

However, it was already known to calculate parity data in this manner. The Jeddeloh reference describes using “RAID XOR circuitry [to] calculate parity data” and distribute commands among a plurality of “channel memory control circuit[s] 338-1, ...338-N.” Ex.1005, [0027], [0038]. And the Kleiman reference (entitled “Fly-by XOR for Generating Parity for Data Gleaned from a Bus) shows that it was known to use RAID XOR circuitry “for performing **fly-by** XOR.” Ex.1006, 3:38. The Ma reference describes further details recited in the claims.

As shown in this Petition, and supported by the declaration of Dr. Paul Min, Jeddeloh, Kleiman, and Ma render obvious claims 1-11 and 13-18 (hereinafter, the “Challenged Claims”) of the ’346 patent.

Accordingly, pursuant to 35 U.S.C. §§ 311, 314(a), and 37 C.F.R. § 42.100, Petitioner respectfully requests that the Board review and cancel as unpatentable under (pre-AIA) 35 U.S.C. § 103(a) the Challenged Claims of the '346 patent.

II. GROUNDS FOR STANDING

Petitioner certifies that the '346 patent is eligible for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims. 37 C.F.R. § 42.104(a).

III. NOTE

Petitioner cites to exhibits' original page numbers. Emphasis in quoted material has been added.

IV. BACKGROUND

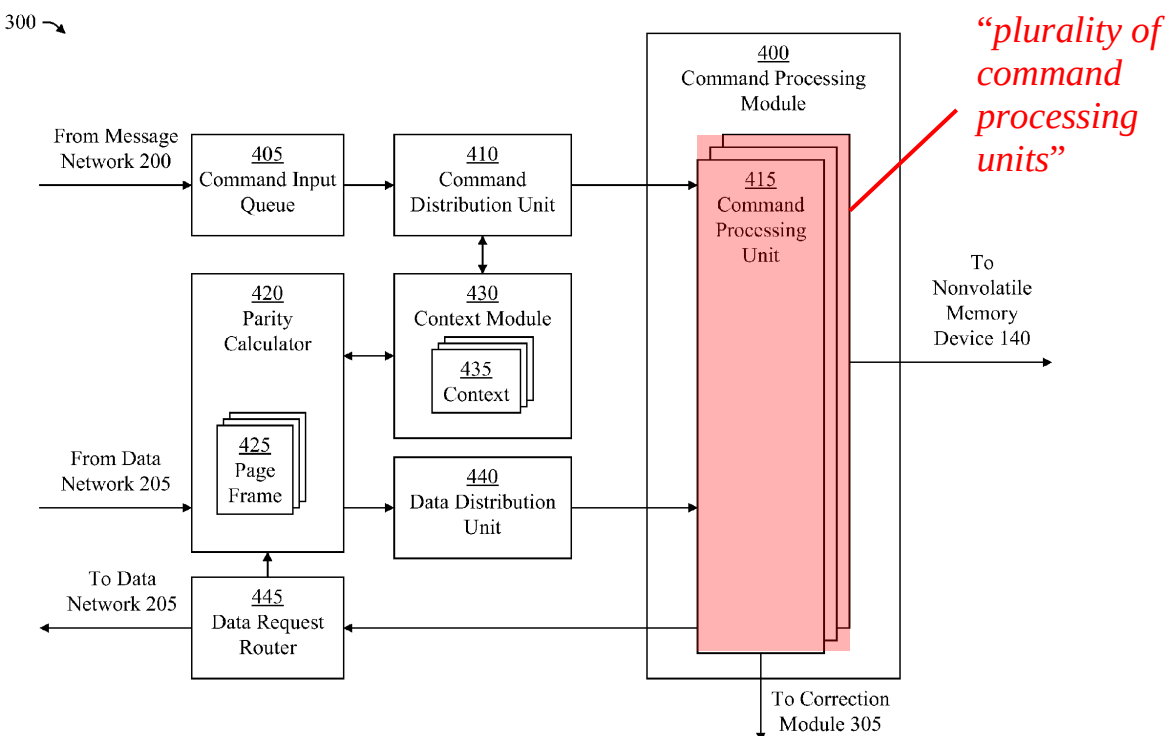
Dr. Paul Min's declaration provides a brief background section describing memory systems, Redundant Array of Independent Disks (RAID), and parity data. Ex.1003, ¶¶29-34.

V. SUMMARY OF THE '346 PATENT

The '346 patent describes and claims nothing more than well-known techniques to calculate and store parity data for a data stripe operation. The '346 relates to a "nonvolatile memory controller performs a data stripe operation on data blocks." Ex.1001, abstract. "The nonvolatile memory controller includes command processing units, each of which processes a command of the data stripe operation

to store a data block into a nonvolatile memory device.” Ex.1001, abstract. The non-volatile memory controller also includes a “parity calculator [that] generates a parity block.” Ex.1001, abstract.

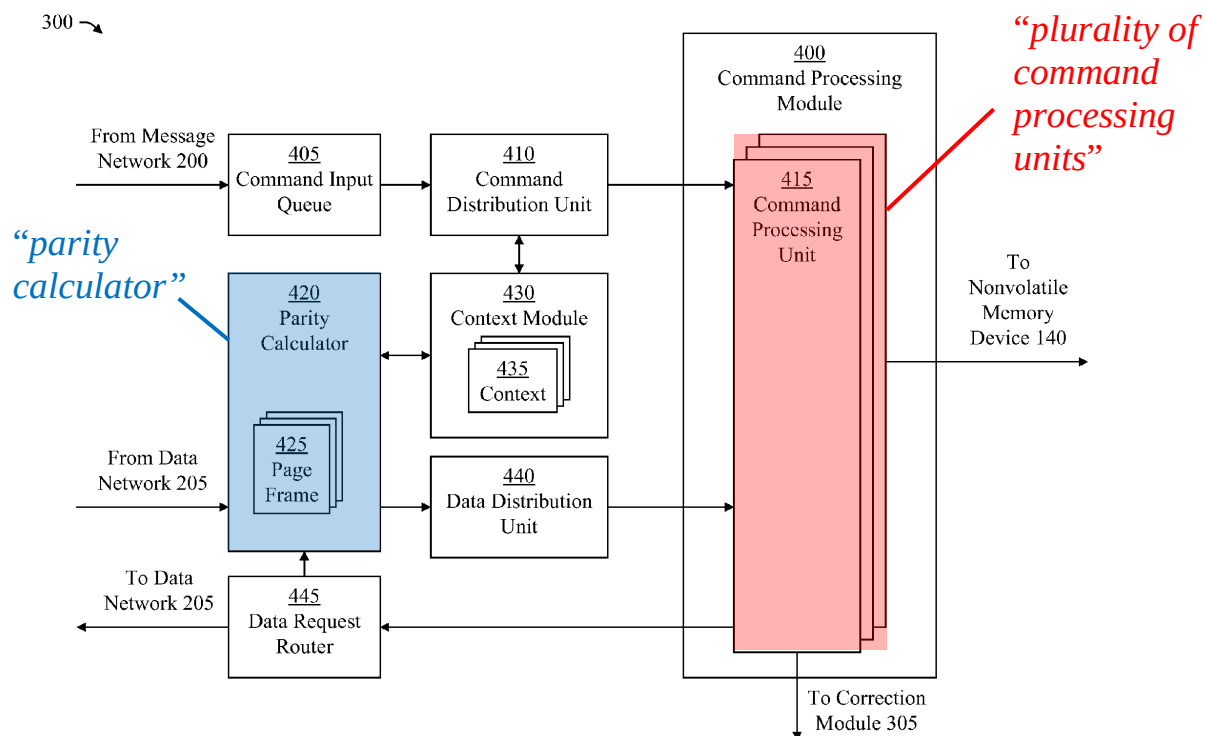
One purported novelty of the ’346 patent is that commands are distributed across a plurality of command processing units. To process these commands, the claimed “nonvolatile memory controller includes a number of command processing units, each of which receives a command in the collection of commands.” Ex.1001, 1:53-55. The plurality of command processing units are shown in Fig. 4 below.



Ex.1001, Fig. 4 (annotated); Ex.1003, ¶36.

The '346 patent also purports to address the complexity of calculating parity data. The '346 patent acknowledges that “generation of parity data in a RAID operation is often a computationally intensive task.” Ex.1001, 1:33-35. In purported conventional systems, each of the “data blocks of a data stripe operation are stored in individual data buffers when computing a parity block.” Ex.1001, 2:16-17. These “data buffers consume a considerable amount of area and power in integrated circuit implementations of the disk drive controller.” Ex.1001, 1:44-46.

Accordingly, rather than storing each of the data blocks in a buffer at the same time, the “parity calculator generates the parity block **on the fly** as the command processing units are receiving the data blocks for the data stripe operation.” Ex.1001, 2:1-3. To do this, the “parity calculator generates a parity block by storing a first data block of the sequence of data blocks into a page frame and updating the data block stored in the page frame with each remaining data block in the sequence of data blocks.” Ex.1001, 1:63-67. The parity calculator is shown in Fig. 4 below.

**Ex.1001, Fig. 4 (annotated); Ex.1003, ¶38.**

The claims of the '346 patent were allowed after the Applicant made amendments directed to performing parity calculations on the fly: "by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer." Ex.1002, 146.

However, as will be explained in detail below, calculating parity data "on-the-fly," as well as distributing the commands among multiple command processors, were already well-known concepts at the time the '346 patent was filed. Ex.1003, ¶¶35-40.

VI. PROSECUTION HISTORY OF THE '346 PATENT

The '346 patent was filed on March 21, 2011 and claims priority to a provisional application filed August 16, 2010. In a first Office Action, the claims were rejected by the Examiner and found obvious over U.S. Patent Publication No. 2009/0077302 to Fukuda et al. ("Fukuda") and U.S. Patent Publication No. 2010/0185808 to Yu ("Yu").

To overcome the rejection, the Applicant added amendments directed to performing parity calculation on-the-fly. The claims were amended to recite that the parity block is generated "by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer." Ex.1002, 146. The Examiner then allowed the claims and the '346 patent issued on December 3, 2013.

However, as will be explained in detail below, calculating parity data "on the fly" was already well-known concepts at the time the '346 patent was filed. Ex.1003, ¶¶41-43.

VII. LEVEL OF ORDINARY SKILL IN THE ART

A Person of Ordinary Skill in The Art ("POSITA") in August of 2010 would have had a working knowledge of the memory system art that is pertinent to the '346 patent, including memory systems and memory controllers. A POSITA would

have had a bachelor's degree in electrical engineering computer science, or an equivalent, and approximately two years of professional experience working in the field of memory systems. Lack of professional experience can be remedied by additional education, and vice versa. Ex.1003, ¶¶22-24.

VIII. CLAIM CONSTRUCTION

Claim terms in IPR are construed according to their “ordinary and customary meaning” to those of skill in the art. 37 C.F.R. § 42.100(b). Petitioner submits that, for the purposes of this proceeding and the Grounds presented herein, the following phrase should be construed.

“without storing each data block in a data buffer.”

Based on the structure of the claims as well as the specification and the prosecution history, the limitation “*without storing each data block in a data buffer*” should be construed as “*without storing each data block in a data buffer at the same time.*” In other words, the claims do **not** require that each data block never pass through any buffer during the parity calculation process (as that would not be possible). Rather, the claims merely require that there is no single point in time in which each of the data blocks involved in the parity calculation are stored in a buffer together. That is, as each data block passes through the buffer, the parity calculation is updated using that block.

The claim language itself suggests this interpretation because the claims

recite that the first block is stored in a page frame, which is a type of buffer. Claim 1 recites “to generate a parity block by **storing a first data block** of the sequence of data blocks **into the page frame** and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer.” The page frame itself is a temporary storage for the first block and is thus a type of buffer. It would thus contradict the claim language to interpret “without storing each data block in a data buffer” to mean that a data block can never pass through a buffer during parity calculation. Accordingly, a POSITA would have understood that this term to mean that the parity block is generated *without storing each data block in a data buffer at the same time*.

The specification of the '346 patent supports this interpretation as well. The specification of the '346 patent states that conventionally, a “dedicated processor stores data blocks into individual data buffers of the disk drive controller, executes computing instructions to generate parity data, and stores the parity data into yet another data buffer.” Ex.1001, 1:37-40. The '346 patent further states that “data buffers consume a considerable amount of area and power in integrated circuit implementations of the disk drive controller.” Ex.1001, 1:44-46.

The '346 patent purports to address the data buffer issue by using an on-the-fly technique:

The parity calculator generates a parity block by storing a first data block of the sequence of data blocks into a page frame and updating the data block stored in the page frame with each remaining data block in the sequence of data blocks. In this way, **the parity calculator generates the parity block on the fly as the command processing units are receiving the data blocks for the data stripe operation.**

Ex.1001, 1:61-2:3.

Moreover, because the parity calculator generates the parity block in the page frame as the parity calculator is receiving the data blocks for the data stripe operation, the parity calculator need not store all the data blocks of the data stripe at the same time when generating a parity block.

Ex.1001, 2:9-13.

As a result of using this on-the-fly technique, the '346 patent purports that “the nonvolatile memory controller consumes less power and area than other nonvolatile memory controllers in which data blocks of a data stripe operation are stored in individual data buffers when computing a parity block.” Ex.1001, 2:13-17. Accordingly, a POSITA would have understood that what the '346 patent seeks to capture, is that the parity block is generated on-the-fly rather than by storing each of the data blocks in an individual buffer at the same time to perform the parity calculation.

For this reason as well, a POSITA would have understood this term to mean

that the parity block is generated *without storing each data block in a data buffer at the same time*. Ex.1003, ¶¶44-50.

IX. RELIEF REQUESTED AND THE REASONS FOR RELIEF

Petitioner asks that the Board institute a trial for *inter partes* review and cancel the Challenged Claims in view of the analysis below.

X. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE

A. Challenged Claims

Petitioner challenges claims 1-11 and 13-18.

B. Statutory Grounds for Challenges

Grounds	Claims	Basis
#1	1-3, 5-11, 13-16, and 18	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Jeddeloh, Kleiman, and Ma
#2	4 and 17	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Jeddeloh, Kleiman, Ma, and Yashiro

U.S. Patent Publication No. 2011/0078496 to Jeddeloh (“Jeddeloh”) was filed September 29, 2009 and published on March 31, 2011. Jeddeloh is thus prior art to the ’346 patent under pre-AIA 35 U.S.C. 102(e).

U.S. Patent No. 5,950,225 to Kleiman (“Kleiman”) was filed February 28, 1997 and issued Sept. 7, 1999. Kleiman is thus prior art to the ’346 patent under at least pre-AIA 35 U.S.C. 102(b).

U.S. Patent No. 8,341,332 to Ma et al. (“Ma”) was filed August 5, 2008 and

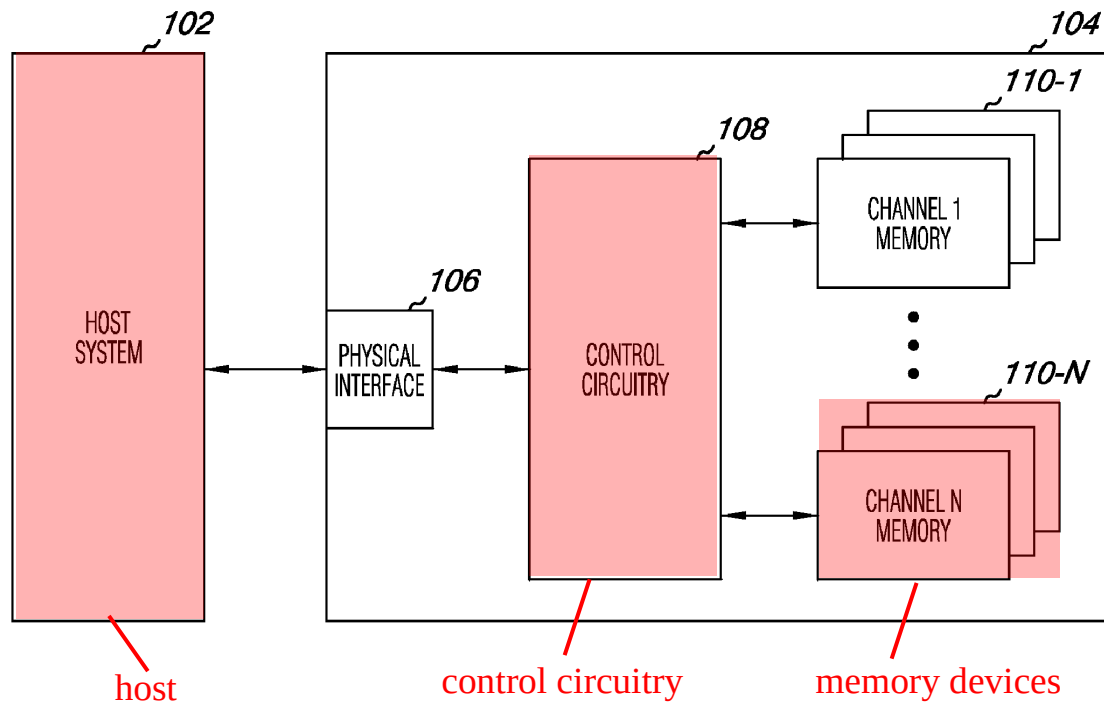
issued on December 25, 2012. Ma is thus prior art to the '346 patent under pre-AIA 35 U.S.C. 102(e).

U.S. Patent No. 5,787,460 to Yashiro et al. ("Yashiro") was filed Nov. 6, 1996 and issued on July 28, 1998. Yashiro is thus prior art to the '346 patent under at least pre-AIA 35 U.S.C. 102(b).

C. Ground 1: Claims 1-3, 5-11, 13-16, and 18 are obvious in view of Jeddeloh, Kleiman, and Ma.

1. Summary of Jeddeloh.

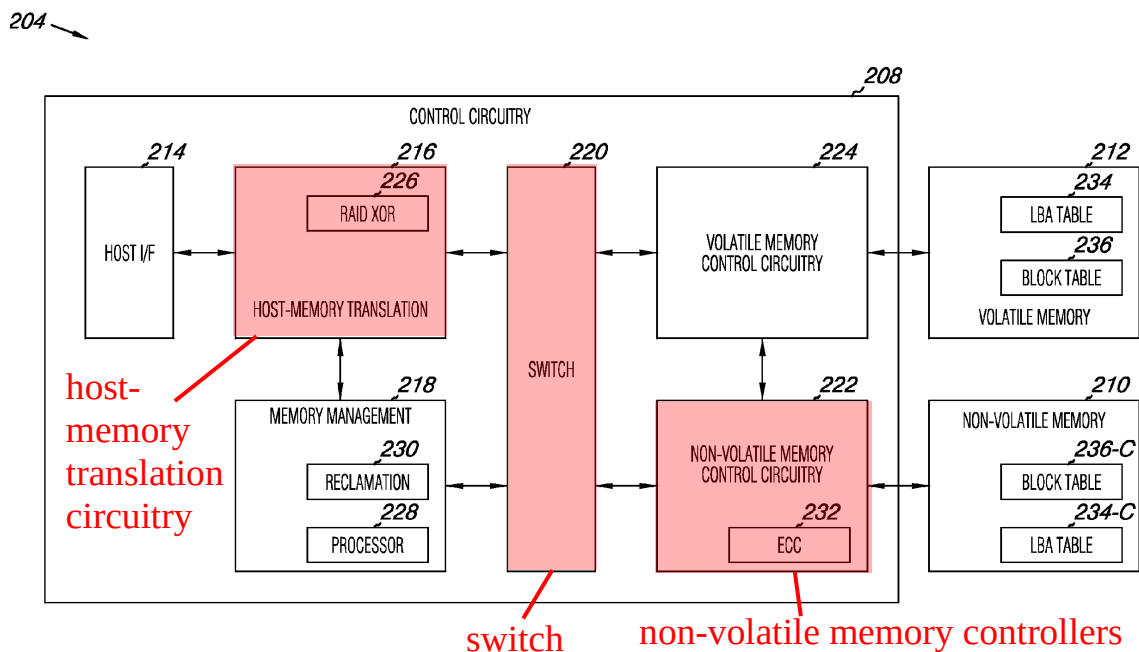
Jeddeloh, like the '346 patent, "relates generally to semiconductor memory devices." Ex.1005, [0001]. Consistent with its title, Jeddeloh describes a "stripe-based memory operation." Ex.1005, [0001]. To perform stripe-based memory operations, Jeddeloh's system includes memory control circuitry 108 for managing memory operations between a host 102 and the multiple memory devices 110 of the stripe operation. Ex.1005, [0015].



Ex.1005, Fig. 1 (annotated); Ex.1003, ¶54.

Jeddeloh illustrates the control circuitry in more detail with respect to Fig. 2.

“The memory system control circuitry 208 can include host interface circuitry 214, host-memory translation circuitry 216, memory management circuitry 218, a switch 220, non-volatile memory control circuitry 222, and/or volatile memory control circuitry 224.” Ex.1005, [0024].

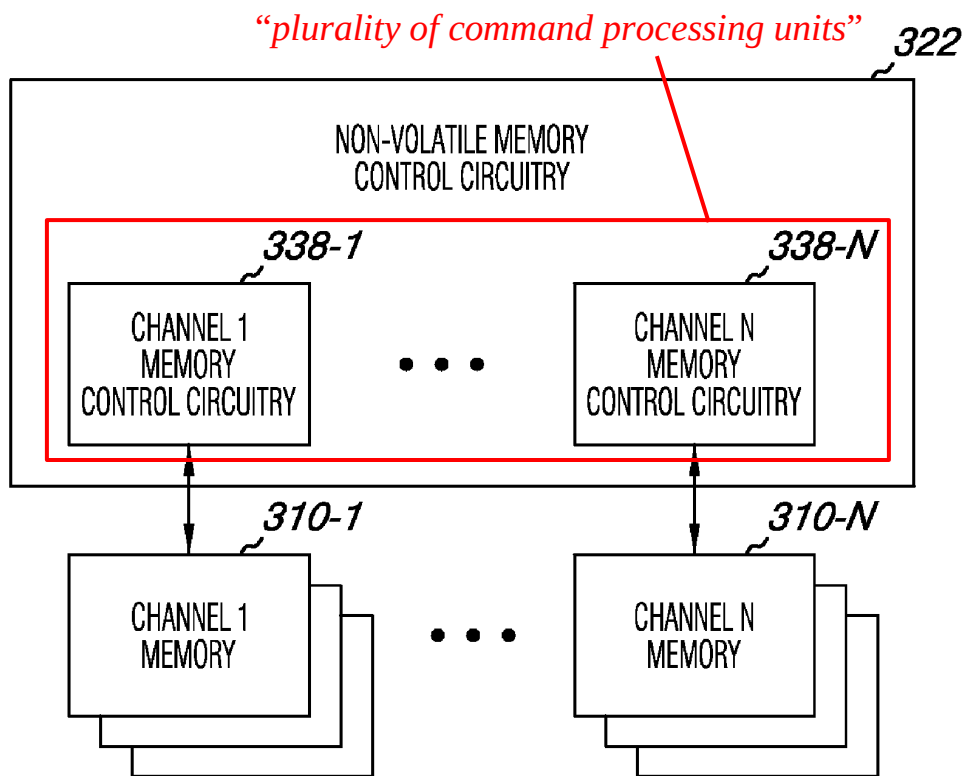
**Ex.1005, Fig. 2 (annotated); Ex.1003, ¶55.**

As shown in Fig. 2, Jeddeloh’s “switch 220 can be coupled to the host-memory translation circuitry 216, the memory management circuitry 218, [and] the non-volatile control circuitry 222.” Ex.1005, [0033]. Jeddeloh further explains that “the switch 220 can be a direct memory access (DMA) module.” Ex.1005, [0033].

Like the ’346 patent, Jeddeloh’s memory control circuitry 208 includes a parity calculator. In particular, “[t]he host-memory translation circuitry 216 can include second level error detection/correction circuitry, such as RAID exclusive or (XOR) circuitry 226. The RAID XOR circuitry 226 can calculate parity data based on data received from the host interface circuitry 214.” Ex.1005, [0027]; *see also* Ex.1005, [0044].

Also like the ’346 patent, Jeddeloh utilizes a plurality of command

processing units to perform the stripe operation. Jeddeloh's non-volatile memory control circuitry 222 includes a plurality of discrete channel memory control circuits 338-1 ... 338-N: "In one or more embodiments, each solid state memory device 310-1, . . . , 310-N can be coupled to the non-volatile memory control circuitry 322 [222 in Fig. 2] by a separate channel. Each channel can be associated with discrete channel memory control circuitry 338-1, . . . , 338-N." Ex.1005, [0038]. The channel memory control circuitry performs "a number of operations on the one or more solid state memory devices 310-1, . . . , 310-N including page read, stripe write, and stripe erase." Ex.1005, [0038]. The discrete channel memory controllers are shown in further detail with respect to Fig. 3, shown below.



Ex.1005, Fig. 3 (annotated); Ex.1003, ¶58.

Thus, Jeddelloh provides evidence that it was known to distribute the processing of commands for a data stripe operation among multiple command processing units, as well as to calculate parity data. Ex.1003, ¶¶54-59.

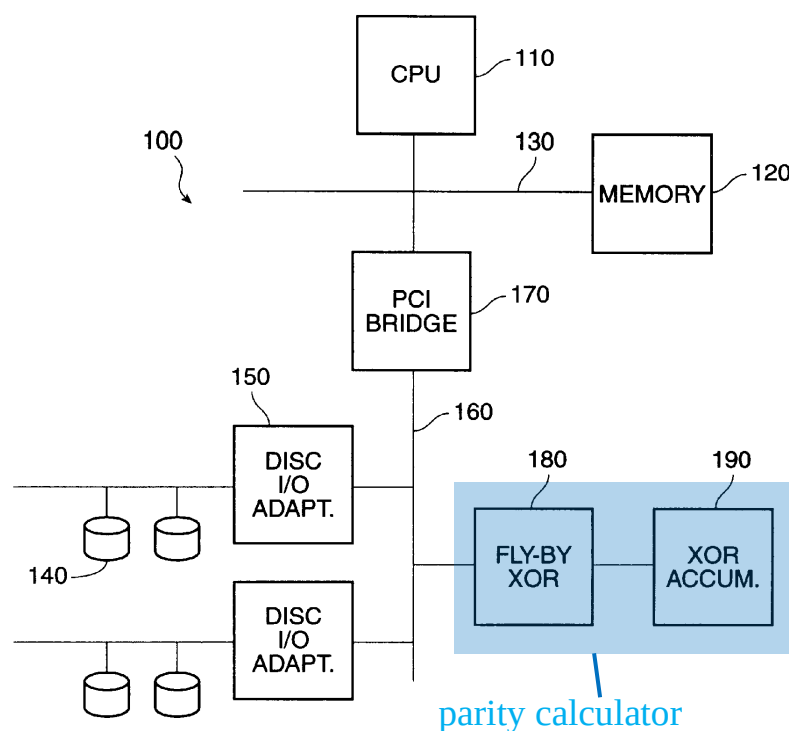
2. Summary of Kleiman.

Kleiman provides evidence that it was known to perform parity calculations “on-the-fly.” Ex.1006, abstract. Like Jeddelloh and the ’346 patent, Kleiman relates to a “method and system for performing XOR operations without consuming substantial computing resources.” Ex.1006, abstract. Kleiman, which is entitled “Fly-by XOR for Generating Parity for Data Gleaned from a Bus,” describes the

same on-the-fly parity calculation technique described by the '346 patent. See Ex.1006, abstract.

Kleiman describes a “fly-by XOR element 180” that “uses an XOR buffer 190 for saving partial and final results of XOR operations.” Ex.1006, 3:3-5.

Kleiman’s fly-by XOR element 180 is shown in Fig. 1 below.



Ex.1006, Fig. 1 (annotated); Ex.1003, ¶62.

Kleiman’s fly-by XOR element detects data transfers to the storage disks. “When the fly-by XOR element 180 recognizes such a transfer, it copies the data being transferred and adds it (by performing an XOR operation) to the accumulated parity information in the associated XOR accumulator buffer.”

Ex.1006 3:60-64. “When all data for the recognized memory buffer has been transferred, the associated XOR accumulator buffer holds the computed parity for the RAID stripe.” Ex.1006, 3:65-67; *see also* Ex.1006, 4:1-6. Thus, Kleiman provides evidence that it was known to utilize an on-the-fly technique for parity calculation in which the data blocks are not stored in a buffer at the same time. Ex.1003, ¶¶60-64.

3. Reasons to Combine Jeddelloh and Kleiman.

A POSITA would have found it obvious for Jeddelloh’s parity calculator to use an on-the-fly technique as taught by Kleiman. Ex.1003, ¶65. Jeddelloh describes a parity calculator generally: “RAID XOR circuitry 226 can calculate parity data based on data received from the host interface circuitry 214.” Ex.1005, [0027]. A POSITA would have looked to known techniques to implement the RAID XOR circuitry. Ex.1003, ¶65.

Kleiman provides an example of one known way to implement RAID circuitry. Kleiman implements a parity calculation technique that calculates parity data on-the-fly: “method of operating a system for performing fly-by XOR.” Ex.1006 3:37-38. In particular, “the fly-by XOR element 180 ... copies the data being transferred and adds it (by performing an XOR operation) to the accumulated parity information in the associated XOR accumulator buffer.” Ex.1006 3:60-65. Then, “[w]hen all data for the recognized memory buffer has

been transferred, the associated XOR accumulator buffer holds the computed parity for the RAID stripe.” Ex.1006, 3:65-67; Ex.1003, ¶66.

A POSITA would have been motivated to utilize Kleiman’s on-the-fly technique because it provides various benefits.

- **First**, Kleiman’s on-the-fly technique “performs XOR operations on data transferred to and from the disk drives without requiring separate transfers.” Ex.1006, 1:67-2:2.
- **Second**, the on-the-fly technique “dynamically computes a set of parity information for the RAID stripe, without requiring additional resources from any part of the system 100.” Ex.1006 3:17-20; Ex.1003, ¶67.

Accordingly, the motivation to combine is explicitly suggested. *KSR Int’l v. Teleflex Inc.*, 550 U.S. 398, 417 (2007).

The results of the proposed combination would have been predictable because Kleiman’s on-the-fly parity calculation is done for the same reason parity data is calculated in Jeddeloh—creating parity data for a RAID stripe operation. Jeddeloh explains that “write data can be striped across multiple solid state memory devices in a RAID operation.” Ex.1005, [0028]. Then, “[t]he memory system, e.g., RAID XOR circuitry 226 ... can calculate parity data for the write data.” Ex.1005, [0044]; Ex.1003, ¶68.

Kleiman likewise performs parity calculation for a RAID scheme. Kleiman explains that “When a RAID stripe is read or written, either entirely or partially, the fly-by XOR element 180 thus dynamically computes a set of parity information for the RAID stripe.” Ex.1006, 3:14-17. Accordingly, a POSITA would have reasonably predicted Kleiman’s on-the-fly technique to be successful within Jeddeloh’s RAID scheme. Ex.1003, ¶69.

A POSITA would have had a reasonable expectation of success because Kleiman’s on-the-fly technique was a well-established method for calculating parity data. *See e.g.*, Ex.1009, abstract (“A high performance data path for performing XOR on the fly.”); Ex.1012, 10:34-37 (“Segments of these data words, e.g. see data paths 342, 344, are written to each of the drives. At this point, a logical XOR operation can be performed between the corresponding bits of the segments ‘on the fly.’”). Ex.1003, ¶70. Accordingly, the combination is nothing more than “the predictable use of prior art elements according to their established functions.” *KSR* 550 U.S. at 417.

Accordingly, the combination of Jeddeloh and Kleiman is merely applying a known technique (Kleiman’s on-the-fly parity calculation) to a known device (Jeddeloh’s RAID XOR circuitry) ready for improvement to yield predictable results (performing parity calculations on-the-fly). *See KSR*, 550 U.S. at 417. Ex.1003, ¶¶65-71.

4. Summary of Ma.

Ma provides additional details as to the processing of write commands. Dr. Min's declaration provides a summary of how Ma provides additional details related to DMA operations of a switch connected to multiple memory controllers. Ex.1003, ¶¶72-75.

5. Reasons to Combine Ma with Jeddeloh and Kleiman.

A POSITA would have found it obvious for Jeddeloh's switch 220—which may be a DMA module—to use known DMA techniques as taught by Ma to communicate with the channel memory controllers 338 and the host. Ex.1003, ¶76.

As explained above, Jeddeloh's memory control circuitry 208 includes a “switch 220 [that] can be coupled to the host-memory translation circuitry 216, the memory management circuitry 218, [and] the non-volatile control circuitry 22.” Ex.1005, [0033]. Jeddeloh further explains that “the switch 220 can be a direct memory access (DMA) module.” Ex.1005, [0033]; Ex.1003, ¶77.

Jeddeloh's switch passes data between the host and the channel memory controllers 338 of the non-volatile memory circuitry 222. “The switch 220 can be coupled to the host-memory translation circuitry 216 [and] the non-volatile control circuitry 222.” Ex.1005, [0033]. Accordingly, Jeddeloh's channel memory controller receives write data through the switch 220. Jeddeloh's channel memory controllers 338 are configured to queue write requests. “A page write command

can be sent, **e.g., queued, to the desired channel memory controller 338-1, . . . , 338-N** and executed on the one or more solid state memory devices 310-1, . . . , 310-N.” Ex.1005, [0040]. Jeddeloh then explains that the data may be obtained from the host. In one example, “Write data for a stripe write operation **can be received from a host system**, e.g., host system 102 in FIG. 1.” Ex.1005, [0040]; Ex.1003, ¶78.

Given that Jeddeloh’s switch may be a DMA module, a POSITA would have found it obvious to look to known techniques for DMA operations between a switch and a plurality of memory controllers. Ex.1003, ¶79. In other words, by referring to DMA techniques, Jeddeloh explicitly suggests the combination. *See In re Kahn*, 441 F.3d 977, 986 (Fed. Cir. 2006) (obviousness may be established by combining or modifying prior art elements when there is a teaching, suggestion, or motivation to do so). Ma provides an example of such known techniques. In particular, Ma provides evidence that it was known for a memory controller to request data from the host when processing write commands in a queue. Like both Jeddeloh and the ’346 patent, Ma “relates to flash-memory solid-state-drive (SSD) devices.” Ex.1007, 1:52-53.

Ma explains that when one of the memory controllers on a flash device is ready to write data, it “sends a DMA activate back to host 10 through smart storage switch 30 to indicate that it is ready for the DMA transfer to begin.” Ex.1007,

10:61-63. In response to the DMA activate request, the “host 10 sends one or more data-out packets to smart storage switch 30, which takes the data and forms one or more data-out packets to send to endpoint-1, with the data to write into flash memory blocks in first single-chip flash-memory device 73.” Ex.1007, 11:45-49. “NVM controller 76 in first single-chip flash-memory device 73 receives these data packets and then writes this data into its flash memory blocks 68 and responds with a status packet back to smart storage switch 30.” Ex.1007, 11:51-54; Ex.1003, ¶80.

A POSITA would have thus found it obvious to implement Jeddelloh’s system such that the channel memory controller sends a DMA request to the host (through the switch) when processing a command from its queue. Ex.1003, ¶81. Jeddelloh’s switch would then send back the requested data as a data-out packet so that the channel memory controller can write the data within that packet to its channel memory. Ex.1003, ¶81. Indeed, the combination is nothing more than “the predictable use of prior art elements according to their established functions.” *KSR* 550 U.S. at 417.

A POSITA would have had a reasonable expectation of success when combining the teachings of Ma with those of Jeddelloh. Both Jeddelloh and Ma relate to solid-state storage devices that stripe data across multiple storage devices. *See e.g.*, Ex.1005, [0036] (“The non-volatile memory control circuitry 222 can be

configured to operate a number of non-volatile memory devices associated with the number of memory channels as a RAID.”); Ex.1007, 2:56-58 (“It is further desired that the smart storage switch interleaves and stripes data accesses to the multiple channels of single-chip flash-memory devices.”). Accordingly, a POSITA would have expected Ma’s DMA techniques to work similarly within Jeddelloh’s system. Ex.1003, ¶82.

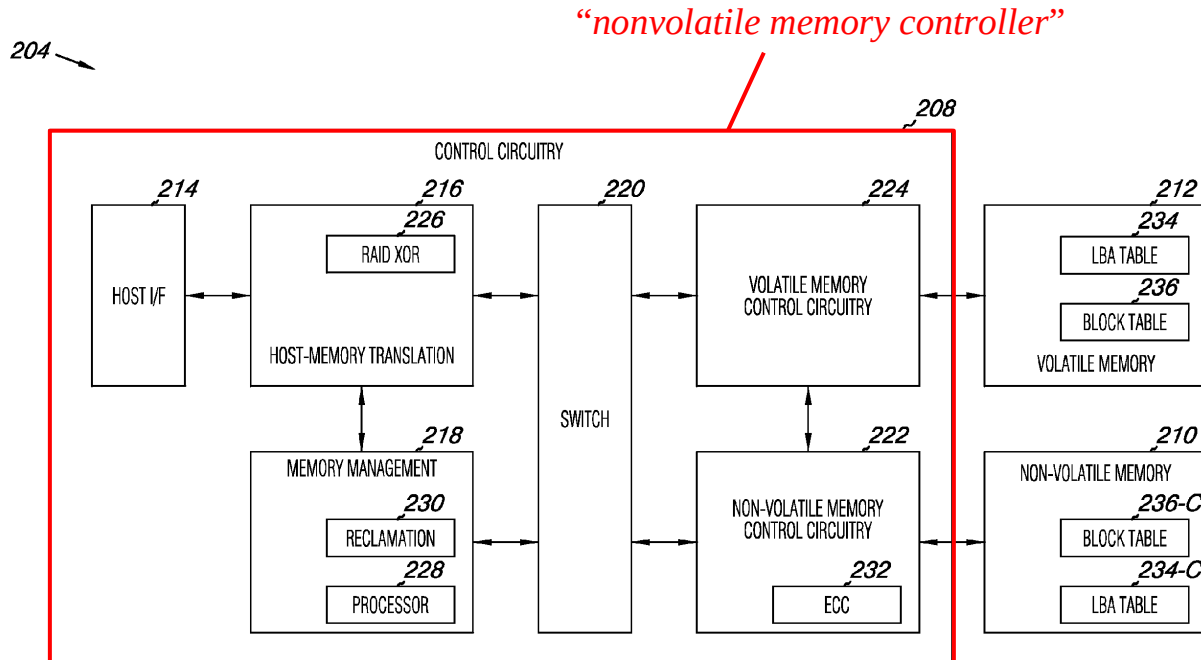
Accordingly, the combination of Jeddelloh and Ma is merely applying a known technique (Ma’s DMA technique) to a known device (Jeddelloh’s memory control circuitry) ready for improvement to yield predictable results (obtaining write data from the host when ready). Ex.1003, ¶¶76-83.

6. Claim 1

[1.0] A nonvolatile memory controller for performing a data stripe operation on a plurality of data blocks, the nonvolatile memory controller comprising:

To the extent the preamble is limiting, it is rendered obvious by Jeddelloh. Ex.1003, ¶84.

First, Jeddelloh describes memory system control circuitry 208 (“*nonvolatile memory controller*”) for controlling non-volatile memory. “The memory system 204 can include memory system control circuitry 208. The memory system control circuitry 208 can be coupled to one or more solid state memory devices, e.g., non-volatile memory 210.” Ex.1005, [0023].



Ex.1005, Fig. 2 (annotated); Ex.1003, ¶85.

Second, Jeddeloh’s memory system control circuitry performs a stripe-based memory operation (“*data stripe operation*”). See Ex.1005, title (“Stripe Based Memory Operation”). “The present disclosure includes methods and devices for **stripe-based memory operation**. One method embodiment includes writing data in **a first stripe across a storage volume of a plurality of memory devices**.” Ex.1005, [0012].

Third, Jeddeloh’s stripe-based memory operation is performed on a plurality of pages (“*a plurality of data blocks*”). “A stripe write operation can include a plurality of page write operations, e.g., one page write operation per each channel associated with the non-volatile memory control circuitry 322.” “For

example, a page write operation can support 4 kilobyte (KB), 8 KB, or another volume of data, depending upon solid state memory device 310-1, . . . , 310-N page size, plus meta-data.” Ex.1005, [0040].

By performing the stripe operation on a plurality of memory pages, Jeddeloh teaches performing a stripe operation on “*a plurality of data blocks*” under the various ways a POSITA would have understood the term “block.” For example, a memory page is a structured form of data and is thus a “block” as claimed. Ex.1003, ¶88.

Additionally, Jeddeloh’s memory pages include logical blocks (the smallest unit of addressable memory). “In one or more embodiments of the present disclosure, and as shown in FIG. 5, a page can store data in a number of sectors.” Ex.1005, [0062]. “As one of ordinary skill in the art will appreciate, **logical block addressing** is a scheme that can be used by a host for identifying a sector of information, e.g., each sector can correspond to a unique LBA. In one or more embodiments, a sector is the smallest addressable portion of a storage volume.” Ex.1005, [0062]. Accordingly, because the stripe operation is performed on memory pages, which are comprised of sector/LBAs (logical *block* addresses), Jeddeloh teaches performing a stripe operation on “*a plurality of data blocks*.”

As another example, Jeddeloh explains that its memory pages can be organized into a larger structure referred to as a block. “The memory arrays can

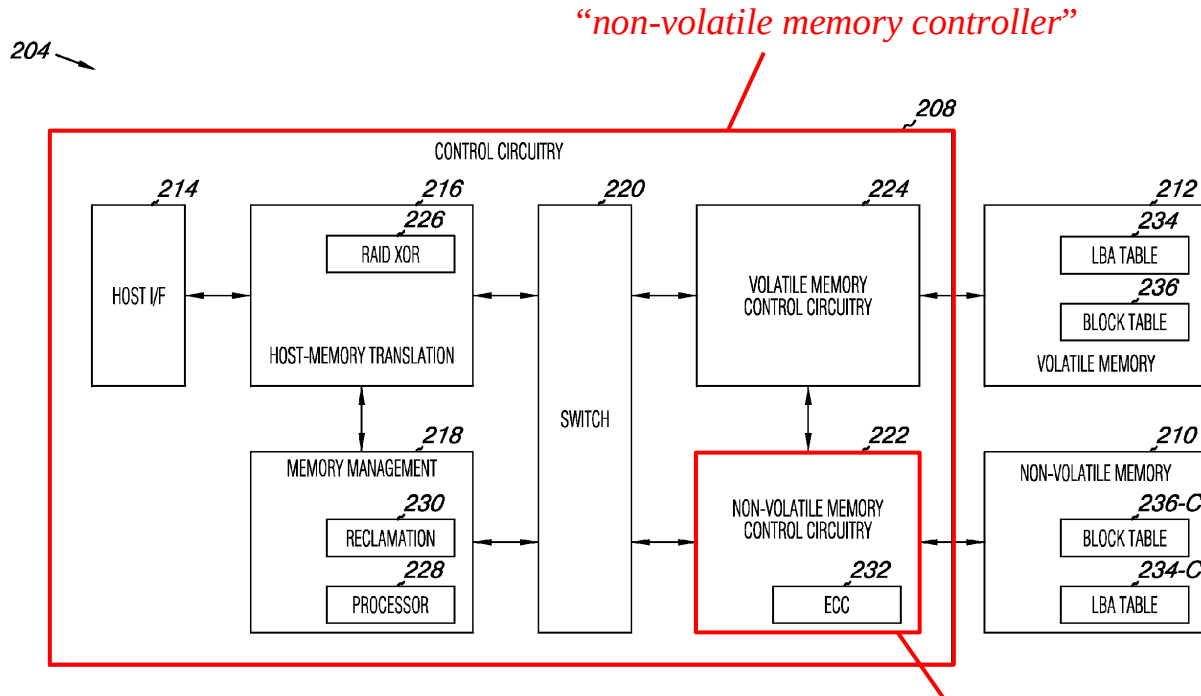
include a number of memory cells organized into a number of physical pages, and the physical pages can be organized into a number of blocks.” Ex.1005, [0005].

Accordingly, when Jeddeloh’s system performs a stripe operation on memory pages, which can be organized into a number of blocks, the stripe operation is performed on “*a plurality of data blocks*” regardless of how the term block is interpreted. Ex.1003, ¶90.

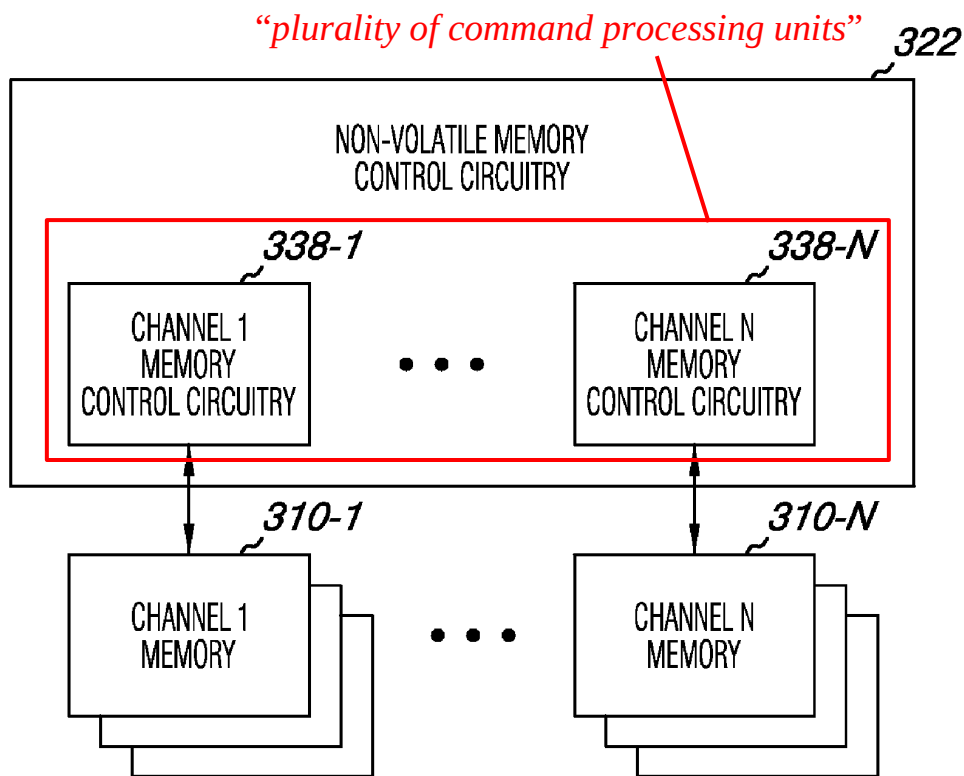
Thus, because Jeddeloh describes memory control circuitry for performing a data stripe operation on a plurality of memory pages, which are comprised of LBAs and together form larger blocks, Jeddeloh renders this limitation obvious. Ex.1003, ¶¶84-92.

[1.1] *a plurality of command processing units, each command processing unit of the plurality of command processing units configured to receive a command of a plurality of commands for performing the data stripe operation,*

First, Jeddeloh’s control circuitry 208 includes non-volatile memory control circuitry 222, which includes a plurality of channel memory control circuits 338 (“*plurality of command processing units*”). “The memory system control circuitry 208 can include ... non-volatile memory control circuitry 222.” Ex.1005, [0024]. “The non-volatile memory control circuitry 222 can be configured to write data in a first stripe across a number of memory channels as described herein.” Ex.1005, [0036].

**Ex.1005, Fig. 2 (annotated); Ex.1003, ¶93.**non-volatile memory
control circuitry

Jeddeloh's non-volatile memory control circuitry 222 includes a plurality of discrete channel memory control circuits 338-1 ... 338-N (*"plurality of command processing units"*). "In one or more embodiments, each solid state memory device 310-1, . . . , 310-N can be coupled to the non-volatile memory control circuitry 322 by a separate channel. Each channel can be associated with discrete channel memory control circuitry 338-1, . . . , 338-N." Ex.1005, [0038]; *see also* Ex.1005, [0038].



Ex.1005, Fig. 3 (annotated); Ex.1003, ¶94.

Jeddeloh’s channel memory control circuits 338 are “*command processing units*” because they process various operations “including page read, stripe write, and stripe erase.” Ex.1005, [0038]. “A stripe write operation can include a plurality of page write operations, e.g., one page write operation per each channel associated with the non-volatile memory control circuitry 322.” Ex.1005, [0040].

Second, in a data stripe operation that includes a plurality of commands, the different channel memory control circuits receive different commands (“*each command processing unit of the plurality of command processing units configured to receive a command of a plurality of commands for performing the data stripe*”).

operation”). For example, during a stripe operation across each of the channel memory devices 310-1 ... 310-N, each of the corresponding channel control circuits will process its respective command for that stripe operation. “A stripe write operation can include a plurality of page write operations, e.g., one page write operation per each channel associated with the non-volatile memory control circuitry 322. In one or more embodiments, the plurality of page write operations in the stripe write operation can be performed substantially simultaneously across the plurality of channels.” Ex.1005, [0040]. “Write data can be striped across a storage volume of a plurality of solid state memory devices 310-1, . . . , 310-N.” Ex.1005, [0041].

Thus, because Jeddeloh’s memory control circuitry includes a plurality of channel memory circuits to process commands, and each of those channel memory circuits receives a command that is part of a data stripe operation, Jeddeloh renders this limitation obvious. Ex.1003, ¶¶93-97.

[1.2] *the plurality of commands including a plurality of data update commands and a parity write command,*

First, Jeddeloh explains that the commands provided to the channel memory circuits (“*command processing units*”) include “*data update commands.*” “A memory system can receive ... a write command and updated write data associated with a particular one or more of the LBAs associated with the data

written in the first stripe 444-1, e.g., an LBA that is the same as at least one

LBA associated with data written in the first stripe 444-1.” Ex.1005, [0050];

see also [0051]. Accordingly, because some write commands are used to write

“updated write data associated with a particular one or more of the LBAs,” they are

“*data update commands*” as claimed. Ex.1005, [0050]; Ex.1003, ¶98.

Second, the commands provided to the channel memory circuits also include

parity write commands. “Storing parity data can allow data associated with an

effectively removed portion of a memory stripe to be recreated, e.g., a portion that

experiences a UECC error.” Ex.1005, [0047]. “In some embodiments that include

writing parity data along with the write data, at least one fragment of write data

can be written to one or more memory devices associated with a first subset of the

channels ... and parity data can be written to one or more memory devices

associated with a second subset of the channels.” Ex.1005, [0049]; *see also*

Ex.1005, [0028] (“write data can be striped across seven of eight memory devices,

where parity data can be stored in an eighth memory device”), [0044] (“a

memory system can include eight channels where seven channels are used for

writing write data and **one channel is used for writing parity data**”).

Jeddeloh explains that one memory channel and its associated memory

device may be dedicated to parity data. “At least one of the number of memory

channels can be operated as a parity channel and accordingly, one or more memory

devices associated with the at least one of the number of memory channels can be operated as a parity memory device(s).” Ex.1005, [0036]. Accordingly, a write command processed by the channel memory controller 338 for the dedicated parity device is a “*parity write command*” as claimed.

Additionally, a POSITA would have found it obvious to use parity write commands when writing parity data. It was known in the art to use a parity write command when writing parity data to memory. *See e.g.*, Ex.1014, 3:3-5 (“The current proposed ANSI standard for “XOR commands” on SCSI disk drives includes read (READ), data update (XDWRITE), parity update (XPWRITE)”; Ex.1003, ¶103. Accordingly, it would have been obvious to use a parity update command, such as XPWRITE, when writing parity data to a dedicated parity channel.

Thus, because Jeddeloh describes that the commands processed by the memory channel circuits include data update commands and parity write commands, Jeddeloh renders this limitation obvious. Ex.1003, ¶¶98-104.

[1.3a] *each command processing unit of the plurality of command processing units receiving a data update command of the plurality of data update commands configured to request a data block of the plurality of data blocks based on the data update command,*

A POSITA would have found it obvious for Jeddeloh’s channel memory circuits 328 to request and receive pages for writing to memory according to

known DMA techniques, as taught by Ma.

First, as explained above at [1.2], channel memory control circuits receive data update commands (*“each command processing unit of the plurality of command processing units receiving a data update command of the plurality of data update commands”*).

Second, when implementing the DMA techniques mentioned by Jeddeloh, the channel memory circuits (*“command processing units”*) are configured to *“request a data block”* as claimed. Jeddeloh explains that write commands are queued to the channel memory controllers, and that the channel memory controllers then write data received from the host system. “A page write command can be sent, **e.g., queued, to the desired channel memory controller 338-1, . . . , 338-N** and executed on the one or more solid state memory devices 310-1, . . . , 310-N.” Ex.1005, [0040]. “Write data for a stripe write operation can be received from a host system, e.g., host system 102 in FIG. 1.” Ex.1005, [0040].

As explained above at X.C.5, it would have been obvious for Jeddeloh’s memory control circuitry 208 to utilize DMA operations. *See e.g.*, Jeddeloh, [0033]; Ex.1003, ¶107. A POSITA would have understood that when a particular channel memory control circuit processes the next command in the queue, it would request that data when ready, as taught by Ma: “flash-memory device 73 ... sends a DMA activate back to host 10 to indicate that it is ready for the DMA transfer to

begin.” Ex.1007, 11:40-44.

Accordingly, by sending a DMA activate message to the host, the DMA host is requesting the write data from the host (“*to request a data block of the plurality of data blocks based on the data update command*”). Accordingly, a POSITA would have found it obvious for Jeddeloh’s channel memory controllers 338 to similarly request the write data associated with the data update command (“*based on the data update command*”) from the host using a DMA activate message. See *supra* X.C.5; Ex.1003, ¶108.

Thus, because Jeddeloh’s channel memory circuits queue commands that when processed, request data from the host, and Ma provides an example of using DMA operations to do so, Jeddeloh and Ma render this limitation obvious.

Ex.1003, ¶¶105-09.

[1.3b] *[each command processing unit ... configured to] receive the data block in response to the request, and write the data block to a nonvolatile memory device; and*

First, Jeddeloh explains that the channel memory controllers 338 write the data blocks to non-volatile memory. See Ex.1005, [0040]-[0041]. As explained above at [1.3a], Jeddeloh’s channel memory controllers 338—implementing Ma’s DMA technique—request a data block when ready. Similarly, Jeddeloh’s channel memory controllers—implementing Ma’s DMA technique—receive the requested data block (as a data-out packet) in response to the request. “[H]ost 10 sends one or

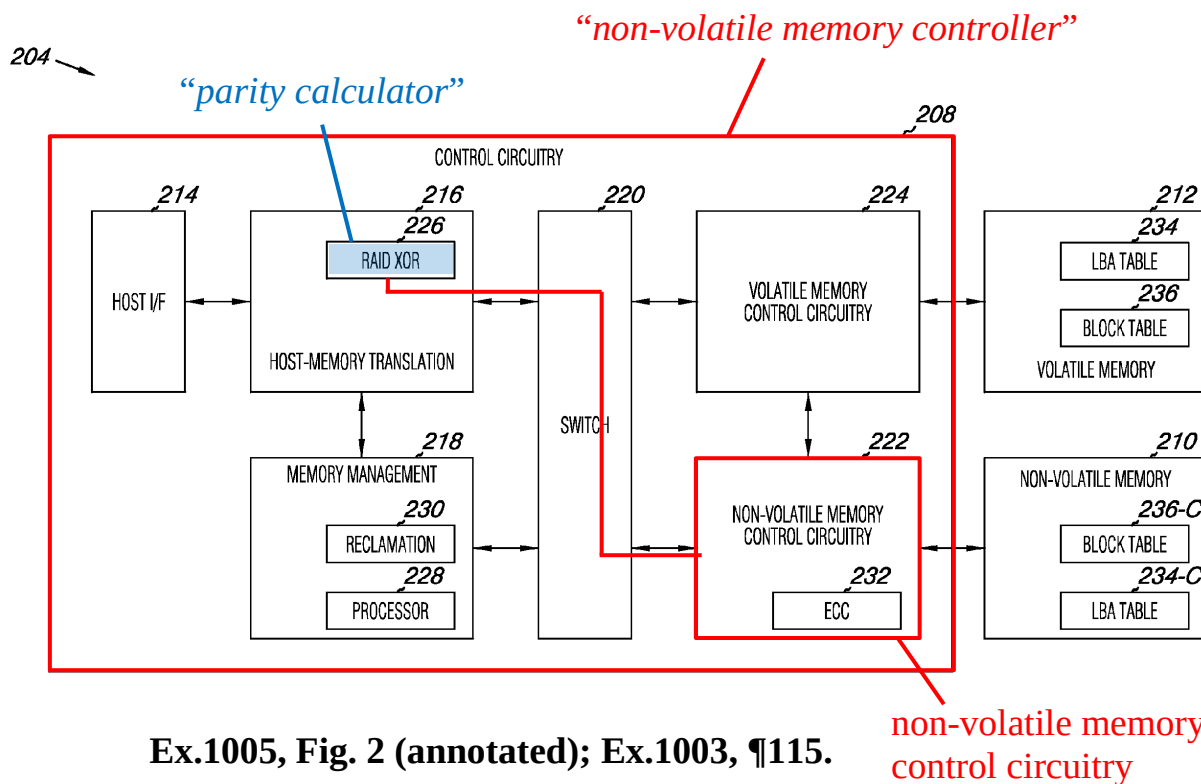
more data-out packets to smart storage switch 30, which takes the data and forms one or more data-out packets to send to endpoint-1, with the data to write into flash memory blocks in first single-chip flash-memory device 73.” Ex.1007, 11:45-50. Accordingly, Jeddeloh’s channel memory controllers—implementing Ma’s DMA technique—would similarly receive from the DMA switch the data-out packets that include the data to write to memory (“*receive the data block in response to the request*”).

Second, Jeddeloh’s channel memory controllers write the data to their respective memory devices “*in response*” to receiving that data from the DMA request. Jeddeloh explains that data that is written is “received from [the] host.” Ex.1005, [0041]. A POSITA would have understood that the data cannot be written to the memory devices until it has been received. As explained by Ma: “NVM controller 76 in first single-chip flash-memory device 73 receives these data packets and then writes this data into its flash memory blocks 68.” Ex.1007, 11:51-55.

Thus, because Jeddeloh’s channel memory controllers write to their respective memory devices, and it would have been obvious to do so in response to receiving the write data according to a DMA operation described in further detail by Ma, Jeddeloh and Ma render this limitation obvious. Ex.1003, ¶¶110-14.

[1.4] a parity calculator coupled to the plurality of command processing units,

First, Jeddeloh's memory control circuit includes RAID XOR circuitry 226 ("a parity calculator"). "The host-memory translation circuitry 216 can include second level error detection/correction circuitry, such as RAID exclusive or (XOR) circuitry 226. The RAID XOR circuitry 226 can calculate parity data based on data received from the host interface circuitry 214." Ex.1005, [0027]; *see also* Ex.1005, [0044]. Jeddeloh's RAID XOR circuitry 226 is shown in Fig. 2 below.



Second, as shown in Fig. 2 above, the RAID XOR circuitry ("parity calculator") is coupled to the channel memory control circuits 338 ("plurality of command processing units") of the non-volatile memory control circuitry 222. *See*

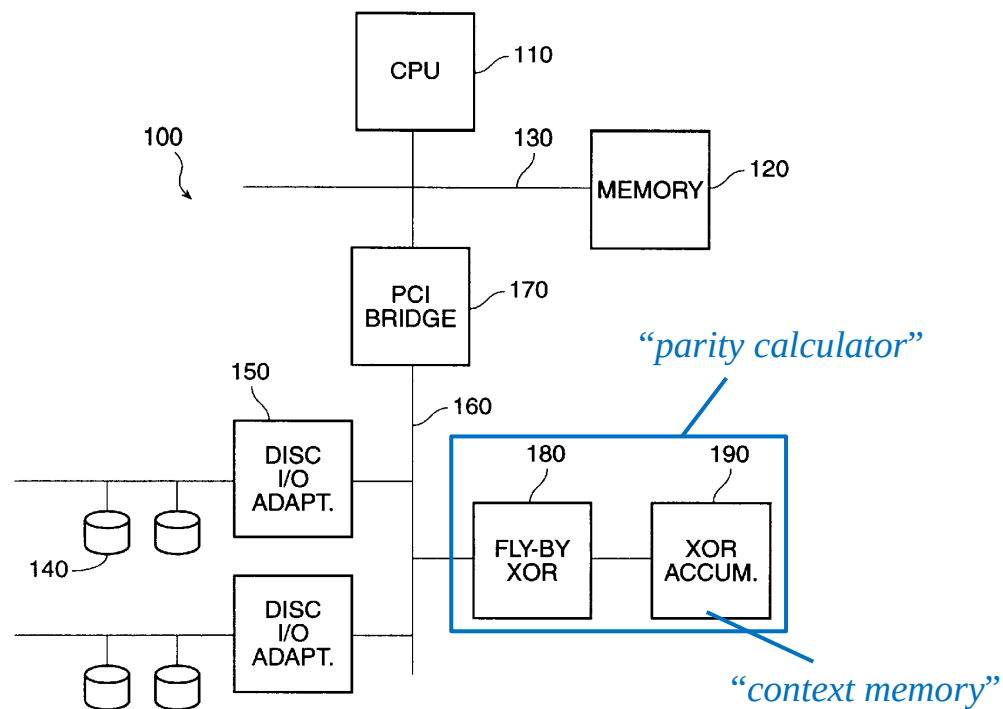
supra [1.1]. Indeed, because the non-volatile memory circuitry (including the channel memory controllers (“*plurality of command processing units*”) receives parity data, they are communicatively coupled to the RAID XOR circuitry that calculates the parity data. See Ex.1005, [0028], [0044].

Thus, because Jeddeloh’s memory control circuit 208 includes RAID XOR circuitry for calculating parity data, and the RAID XOR circuitry is connected to the channel memory circuitry 338 of the non-volatile memory control circuitry 222, Jeddeloh renders this limitation obvious. Ex.1003, ¶¶115-17.

[1.5] *the parity calculator further comprising a context memory including a page frame,*

For the reasons explained above at X.C.2, it would have been obvious for Jeddeloh’s RAID XOR circuitry 226 to be implemented according to Kleiman’s on-the-fly technique. Ex.1003, ¶118.

First, Jeddeloh’s parity calculator—implemented according to Kleiman’s techniques—includes a “*context memory*” as claimed. Kleiman’s on-the-fly technique utilizes a XOR buffer 190 (“*context memory*”) to store the partial parity result until the parity block is complete.



Ex.1006, Fig. 1 (annotated); Ex.1003, ¶119.

In Kleiman, a “fly-by XOR element 180 is coupled to the mezzanine bus 160, so as to glean data from data transfers which use the mezzanine bus 160. The fly-by XOR element 180 uses an XOR buffer 190 for saving partial and final results of XOR operations. Ex.1006, 3:1-5. “As the data is transferred using the mezzanine bus 160, the fly-by XOR element 180 reads the data (without interference with the data transfer) and adds it to one of the XOR accumulators (see FIG. 2) in the XOR buffer 190.” Ex.1006, 3:6-22.

Kleiman’s XOR buffer 190 is a “context” memory as claimed because it maintains the context of the parity calculation, similar to the context memory

described in the '346 patent. *See* Ex.1001, 14:24-30. The context of the operation is maintained by storing the partial results of the parity calculation until all data blocks have passed through. “At a step 222, the ... processor 110 also allocates one of the XOR accumulator buffers in the XOR buffer 190 to accumulate the results of the XOR operation.” Ex.1006, 3:49-56. The XOR element 180 “copies the data being transferred and adds it (by performing an XOR operation) to the accumulated parity information in the associated XOR accumulator buffer.” Ex.1006, 3:57-67. Accordingly, because the XOR buffer stores the updated parity block throughout the stripe operation, it is a “*context memory*” as claimed.

Second, Kleiman’s XOR buffer 190 “*context memory*” includes at least one XOR accumulator buffer (“*page frame*”). Kleiman explains that “[t]he XOR buffer 190 includes a random access memory (RAM) 340, which provides a set of 32 XOR accumulator buffers, each of which is 1024 entries long by 4 bytes (32 bits) wide, thus 4K bytes in size.” Ex.1006, 5:33-36.

Kleiman’s XOR accumulator buffers, as they would have been implemented within Jeddeloh’s system would have been sized to store a memory page. Jeddeloh performs its operations on pages by writing different pages to different memory devices. *See* Ex.1005, [0040]. Accordingly, Jeddeloh’s RAID circuit, implemented according to Kleiman’s technique, would include a XOR accumulator buffer sized for a page. A POSITA would have recognized that a XOR accumulator buffer

sized for a page is a “*page frame*” as claimed. See *e.g.*, Ex.1011, 789 (“page frame ... A block of main storage having the size of, and used to hold, a page ... An area of main storage used to hold a page.”) Accordingly, Jeddeloh’s system as implemented with Kleiman’s on-the-fly technique would use a XOR accumulator with enough memory space to hold a page and would thus include a “*page frame*” as claimed.

Thus, because Jeddeloh describes RAID XOR circuitry, and a POSITA would have found it obvious for the RAID XOR circuitry to include a XOR buffer with XOR accumulators, Jeddeloh and Kleiman render this limitation obvious.

¶¶118-25

[1.6] *the parity calculator configured to receive the plurality of data blocks as a sequence of data blocks,*

First, as explained above at [1.4], Jeddeloh describes that “RAID XOR circuitry 226 can calculate parity data based on data received from the host interface circuitry 214.” Ex.1005, [0027].

Second, when using Kleiman’s on-the-fly technique, the data being received from the host interface circuitry is received in sequence. “The timing and control element 320 sequences each word in the FIFO queue 350 ... through the XOR operator 354, so as to perform an XOR operation on data in the associated XOR accumulator buffer in the RAM 340 with data in the FIFO queue 350.” Ex.1006,

7:26-32. “The XOR buffer 190 also includes a FIFO queue 350, which provides for inputting sequential words of bus data values and performing the XOR operation on those **sequential words**.” Ex.1006, 5:39-44. Accordingly, it would have been obvious for Jeddeloh’s RAID XOR circuitry, as it implements Kleiman’s on-the-fly technique, to receive pages (“*plurality of data blocks*”) in sequence.

Thus, because Kleiman’s fly-by XOR element receives data in sequence, Jeddeloh and Kleiman render this limitation obvious. Ex.1003, ¶¶126-29.

[1.7] [the parity calculator configured] to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks,

First, to generate a parity block, Kleiman’s on-the-fly technique “*stor[es] a first data block of the sequence of data blocks into the page frame.*” Kleiman’s fly-by XOR element “copies the data being transferred and adds it (by performing an XOR operation) to the accumulated parity information in the **associated XOR accumulator buffer**.” Ex.1006, 3:62-64.

Kleiman also explains that before the parity block operation, the XOR accumulator is “reset to a uniform zero value.” Ex.1006, 10:47-48. Accordingly, because a bit value XORed with zero is the original bit value, the first data block stored in the XOR accumulator will simply be that first data block. Accordingly, Kleiman’s technique “*stor[es] a first data block of the sequence of data blocks into*

the page frame.” Using this technique in Jeddeloh, a first page (*“first data block”*) is stored in the XOR accumulator (*“page frame”*) of the XOR buffer.

Second, for each subsequent piece of data passing through, Kleiman’s fly-by XOR element replaces (*“updat[es]”*) the data in the XOR accumulator with an XOR of the subsequent data and the data in the XOR buffer (*“updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks”*). “As the data is transferred using the mezzanine bus 160, the fly-by XOR element 180 reads the data (without interference with the data transfer) and adds it to one of the XOR accumulators (see FIG. 2) in the XOR buffer 190.” Ex.1006, 3:7-21. “When the fly-by XOR element 180 recognizes such a transfer, it copies the data being transferred and adds it (by performing an XOR operation) to the accumulated parity information in the associated XOR accumulator buffer.” Ex.1006, 3:57-67.

This process, described by Kleiman, was a well-known process for on-the-fly parity calculation. For example, Solomon similarly describes this process. “In performing an XOR on data transfers, **the first data being passed between the host-side memory and the disk-side memory is copied into the XOR buffer 48.**” Ex.1009, 4:22-41. “In subsequent data transfers between the two memories, data words are XORed by the DMA/XOR engine with the corresponding data words in the XOR buffer 48. Each time the result of the XORing is replaced into

the XOR buffer 48.” Ex.1009, 4:22-41.

Using Kleiman’s technique in Jeddelloh, the RAID XOR circuitry 222 updates the data stored in a buffer with each subsequent page passing through. In particular, the RAID XOR circuitry XORs each passing page with the data stored in the XOR buffer and replaces the data in the XOR buffer with the result. Ex.1003, ¶34.

Thus, because it would have been obvious for Jeddelloh’s RAID XOR circuitry to use Kleiman’s on-the-fly technique to calculate parity data, and that technique updates the XOR buffer with an XOR result from each subsequent page passing through, Jeddelloh and Kleiman render this limitation obvious. Ex.1003, ¶¶130-35.

[1.8] *without storing each data block in a data buffer,*

Jeddelloh’s RAID XOR circuitry, implemented with Kleiman’s on-the-fly technique, does not have to store each data block in a buffer at the same time in order to perform the XOR calculation. Instead, it performs the XOR calculation “on-the-fly” and thus does so “*without storing each data block in a data buffer.*”

Kleiman’s technique is consistent with the on-the-fly technique described in the ’346 patent. As explained above at VIII, a POSITA would have understood that the term “*without storing each data block in a data buffer*” would be interpreted as “*without storing each data block in a data buffer at the same time.*” **“In this way,**

the parity calculator generates the parity block on the fly as the command

processing units are receiving the data blocks for the data stripe operation.”

Ex.1001, 1:61-2:3; Ex.1003, ¶137.

Thus, because it would have been obvious for Jeddeloh’s RAID XOR circuitry to utilize Kleiman’s on-the-fly technique, Jeddeloh and Kleiman render this limitation obvious. Ex.1003, ¶¶136-38.

[1.9] the command processing unit receiving the parity write command configured to write the parity block to a nonvolatile memory based on the parity write command.

Jeddeloh’s memory controller writes parity data based on the parity write command. “A page write command can be sent, e.g., queued, to the desired channel memory controller 338-1,..., 338-N and executed on the one or more solid state memory devices 310-1,..., 310-N.” Ex.1005, [0040]. “As an example, write data can be striped across seven of eight memory devices, where parity data can be stored in an eighth memory device, e.g., memory system 204 can include multiple non-volatile memory devices 210, each coupled to the memory system control circuitry 208 by a separate channel.” Ex.1005, [0028].

The parity data is written to a specific memory channel and thus processed by one of the channel memory controllers (“*command processing units*”). “At least one of the number of memory channels can be operated as a parity channel and accordingly, one or more memory devices associated with the at least one of the

number of memory channels can be operated as a parity memory device(s).”

Ex.1005, [0036]; *see also* Ex.1005, [0048].

Thus, because Jeddeloh describes using channel memory controllers to write parity data to memory, Jeddeloh renders this limitation obvious. Ex.1003, ¶¶139-41.

7. Claim 2

[2.1] *The nonvolatile memory controller of claim 1, wherein the parity calculator is further configured to update the data block stored in the page frame by performing a logical operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks.*

As explained above at [1.7], Jeddeloh’s RAID XOR circuitry, utilizing Kleiman’s on-the-fly technique, updates the parity block by performing an XOR operation on the data stored in the XOR buffer and a subsequent data block passing through. The XOR function is a “*logical operation*.” The “XOR operation” described by Kleiman is a Boolean logical operation that returns a “1” if the two bit values are different and a “0” if both bit values are the same. *See e.g.*, Ex.1011, 403.

Thus, because Kleiman’s on-the-fly technique uses a XOR operation, which is a Boolean logical operation, Jeddeloh and Kleiman render this limitation obvious. Ex.1003, ¶¶142-43.

8. Claim 3

[3.1] *The nonvolatile memory controller of claim 2, wherein the logical operation includes an exclusive-or operation.*

As explained above at [1.7] and [2.1], Kleiman’s on-the-fly technique utilizes an XOR (exclusive-OR) operation. Thus, Jeddeloh and Kleiman render this limitation obvious. Ex.1003, ¶144.

9. Claim 5

[5.1] *The nonvolatile memory controller of claim 1, wherein the nonvolatile memory controller further comprises a command distribution unit configured to distribute the plurality of data update commands to command processing units of the plurality of command processing units,*

First, Jeddeloh’s memory control circuitry 208 includes host memory translation circuitry 216 (“*command distribution unit*”) that distributes commands to the channel memory controllers 338 of the non-volatile memory control circuitry 222. “The host-memory translation circuitry 216 might, for example, convert host sector read and write operations to commands directed to specific portions of the non-volatile memory 210.” Ex.1005, [0027].

As explained above at [1.1], different portions of memory (i.e., different channels) are managed by different memory channel control circuits 338 (“*command processing units*”). Thus, by translating commands and directing them to specific portions of memory and thus the memory channel control circuits associated therewith, the host-memory translation circuitry “*distribute[s] the*

plurality of data update commands to command processing units of the plurality of command processing units.”

Additionally, the non-volatile memory control circuitry 222/322 distributes commands across the different memory channels. “The non-volatile memory control circuitry 222 can be configured to write data in a first stripe across a number of memory channels as described herein.” Ex.1005, [0036]. “At least one of the number of memory channels can be operated as a parity channel and accordingly, one or more memory devices associated with the at least one of the number of memory channels can be operated as a parity memory device(s).” Ex.1005, [0036].

Again, as explained above at [1.1], each of the memory channels is controlled by memory channel control circuits 338. Thus, by sending commands to the different memory channels and thus the memory channel control circuits associated therewith, the host translation circuitry 216 “*distribute[s] the plurality of data update commands to command processing units of the plurality of command processing units.”*

Thus, because the host-memory translation circuitry 216 distributes commands to different memory channel controllers, Jeddeloh renders this limitation obvious. Ex.1003, ¶¶145-49.

[5.2] [the command distribution unit configured to] determine generation of the

parity block is complete, and distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete.

First, as explained above at [1.4], the host-memory translation circuit includes RAID XOR circuitry 226. The RAID XOR circuitry—implemented with Kleiman’s on-the-fly technique—determines that the parity block is complete. Kleiman explains that the system updates the XOR accumulator with each passing data block. Then, when the last of the data blocks has been XORed, the contents of the XOR buffer are written to memory as the parity data. “When all data for the recognized memory buffer has been transferred, the associated XOR accumulator buffer holds the computed parity for the RAID stripe.” Ex.1006, 3:65-67. Then, “the processor 110 directs the fly-by XOR element 180 to readout the accumulated parity information from the associated XOR accumulator buffer, either to a memory buffer in the memory 110 or to a storage block on one of the disk drives 140.” Ex.1006, 4:1-11.

Second, as explained above at [5.1], the host-memory translation circuitry 222 directs commands—including the parity write command—to the channel memory control circuits 338.

Third, as explained above at [1.9], the parity write command is sent to the appropriate channel memory after it is complete.

Thus, because Jeddeloh includes translation circuitry that distributes write

and parity commands to the channel memory controllers, and the RAID XOR circuitry implemented according to Kleiman's technique distributes the parity block once complete, Jeddeloh and Kleiman render this limitation obvious. Ex.1003, ¶¶150-53.

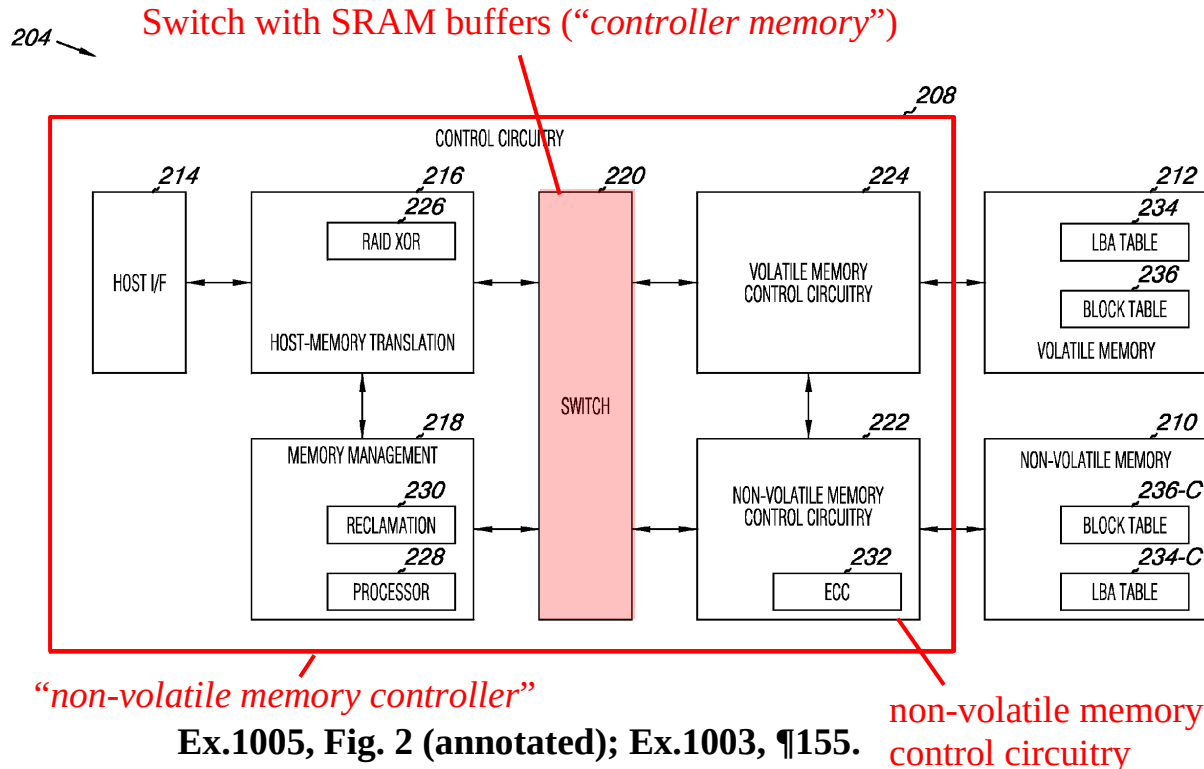
10. Claim 6

[6.0] *The nonvolatile memory controller of claim 1, further comprising.*

See Claim 1. Ex.1003, ¶154.

[6.1] *a controller memory configured to store the plurality of data blocks; and*

First, Jeddeloh's memory controller includes a switch 220 with SRAM buffers ("*controller memory*"). "The switch 220 can be a cross bar switch and can include and/or be coupled to one or more buffers, e.g., static random access memory (SRAM) buffers." Ex.1005, [0033].



Second, because the memory pages (“data blocks”) pass through the switch 220 on their way from the host to the memory devices, the switch is configured to store the memory pages in the switch’s SRAM buffers, for example. Indeed, Ma, which provides more details as to a DMA switch’s operation. Ma explains that data blocks being passed to the memory control circuitry are stored in the switch’s buffers: “Host 10 responds with the data-out packet with the write data, DATA-1, which is stored in the SDRAM buffer of smart storage switch 30.” Ex.1007, 12:44-49. Accordingly, it would have been obvious for Jeddeloh’s switch 220 to similarly buffer incoming write data (“data blocks”) in its SRAM buffers.

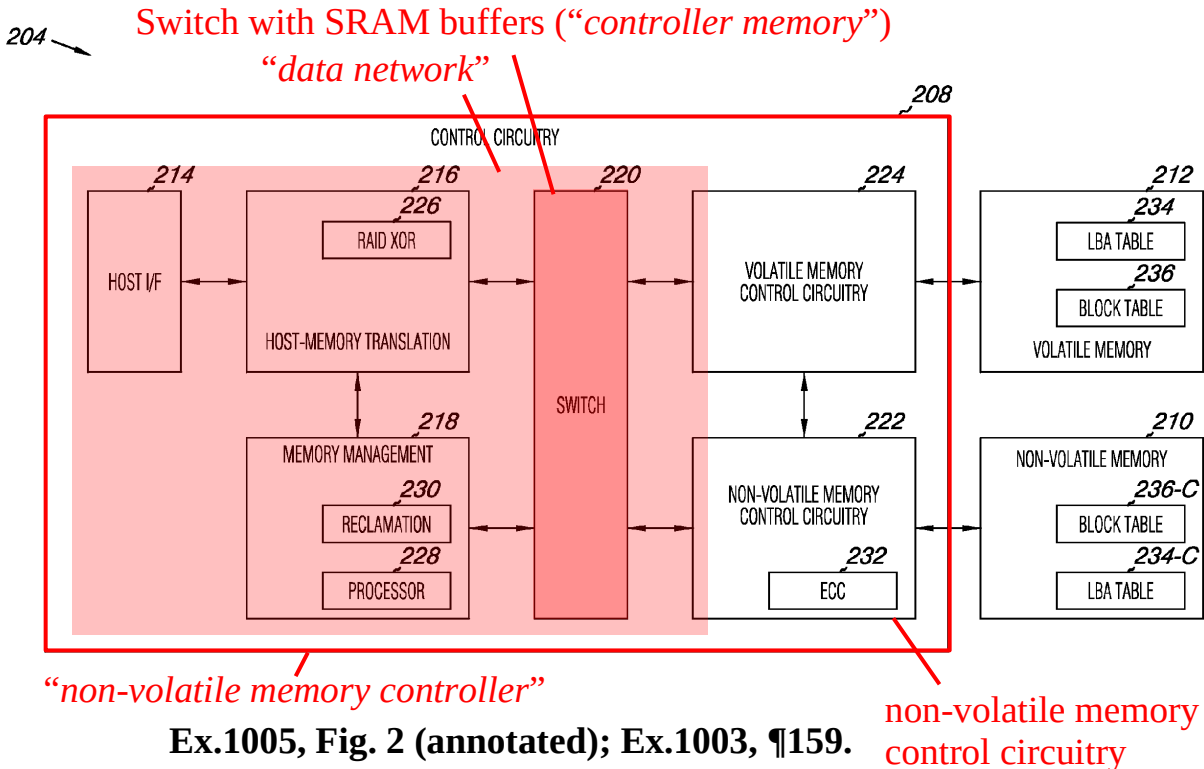
Thus, because page write operation data (“the plurality of data blocks”) pass

through the buffers of the switch 220 from the host translation circuitry to the non-volatile memory control circuitry 222, Jeddeloh renders this limitation obvious.

Ex.1003, ¶¶155-58.

[6.2] *a data network coupled to the controller memory, the plurality of command processing units, and the parity calculator,*

First, Jeddeloh’s memory controller includes a “*data network*” that connects the various components such as the host interface 214, host memory translation circuitry 216, switch 220, and non-volatile memory control circuitry 222, as illustrated in Fig. 2 below. “The switch 220 can be coupled to the host-memory translation circuitry 216, the memory management circuitry 218, the non-volatile control circuitry 222, and/or the volatile memory control circuitry 224.” Ex.1005, [0033].



Second, the network is connected to the switch 220 that includes SRAM buffers (“controller memory”). “The switch 220 can be a crossbar switch and can include and/or be coupled to one or more buffers, e.g., static random access memory (SRAM) buffers.” Ex.1005, [0033]. Accordingly, the “data network [is] coupled to the controller memory.”

Third, the network is connected to the channel memory control circuits 338 (“the plurality of command processing units”) of the non-volatile memory control circuitry (222). “The non-volatile memory control circuitry 222, e.g., controller, can be coupled to the switch 220 and to one or more non-volatile memory devices 210.” Ex.1005, [0034]. Accordingly, the “data network [is] coupled to ... the

plurality of command processing units” as claimed.

Fourth, the network is connected to the Raid XOR circuitry 226 (“*parity calculator*”) of the host-memory translation circuitry 216. “The switch 220 can be coupled to the host-memory translation circuitry 216.” Ex.1005, [0033].

According, the “*data network [is] coupled to the ... parity calculator*” as claimed.

Thus, because Jeddeloh’s memory controller includes a switch 220 with (or coupled to) SRAM buffers, host translation circuitry 222, and non-volatile memory circuitry 222 all interconnected together, Jeddeloh renders this limitation obvious. Ex.1003, ¶¶159-63.

[6.3] wherein the plurality of command processing units is further configured to request the plurality of data blocks by generating a plurality of data request packets,

First, as described above at [1.3a] and [1.3b], each of the channel memory controllers 338 (“*plurality of command processing units*”) requests the data from the host using, for example, a “DMA activate” request as evidenced by Ma. Accordingly, because a plurality of channel memory controllers send such requests, there are a plurality of data requests.

Second, a POSITA would have understood that the requests are “*request packets*” as claimed. For example, Ma describes a DMA activate request as a “DMA activate packet” that requests the write data from the host: “Smart storage switch 30 generates **a DMA activate packet** back to host 10. Host 10 responds

with the data-out packet with the write data, DATA-1, which is stored in the SDRAM buffer of smart storage switch 30.” Ex.1007, 12:43-46.

Thus, because Jeddeloh’s channel memory circuits—implementing Ma’s DMA technique—send out DMA activate packets to request write data, Jeddeloh and Ma render this limitation obvious. Ex.1003, ¶¶164-66.

[6.4] *the controller memory is further configured to generate a plurality of completion packets including the plurality of data blocks, and*

First, as described above at [6.1], Jeddeloh’s memory controller includes a switch 220 with SRAM buffers (“*controller memory*”). Jeddeloh further explains that “the switch 220 can be a direct memory access (DMA) module.” Ex.1005, [0033].

Second, when performing DMA operations (described in more detail by Ma), the switch 220 (“*controller memory*”) would transmit the data to be written in a data-out packet (“*completion packets*”). “Next host 10 sends one or more data-out packets to smart storage switch 30, which takes the data and forms one or more **data-out packets** to send to endpoint-1 [e.g., Jeddeloh’s channel control circuits 338].” Ex.1007, 11:45-50. Ma’s data-out packets are “*completion packets*” as claimed. In particular, the data-out packets include the “data to write to flash memory blocks” (“*including the plurality of data blocks*”).

Thus, because Jeddeloh’s switch, when implementing Ma’s DMA technique,

generates data-out packets with the data to be written to memory, Jeddeloh and Ma render this limitation obvious. Ex.1003, ¶¶167-70.

[6.5] both the parity calculator and the plurality of command processing units are further configured to receive the plurality of data blocks through the data network.

First, as described above at [6.2], Jeddeloh’s data network connects the switch 220 to the host-memory translation circuitry 216 (which includes the RAID XOR circuitry (“*parity calculator*”)) and the channel memory controllers (“*plurality of command processing units*”).

Second, the RAID XOR circuitry 226 (“*parity calculator*”) receives the memory pages to be written to memory from the host interface 214 over the data network. “The host-memory translation circuitry 216 can be coupled to the host interface circuitry 214, to the memory management circuitry 218, and/or to the switch 220.” Ex.1005, [0027]. “The host-memory translation circuitry 216 can include ... RAID exclusive or (XOR) circuitry 226. The RAID XOR circuitry 226 can calculate parity data based on data received from the host interface circuitry 214.” Ex.1005, [0027]. Accordingly, because the RAID XOR circuitry receives data to be written to memory from the host interface, the RAID XOR circuitry is “*configured to receive the plurality of data blocks through the data network.*”

Second, as explained above at [1.3b] the channel memory controllers 338 receive the write data from the host. As explained at [6.1] and [6.2], the channel

memory controllers are connected to the host over a data network between the channel memory controllers and the host interface. Accordingly, the channel memory controllers are “*configured to receive the plurality of data blocks through the data network.*”

Thus, because Jeddeloh’s RAID XOR circuitry and channel memory controllers receive write data over interconnections to the host interface, Jeddeloh renders this limitation obvious. Ex.1003, ¶¶171-75.

11. Claim 7

[7.1] *The nonvolatile memory controller of claim 6, wherein the nonvolatile memory controller further comprises a command distribution unit configured to distribute the plurality of data update commands to command processing units of the plurality of command processing units,*

See [5.1]. Ex.1003, ¶176.

[7.2] *determine generation of the parity block is complete, and distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete.*

See [5.2]. Ex.1003, ¶177.

12. Claim 8

[8.1] *The nonvolatile memory controller of claim 7, wherein each command processing unit of the plurality of command processing units comprises a command processing unit command queue for storing commands distributed to the command processing unit from the command distribution unit.*

Jeddeloh explains that each of the channel memory control circuits (“*command processing units*”) are capable of queuing commands. “A page write

command can be sent, e.g., queued, to the desired channel memory controller 338-1, . . . , 338-N and executed on the one or more solid state memory devices 310-1, . . . , 310-N.” Ex.1005, [0040].

Thus, because Jeddeloh’s channel memory controllers queue received commands, Jeddeloh renders this limitation obvious. Ex.1003, ¶¶178-79.

13. Claim 9

[9.1] *The nonvolatile memory controller of claim 7, further comprising a context memory including a plurality of page frames, wherein each command of the plurality of commands includes a flow identifier, and the command distribution unit is further configured to allocate a page frame of the context memory to the data stripe operation by associating the flow identifier with the page frame.*

First, for the reasons explained above at [1.5], Kleiman describes a XOR buffer (“*context memory*”) that includes a plurality of XOR accumulators (“*plurality of page frames*”).

Second, Kleiman’s fly-by XOR element allocates certain XOR accumulators to certain stripe operations using 20-bits of a bus address value associated with an address in host memory 120 (“*the command distribution unit is further configured to allocate a page frame of the context memory to the data stripe operation by associating the flow identifier with the page frame*”). “To allocate an XOR accumulator buffer for a new RAID stripe ... the timing and control element 320 causes the CAM 330 to be loaded with a 20-bit memory address for a memory buffer in the memory 120 ... and associates that 20-bit memory address with a 5-bit

identifier for one of the 32 XOR accumulator buffers.” Ex.1006, 6:36-55. In other words, Kleiman uses the 20-bits of the memory address where data for the data stripe operation is stored in host memory 120 as an identifier for that data stripe. That memory address is then used to allocate an XOR buffer (“*page frame*”) to the data stripe operation.

As the data commands pass through the bus, Kleiman’s technique looks at 20-bits of the bus address to determine which XOR accumulator should be used. Kleiman’s “processor 110 allocates a memory buffer in the memory 120, and sets up data to be DMA transferred to or from the memory buffer and one of the disk drives 140.” Ex.1006, 3:45-48. “At a step 223, the DMA transfer is performed. The fly-by XOR element 180 monitors the mezzanine bus 160 and attempts to recognize transfers to or from the memory buffer.” Ex.1006, 3:57-59. “To monitor the mezzanine bus 160 as in the step 223, the timing and control element 320 selects the bus address path 312 for coupling to the tag port 332.” Ex.1006, 6:56-64. “When the high-order 20 bits of a memory address (or an address within a null memory buffer) appearing on the mezzanine bus 160 matches one of the 20-bit tags in the CAM 330, the CAM 330 matches bits 12 through 31 of the bus address and associates a 5-bit value with that 20-bit tag.” Ex.1006, 6:56-64

Then, “[t]he associated 5-bit value is used to select one of the 32 XOR accumulator buffers in the RAM 340.” Ex.1006, 6:65-66. Accordingly, as the write

commands pass through the data bus, the associated bus address is used as a “*flow identifier*” (“*wherein each command of the plurality of commands includes a flow identifier*”).

As explained above at X.C.3, it would have been obvious for Jeddeloh’s RAID XOR circuitry 226 of the host-memory translation circuit (“*command distribution unit*”) to be implemented according to Kleiman’s on-the-fly technique. In doing so, the RAID XOR circuitry 226 of the host-memory translation circuit (“*command distribution unit*”) would use 20 bits of the bus address (“*flow identifier*”) to associate the command of the data stripe operation with a specific XOR accumulator (“*page frame of the context memory*”).

Thus, Jeddeloh’ RAID XOR circuitry—as implemented using Kleiman’s technique uses 20 bits of a bus address to associate write commands with a particular XOR accumulator, Jeddeloh and Kleiman render this limitation obvious. Ex.1003, ¶180-86.

14. Claim 10

[10.1] *The nonvolatile memory controller of claim 1, wherein the plurality of command processing units is further configured to perform a plurality of data stripe operations in parallel.*

Jeddeloh explains that data stripe operations are performed “simultaneously” (“*in parallel*”). “In one or more embodiments, the plurality of page write operations in the stripe write operation can be performed substantially

simultaneously across the plurality of channels.” Ex.1005, [0040]. Additionally, in Kleiman’s on-the-fly technique, “up to 32 different RAID stripes can have XOR accumulation performed simultaneously by the fly-by XOR element 180.” Ex.1006, 5:32-37.

Thus, because Jeddeloh’s channel control circuits perform page write operations substantially simultaneously, and Kleiman’s on-the-fly-technique performs several stripe operations in parallel, Jeddeloh and Kleiman render this limitation obvious. Ex.1003, ¶¶187-89.

15. Claim 11

[11.0] A *nonvolatile memory controller* comprising:

For the reasons explained at [1.0], the prior art teaches a “*non-volatile memory controller*” as claimed. Ex.1003, ¶190.

[11.1] *a command distribution unit configured to receive a plurality of commands for performing a data stripe operation on a plurality of data blocks, the plurality of commands comprising a plurality of data update commands and a parity write command;*

First, for the reasons explained above at [5.1], Jeddeloh’s device includes host-memory translation circuitry that distributes page write commands of a stripe operation to the channel memory controllers 338. The channel memory controllers receive the plurality of commands for the stripe operations as discussed above at [1.1]. Thus, Jeddeloh teaches a “*command distribution unit configured to receive a*

plurality of commands for performing a data stripe operation on a plurality of data blocks” as claimed.

Second, as explained above at [1.2], the plurality of commands include “a plurality of data update commands and a parity write command.” Ex.1003, ¶¶191-92.

[11.2] a plurality of command processing units coupled to the command distribution unit,

First, for the reasons explained above at [1.1] Jeddeloh includes a plurality of channel memory controllers 338 (“a plurality of command processing units”).

Second, for the reasons explained above at [5.1], Jeddeloh includes a host-memory translation circuitry 216 (“command distribution unit”).

Third, as shown in Jeddeloh’s Fig. 1, the channel memory controllers 338 are coupled to the command distribution unit through the switch.

Thus, because Jeddeloh includes a plurality of channel memory controllers coupled to the host translation circuitry, Jeddeloh renders this limitation obvious. Ex.1003, ¶¶193-96.

[11.3] the command distribution unit further configured to distribute the plurality of data update commands among command processing units of the plurality of command processing units,

See [1.0]. Ex.1003, ¶197.

[11.4] each command processing unit receiving a data update command configured to request a data block of the plurality of data blocks based on the

data update command, receive the data block in response to the request, and write the data block to a nonvolatile memory device; and

For the reasons explained above at [1.3a] and [1.3b], Jeddeloh and Ma render this limitation obvious. Ex.1003, ¶198.

[11.5] *a parity calculator coupled to the plurality of command processing units,*

See [1.4]. Ex.1003, ¶199.

[11.6] *the parity calculator including a context memory including a page frame,*

See [1.5]. Ex.1003, ¶200.

[11.7] *the parity calculator configured to receive the data blocks of the plurality of data blocks as a sequence of data blocks,*

See [1.6]. Ex.1003, ¶201.

[11.8] *[the parity calculator configured] to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame by performing an exclusive-or operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks,*

First, for the reasons explained above at [1.7], Jeddeloh teaches “[*the parity calculator configured] to generate a parity block by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame.*”

Second, for the reasons explained at [1.7], [2.1] and [3.1], updating the block in the page frame is done “*by performing an exclusive-or operation on the data block stored in the page frame and a data block following the first data block*

in the sequence of data blocks.” Ex.1003, ¶202-03.

[11.9] the command distribution unit further configured to determine generation of the parity block is complete and to distribute the parity write command to a command processing unit of the plurality of command processing units in response to determining the parity block is complete,

See [5.1]. Ex.1003, ¶204.

[11.10] the command processing unit receiving the parity write command configured to write the parity block into the nonvolatile memory device.

See [1.9]. Ex.1003, ¶205.

16. Claim 13

[13.1] The nonvolatile memory controller of claim 12, wherein the context memory includes a plurality of page frames for storing a plurality of parity blocks of a plurality of data stripe operations, and wherein the plurality of command processing units is further configured to perform the plurality of data stripe operations in parallel.

See [9.1]. Ex.1003, ¶206.

17. Claim 14

[14.0] A method of generating parity data, the method comprising:

Jeddeloh describes a method for generating parity data during a data stripe operation. “The present disclosure includes methods and devices for stripe-based memory operation. One method embodiment includes writing data in a first stripe across a storage volume of a plurality of memory devices.” Ex.1005, [0012]. The data stripe operation uses “RAID XOR circuitry 226 [to] calculate parity databased on data received from the host interface circuitry 214.” Ex.1005, [0027]; Ex.1003,

¶207.

[14.1] *distributing a plurality of commands for performing the data stripe operation among a plurality of command processing units in the nonvolatile memory controller, the plurality of commands including a plurality of data update commands and a parity write command;*

For the reasons explained above at [1.1], Jeddeloh renders this limitation obvious. Ex.1003, ¶208.

[14.2] *generating a plurality of data requests by the plurality of command processing units based on the plurality of data update commands;*

For the reasons explained above at [1.3a], Jeddeloh and Ma render this limitation obvious. Ex.1003, ¶209.

[14.3] *receiving a plurality of data blocks at the plurality of command processing units and at a parity calculator of the nonvolatile memory controller in response to the plurality of data requests;*

First, for the reasons explained above at [1.3b], Jeddeloh and Ma render obvious “*receiving a plurality of data blocks at the plurality of command processing units ... in response to the plurality of data requests*” as claimed.

Second, because the data is received by the channel memory circuits 338 from the host, the data passes through the RAID XOR circuitry (“*at a parity calculator of the nonvolatile memory controller*”) as well. Ex.1003, ¶¶210-11.

[14.4] *writing the plurality of data blocks to a plurality of nonvolatile memory devices by the plurality of command processing units;*

For the reasons explained above at [1.3b], Jeddeloh and Ma render this

limitation obvious. Ex.1003, ¶212.

[14.5] *generating a parity block in a page frame of a context memory by the parity calculator based on the plurality of data blocks by initializing a parity block in the page frame by storing a first data block of the sequence of data blocks into the page frame and updating the data block stored in the page frame with each data block following the first data block in the sequence of data blocks, without storing each data block in a data buffer;*

For the reasons explained above at [1.4]-[1.8], Jeddeloh renders this limitation obvious. Ex.1003, ¶213.

[14.6] *determining that generation of the parity block is complete; and*

For the reasons explained above at [5.2], Jeddeloh renders obvious “determining that generation of the parity block is complete” as claimed. Ex.1003, ¶214.

[14.7] *writing the parity block to a nonvolatile memory device by a command processing unit of the plurality of command processing units based on the parity write command after determining generation of the parity block is complete.*

For the reasons explained above at [5.2] and [1.9], Jeddeloh renders obvious “writing the parity block to a nonvolatile memory device by a command processing unit of the plurality of command processing units based on the parity write command after determining generation of the parity block is complete” as claimed. Ex.1003, ¶215.

18. Claim 15

[15.1] *The method of claim 14, wherein ... the sequence of data blocks.*

See [2.1]. Ex.1003, ¶216.

19. Claim 16

[16.1] *The method of claim 15, wherein the operation includes an exclusive-or operation.*

See [3.1]. Ex.1003, ¶217.

20. Claim 18

[18.1] *The method of claim 14, wherein ... associating the flow identifier with the page frame.*

See [9.1]. Ex.1003, ¶218.

D. Ground 2: Claims 4 and 17 are obvious in view of Jeddeloh, Kleiman, Ma, and Yashiro.

1. Summary of Yashiro

Yashiro provides evidence that it was known to use a counter to determine whether a parity block is complete. Dr. Min provides a summary of Yashiro in his declaration. Ex.1003, ¶¶219-21

2. Reasons to Combine Yashiro with Jeddeloh, Kleiman, and Ma

A POSITA would have found it obvious to use a counter for determining that the parity block of the Jeddeloh/Kleiman combination is complete. Ex.1003, ¶222.

As explained above at X.C.2, Kleiman describes a known method in which a parity block is calculated on-the-fly. Ex.1006, title, abstract. In particular, Kleiman describes Kleiman describes a “fly-by XOR element 180” that “uses an XOR

buffer 190 for saving partial and final results of XOR operations.” Ex.1006, 3:3-5. Then, “[w]hen all data for the recognized memory buffer has been transferred, ... the processor 110 directs the fly-by XOR element 180 to readout the accumulated parity information from the associated XOR accumulator buffer ... to a storage block on one of the disk drives 140.” Ex.1006, 3:65-4:6; Ex.1003, ¶223.

A POSITA would have found it obvious to look to known techniques for determining when “all data for the recognized memory buffer has been transferred” as described by Kleiman. Ex.1006, 3:65-67; Ex.1003, ¶224. Yashiro provides one example of a known technique in which a counter is used for determining when the parity block is complete. In particular, Yashiro further describes using a counter to determine when the parity block is complete. “The counter N has been cleared to N=0 in the initial state.” Ex.1008, 14:31-32. As the system processes write commands (described in the text accompanying Fig. 12), the “count value of the count N ... is increased by 1.” Ex.1008, 14:30-31. If the counter N has not yet reached the “set [] number of [] times” (i.e., a threshold), then the method returns to processing the next write command with respect to Fig. 12. However, once the counter reaches the threshold, the parity block is complete and the parity block can be stored on the disk in Step 8. See Ex.1008, 14:28-55.

A POSITA would have been motivated to use Yashiro’s counter technique because it provides certain benefits.

- **First**, Yashiro is a tried-and-true technique for determining when the parity block is complete. Ex.1003, ¶225.
- **Second**, given that Kleiman stores the parity block upon completion, a POSITA would have found that using a counter to count data blocks would have predictably resulted in accurately determining completion. Ex.1003, ¶225.

A POSITA would have had a reasonable expectation of success because Yashiro discloses a similar operation for calculating parity data as Kleiman—an XOR operation. Ex.1003, ¶226. Kleiman uses “XOR accumulator buffers in the XOR buffer 190 to accumulate the results of the XOR operation.” Ex.1006, 3:53-55. Similarly, in Yashiro, “the exclusive OR of the data in a plurality of disk apparatuses is calculated and is set to a parity and is held into the disk apparatus for parities.” Ex.1008, 4:22-25.

Accordingly, the combination of Yashiro with Jeddeloh and Kleiman merely represents applying a known technique (Yashiro’s counter) to a known method (Kleiman’s on-the-fly technique) ready for improvement to yield predictable results (accurately determining when the parity block is complete). Ex.1003, ¶¶222-27.

3. Claim 4

[4.1] *The nonvolatile memory controller of claim 1, further comprising a context*

associated with the page frame and including a stripe count for counting each occurrence of updating the parity block, the nonvolatile memory controller further comprising a command distribution unit configured to determine the parity block is generated by determining the stripe count has reached a threshold value.

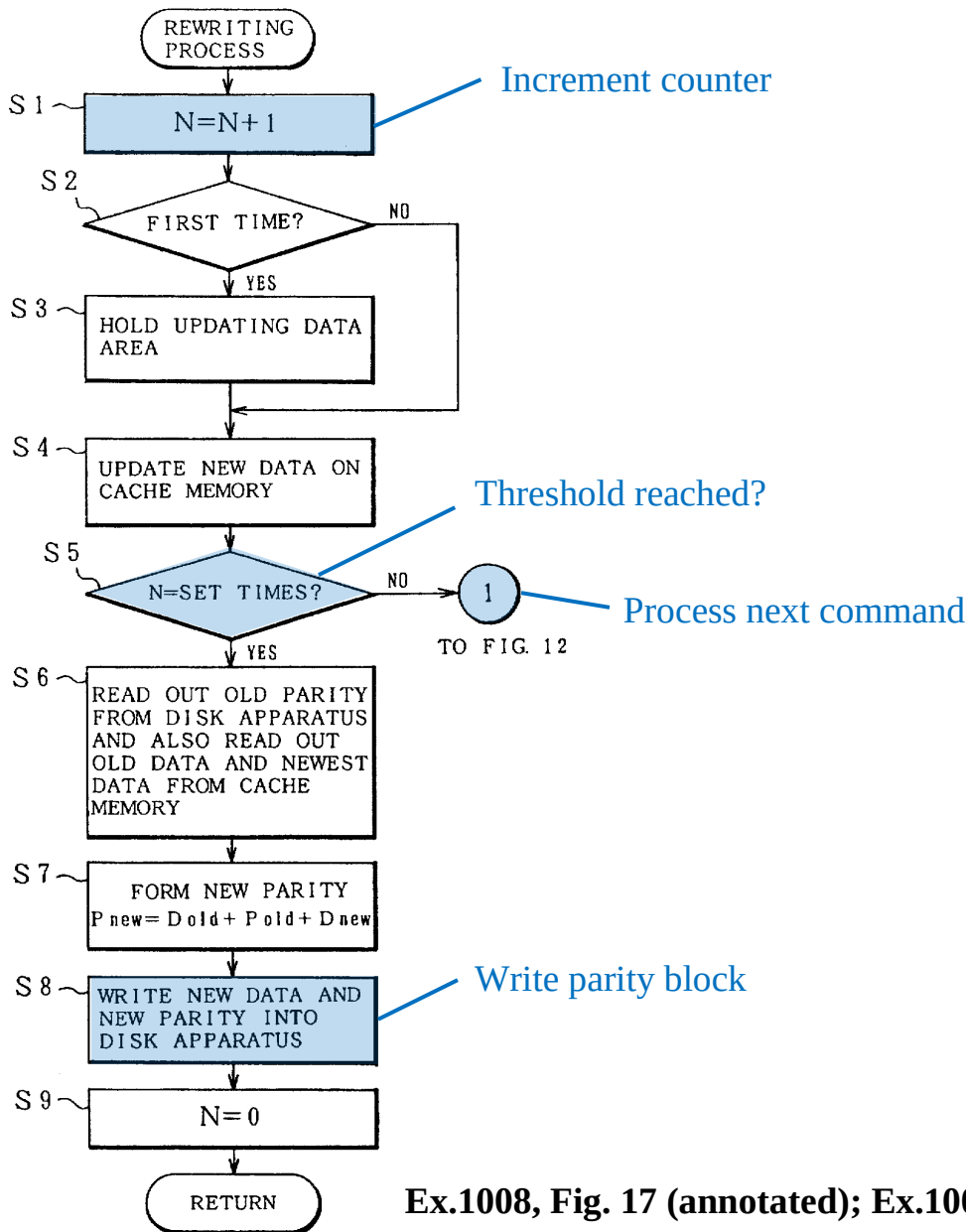
First, Jeddeloh's RAID XOR circuitry as implemented according to Kleiman's teachings maintains a context. The term "context" as used in computer science and processor/memory systems means the minimal set of data needed to complete a task. Ex.1003, ¶228. For example, the "context" may include the partial or final results in the XOR accumulator ("*page frame*") of the XOR buffer. "The fly-by XOR element 180 uses an XOR buffer 190 for saving partial and final results of XOR operations." Ex.1006, 3:3-5.

Second, it would have been obvious for Kleiman's on-the-fly XOR technique to maintain a stripe count as part of that context. Kleiman explains that the system updates the XOR buffer with each passing data sector. "Ex.1006, 3:60-64. Then, "[w]hen all data for the recognized memory buffer has been transferred ... the processor 110 directs the fly-by XOR element 180 to readout the accumulated parity information from the associated XOR accumulator buffer." Ex.1006, 3:65-4:3.

One known way to determine whether each of the sectors has passed through would be to maintain a counter. *See generally*, Ex.1008, Fig. 17. Once the counter reaches the threshold, the parity block is complete and the parity block can be

stored on the disk in Step 8. This process is illustrated below in Fig. 17. See

Ex.1008, 14:28-55.



For the reasons explained above at X.D.2. it would have been obvious for the Jeddeloh/Kleiman parity calculator to utilize a counter. In Jeddeloh's example

where there are seven data blocks and one parity block per stripe, the counter would increment to seven. When the counter reaches seven, it is determined that the parity block is complete.

Thus, because it would have been obvious for Kleiman's on-the-fly technique to utilize a counter to determine when the parity block is complete, Jeddeloh, Kleiman, and Yashiro render this limitation obvious. Ex.1003, ¶¶228-32.

4. Claim 17

[17.0] The method of claim 14, further comprising: initializing a stripe count to a predetermined value; and decrementing the stripe count in response to each occurrence of updating the parity block, wherein determining generation of the parity block is complete comprises determining the stripe count has reached a threshold value.

As explained above at [4.1], it would have been obvious to use a counter to determine when the parity block is complete. Claim 17 recites a similar concept to that of claim 4. But rather than incrementing the counter from zero to a threshold, claim 17 recites decrementing the counter from the threshold to zero. This alternative approach is merely an obvious design choice. Indeed, POSITAs understood that incrementing or decrementing in this manner were interchangeable. *See* Ex.1013, 5:9-11 (“alternatively use a decrementing counter rather than an incrementing counter, and could increment or decrement the counter by any quantity per event”).

Accordingly, in the case of Jeddeloh's system, it would have been obvious

to initialize the counter to seven, and then decrement the counter as each successive block passes through. Then, when the counter reaches zero (“*a threshold value*”) it is determined that the parity block is complete. In Jeddeloh’s example where there are seven data blocks and one parity block per stripe, the counter would be initialized to seven. When the decrementing counter reaches zero, it is determined that the parity block is complete.

Thus, because it would have been obvious for Kleiman’s on-the-fly technique to utilize a counter to determine when the parity block is complete, whether incrementing or decrementing, Jeddeloh, Kleiman, and Yashiro render this limitation obvious. Ex.1003, ¶¶233-35.

XI. DISCRETIONARY DENIAL IS NOT WARRANTED

Petitioner respectfully submits that the Board should not exercise its discretion under 35 U.S.C. §§314(a) or 325(d) to deny this Petition.

A. The Fintiv factors favor institution.

Denial would be improper based on factors in *Apple v. Fintiv*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential).

1. No evidence regarding a stay

No motion to stay has been filed, so the Board should not infer the outcome of such a motion.

2. Parallel proceeding trial date

This factor weighs against discretionary denial because no trial date has currently been scheduled. Moreover, the projected trial date—based on median time-to-trial statistics—is in January of 2027¹, which is well after the projected date for the Board to issue a Final Written Decision in July of 2026. Because the projected trial date is approximately six months *after* the Board’s expected date for issuing a Final Written Decision, this factor weighs against discretionary denial.

3. Investment in the parallel proceeding

The investment in the co-pending litigation has been minimal. No schedule has been set. Thus, the Markman hearing is unlikely to occur before the Board issues an institution decision. This lack of investment favors institution.

4. Overlapping issues with the parallel proceeding

The co-pending litigation is in its early stages. Petitioner served its preliminary invalidity contentions on December 16, 2024. However, Petitioner has not served its final invalidity contentions, nor has the deadline for doing so been set. The extent of overlap is thus speculative at this point in time.

¹ The current average time-to-trial for the district court hearing the co-pending litigation is 29.1 months. *See* Ex.1015 and Ex.1016.

5. Petitioner is a defendant

Petitioner is a defendant in the co-pending litigation. That is true of most Petitioners in IPR proceedings, making this factor neutral.

6. Other circumstances

“[T]he PTAB will not deny institution of an IPR or PGR under *Fintiv* (i) when a petition presents compelling evidence of unpatentability.” Ex.1017, 9. Here, the petition—along with Dr. Min’s expert testimony—plainly shows that the ’346 patent claims no more than known concepts related to distributed processing and parity calculation on-the-fly.

B. Advanced Bionics Test Favors Institution.

Denial under 35 U.S.C. § 325(d) is not warranted because the challenges presented in this petition are neither cumulative nor redundant to the prosecution of the ’346 patent. Neither Jeddeloh, Kleiman, Ma, or Yashiro were before the patent office during examination of the ’346 patent. Accordingly, discretionary denial under 325(d) is not warranted.

XII. CONCLUSION

Petitioner has established a reasonable likelihood that the Challenged Claims are unpatentable.

IPR2025-00516 Petition
Inter Partes Review of 8,601,346

Respectfully submitted,

Dated: January 23, 2025
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XIII. MANDATORY NOTICES**A. Real Party-in-Interest**

The real parties-in-interest (“RPI”) are Sandisk Technologies, Inc. and Western Digital Technologies, Inc. (“Petitioner”).

B. Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), to the best knowledge of the Petitioner, the ’346 patent is or was involved in the following cases:

Case Heading	Number	Court	Filed	Status
<i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i>	2-24-cv-02864	CDCA	April 9, 2024	Pending
<i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i>	1-24-cv-00101	WDTX	January 30, 2024	Pending

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Please address all correspondence in this proceeding to lead and back-up counsel. Petitioner consents to service in this proceeding by email at the addresses above

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner hereby certifies, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,967. Pursuant to 37 C.F.R. § 42.24(d), this word count excludes the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: January 23, 2025

/David M. O'Dell/

David M. O'Dell
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CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105, service was made on Patent Owner as detailed below.

Date of service January 23, 2025

Manner of service FEDERAL EXPRESS

Documents served Petition for *Inter Partes* Review Under 35 U.S.C. § 312 and 37 C.F.R. § 42.104 of U.S. 8,601,346; Petitioner's Power of Attorney; Petitioner's Exhibit List; All Exhibits.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND
WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioners

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner

Case IPR2025-00516
U.S. Patent No. 8,601,346

**PATENT OWNER POLARIS POWERLED TECHNOLOGIES, LLC'S
BRIEF ON DISCRETIONARY DENIAL**

Mail Stop "PATENT BOARD"
Patent Trial and Appeal Board
U.S. Patent and Trademark Office
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Alexandria, VA 22313-1450

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Case IPR2025-00516
U.S. Patent No. 8,601,346**PATENT OWNER'S EXHIBIT LIST**

Exhibit No.	Description
2001	List of Docket Entries, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 1-24-cv-00101 (W.D. Tex.)
2002	List of Docket Entries, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal)
2003	List of Docket Entries, <i>Micron Technology Inc. et al. v. Polaris PowerLED Techs., LLC</i> , 1-25-cv-00073 (D. Idaho)
2004	Scheduling and Case Management Order, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Jan. 27, 2025), ECF No. 54
2005	Western Digital's Notice of Motion and Motion to Stay Action Pending <i>Inter Partes</i> Review, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Feb. 3, 2025), ECF No. 58
2006	Minute Order, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Feb 3, 2025), ECF No. 59
2007	Plaintiff's Opposition to Motion to Stay, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Feb. 10, 2025), ECF No. 60
2008	Patent L.R. 3-3 and 3-4 Invalidity Disclosures of Western Digital Defendants, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal), ECF No. 60-3 and Appendices A-C of the Invalidity Disclosures
2009	Defendants' Identification of Claim Terms for Construction, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal), ECF No. 60-4
2010	Stipulated Protective Order, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal), ECF No. 61

Case IPR2025-00516
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Exhibit No.	Description
2011	Western Digital's Reply in Support of Motion to Stay Action Pending <i>Inter Partes</i> Review, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Feb. 14, 2025), ECF No. 62
2012	USPTO Appeal Statistics (Mar. 31, 2025), <i>available at</i> https://www.uspto.gov/patents/ptab/statistics
2013	Patent Trial & Appeal Board (PTAB) Dashboard, <i>available at</i> https://www.uspto.gov/dashboard/ptab/
2014	Press Release: SanDisk Celebrates Nasdaq Listing After Completing Separation from Western Digital (Feb. 24, 2025), <i>available at</i> https://shop.sandisk.com/company/newsroom/press-releases/2025/sandisk-celebrates-nasdaq-listing-after-completing-separation
2015	Defendants' Identification of Claim Terms for Construction (Apr. 18, 2025), <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal. Feb. 10, 2025)

I. INTRODUCTION

The Board should exercise its discretion under 35 U.S.C. § 314(a) and *Fintiv* to deny institution of this *inter partes* review (IPR) because the same parties are in advanced stages of litigating the validity of this patent in district court. The district court trial is scheduled for June 16, 2026—more than two months *before* the Board’s projected deadline for issuing a final written decision. Litigating the same issues at the Board would therefore be duplicative and contrary to the intent of IPRs for “providing a more efficient system for challenging patents” and “reducing unwarranted litigation costs.” H.R. Rep. No. 112-98 at 39-40 (2011); *see also NHK Spring Co. Ltd. v. Intrix-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 19-20 (P.T.A.B. Sept. 12, 2018) (precedential).

Other considerations also strongly favor discretionary denial. For example, Petitioners have not agreed to a *Sotera* stipulation or identified any reason why instituting an IPR would reduce the number of issues litigated in district court. Since the district court trial is already scheduled and instituting an IPR would not improve judicial efficiencies, the Board should deny institution and focus its limited resources on other pending cases at the Board.

II. THE BOARD SHOULD DENY INSTITUTION UNDER § 314(a).

A. The *Fintiv* factors favor discretionary denial.

When the patent owner raises an argument for discretionary denial due to an earlier trial date in a co-pending litigation, the Board weighs the following factors:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Apple Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 at 5-6 (P.T.A.B. Mar. 20, 2020) (precedential) ("*Fintiv*"). These factors, when considered as a whole, support *denying* institution. Factor 1 is neutral, factors 2-6 all weigh in favor of denial, and no factor weighs against exercising the Board's discretion to deny institution.

1. Factor 1 is, at worst, neutral because there is no evidence a stay order will be granted in the district court.

Under the first factor, if the district court stays the case or provides guidance that it will stay the case and await the Board's final resolution of the patentability issues, this fact usually weighs against exercising authority to deny institution. *Fintiv*, 7. However, here, the district court has not provided such guidance and issued a scheduling order to continue through trial. EX2004.

Actions in the district court indicate that a stay is *not* imminent because the case is moving faster than initially scheduled. On January 27, 2025, the district

court issued its scheduling and case management order, which set the deadlines to file infringement contentions and invalidity contentions as February 18, 2025, and April 4, 2025, respectively. EX2004, 26. After Western Digital filed a motion to stay the case (EX2005), the parties decided to advance the case by jointly stipulating to serve, before they were due, amended infringement and invalidity contentions. EX2006.

The amended infringement and invalidity contentions were served early to resolve a discovery dispute over the scope of accused products. Polaris's initial infringement contentions, served in October 2024, accused all Western Digital and SanDisk solid-state drive products from 2018 onward supporting NVMe, among other features, and included a list of exemplar product lines. Western Digital challenged the sufficiency of these contentions, arguing they lacked adequate detail for products beyond WD Black-branded SSDs, and consequently limited its discovery production to only those SSDs. To break this impasse and advance discovery on the full scope of accused products, Polaris prepared and sent proposed amended infringement contentions to Western Digital. These amended contentions included significantly expanded claim charts, reflecting a substantial increase in detail about exemplary SSD product lines. Polaris maintained that its initial contentions were sufficient and compliant with applicable rules, and the amended contentions were offered to address Western Digital's concerns and

resolve the dispute amicably. Western Digital acknowledged that the proposed amended contentions addressed its concerns about detail but conditioned its agreement to Polaris' service of these contentions on Polaris allowing Western Digital to serve amended invalidity contentions. Western Digital claimed its December 2024 invalidity contentions inadvertently omitted certain details and sought to amend them. After negotiations, the parties reached an agreement and submitted a stipulation to the Court on February 3, 2025. That same day, the Court approved the stipulation, permitting both Polaris' amended infringement contentions and Western Digital's amended invalidity contentions. As ordered, the parties exchanged the amended infringement and invalidity contentions early.

The parties also exchanged proposed terms for construction earlier than required. EX2002 (deadline for exchange April 18, 2025); EX2009 (identification of claim terms served on January 24, 2025). Such proactive measures show that the district court case is advancing according to schedule (if not faster).

Western Digital's motion to stay the district court case (EX2005) is still pending, but there is no indication that the court will grant the motion. In fact, the district court canceled the hearing on the motion. EX2002, ECF No. 63. And the court has denied motions to stay in cases—like this one—where the defendant waited almost a year after it was served with a complaint to file an IPR petition. Order Denying Defendant Skechers U.S.A., Inc.'s Motion to Stay Pending *Inter*

Partes Review at 2, *Nike, Inc. v. Skechers U.S.A., Inc.*, 2-19-cv-9230 (C.D. Cal Dec. 30, 2020), ECF No. 82 (“Defendant waited almost a year after it was served with the Complaint to file its IPR petitions. Defendants’ delay in filing its IPR petitions also weighs against granting a stay.”) (citation omitted); Order Denying Defendant’s Motion to Stay at 5, *Jiaying Super Lighting Elec. Appliance Co., Ltd. et al. v. MaxLite, Inc.*, 2-19-cv-4047 (C.D. Cal June 17, 2020), ECF No. 73 (“Such a delay cuts against granting a stay because ‘courts expect accused infringers to evaluate whether to file, and then to file, IPR petitions as soon as possible after learning that a patent may be asserted against them.’”) (citation omitted).

Regardless of Western Digital’s arguments in favor of a stay (EX2005, EX2011), there is no specific evidence that the district court will stay the case. “In the absence of specific evidence, [the Board] will not attempt to predict how the district court in the related district court litigation will proceed because the court may determine whether or not to stay any individual case . . . based on a variety of circumstances and facts beyond [the Board’s] control and to which the Board is not privy.” *Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (P.T.A.B. June 16, 2020) (informative). The first *Fintiv* factor is therefore, at worst, neutral. *Id.*; *Fintiv*, 6-9.

2. Factor 2 favors discretionary denial because the district court’s trial date is scheduled to occur before the projected final written decision.

The second factor weighs in favor of denying institution because the district court’s scheduled trial date is before the Board’s projected statutory deadline. See *Fintiv*, 9. The district court scheduled trial for June 16, 2026. EX2004, 25. This trial date is *before* the Board’s projected final written decision. Polaris’s POPR is due May 27, 2025.¹ An institution decision is then due August 27, 2025. 35 U.S.C. § 314(b). If instituted, that timeline would make the final written decision due August 27, 2026—more than two months *after* the district court’s trial date. 35 U.S.C. § 316(a)(11). “If the court’s trial date is earlier than the projected statutory deadline, the Board generally has weighed this fact in favor of exercising authority to deny institution” *Fintiv*, 9. In *Fintiv*, a scheduled district court trial date two months before the projected final written decision—a similar timeframe—weighed in favor of discretionary denial. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 13 (P.T.A.B. May 13, 2020) (informative) (“*Fintiv II*”).

Petitioners’ statistical-based argument for a 2027 trial date is no longer

¹ The POPR is due three months after the February 26th Notice of Filing Date. 37 C.F.R. § 42.107(b). May 26th is a Federal holiday, which makes the POPR due the next business day. 37 C.F.R. § 1.7(a).

relevant. In the petition, Petitioners projected a trial date in January 2027 based on the median time-to-trial for civil cases in the Central District of California. Pet., 77 n.1 (citing EX1016). But after Petitioners filed the petition, the court scheduled trial for June 16, 2026. EX2004, 25. Nothing in the district court record indicates that the court intends to deviate from this schedule. To the contrary, the court stated that this date was “firm.” EX2004, 1.

The second *Fintiv* factor therefore weighs in favor of discretionary denial as it did in *Fintiv*. *Fintiv*, 9; *Fintiv II*, 13.

3. Factor 3 favors denial because the parties have already invested substantial resources in the parallel proceedings.

Under the third *Fintiv* factor, “[t]he Board also has considered the amount and type of work already completed in the parallel litigation by the court and the parties *at the time of the institution decision*.” *Fintiv*, 9 (emphasis added). The deadline for issuing an institution decision is August 27, 2025. *Supra* Section II.A.2. By this date, substantial work will have already been done, including final invalidity contentions, all discovery and briefing for claim construction, and the Markman hearing. This heavy investment by the parties and the district court favors denial of institution. *Fintiv*, 9-12.

Work Performed to Date:

- January 30, 2024: Polaris filed a complaint for patent infringement in the Western District of Texas. EX2001, ECF No. 1.

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- April 9, 2024: Polaris re-filed the case in the Central District of California to resolve a threatened motion to transfer. EX2002, ECF No. 1. Polaris dismissed its Western District of Texas (W.D. Tex.) case on April 5, 2024, and refiled in the Central District of California (C.D. Cal.) on April 9, 2024, at Western Digital's suggestion, to resolve a venue dispute and avoid related motion practice costs. Western Digital proposed a stipulated dismissal without prejudice for transfer to C.D. Cal. because Western Digital argued that W.D. Tex. was an improper venue.
- June 21, 2024: Polaris filed an amended complaint. EX2002, ECF No. 40. The complaint included claim charts detailing alleged infringement of claims 1–3, 5-8, 10, 11, and 14-16 of the '346 patent. *See* EX2002, ECF No. 40-6.
- October 2, 2024: Polaris served its first sets of requests for production and interrogatories. *See* EX2007, *22.
- October 2, 2024: Polaris served its initial infringement contentions and accompanying document production. *See* EX2007, *22. The initial infringement contentions again identified the asserted claims. EX2008, *3.
- June 5, 2024: Western Digital filed answers to the amended complaint. EX2002, ECF Nos. 43-45.
- November 1, 2024: Western Digital responded to requests for production. *See* EX2007, *22.
- November 22, 2024: Western Digital responded to interrogatories. *See* EX2007, *22.
- December 16, 2024: Western Digital served invalidity contentions and accompanying document production. EX2008. The contentions charted 10 references for the '346 patent, cited numerous other references, and cited product art from different companies. *Id.*, *17-20. The contentions also analyze the motivation to combine for different combinations. *Id.*, *20-26. They also provide contentions under §§ 101 and 112. *Id.*, *26-32. In total, the invalidity contentions comprise over 3,000 pages. *See* EX2007, *22.
- January 24, 2025: Western Digital identified terms for construction, including eleven terms for the '346 patent. EX2009.

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- February 4, 2025: Polaris had served amended infringement contentions that identified the asserted claims again. *See* EX2007, *22.
- February 6, 2025: Western Digital served amended invalidity contentions. *See* EX2007, *22.
- February 11, 2025: The court ordered entry of the protective order. EX2010.
- April 18, 2025: Western Digital served Defendants’ Identification of Claim Terms for Construction, which this time included four terms for the ’346 patent. EX2015, *3-4.

Additional Work To Be Completed Before the Institution Decision (EX2004, 26):

- May 9, 2025: Preliminary Claim Constructions and Extrinsic Evidence Due
- May 24, 2025: Damages Contentions Due
- June 3, 2025: Joint Claim Construction, Prehearing Statement, and Expert Reports on Claim Construction Due
- June 23, 2025: Responsive Damages Contentions Due
- July 28, 2025: Deadline to Amend Pleadings or Add Parties
- July 3, 2025: Claim Construction Discovery Cutoff
- July 18, 2025: Claim Construction Opening Briefs Due
- July 23, 2025: Damages Contentions Meeting Deadline
- August 1, 2025: Claim Construction Responsive Briefs Due
- August 8, 2025: Claim Construction Reply Briefs Due
- August 22, 2025: Markman Hearing

For the work scheduled between filing this brief and the deadline of the institution decision, the district court has stated that “[t]hese dates and requirements are firm.” EX2004, 1. Based on the level of investment and effort

already expended on claim construction and invalidity contentions in the district court, this factor weighs in favor of discretionary denial. *Fintiv II*, 14.

Under *Fintiv* factor 3, the Board also considers whether the petitioner could have filed the petition more expeditiously to avoid unnecessary investment by the parties and the court. *Fintiv*, 11. “[I]f the petitioner cannot explain the delay in filing its petition, these facts have favored denial.” *Fintiv*, 12; *Next Caller Inc. v. TRUSTID, Inc.*, IPR2019-00961, Paper 10 at 16 (P.T.A.B. Oct. 16, 2019) (weighing the petitioner’s unexplained delay in filing the petition in favor of denial and noting that had the petitioner filed the petition earlier, the PTAB proceeding may have resolved the issues before the district court).

Here, Petitioners could have filed the IPR petition well before substantial work started in the district court case. Western Digital Technologies, Inc. was first served with a complaint alleging infringement of the ’346 patent on January 30, 2024. EX2001 at ECF No. 1.² Polaris first identified the asserted claims on June

² The litigation was originally filed in the Western District of Texas on January 30, 2024, as Case No. 1:24-cv-00101, but refiled in the Central District of California on April 9, 2024. The one-year time bar for filing an IPR petition is tied to the filing of the first case. *Click-To-Call Techs., LP v. Ingenio, Inc.*, *Yellowpages.Com, LLC*, 899 F.3d 1321, 1328 n.3 (Fed. Cir. 2018) (*en banc*),

21, 2024, in its amended complaint, and then again on October 2, 2024, in its initial infringement contentions. *See* EX2002, ECF No. 40-4; EX2008, *3. So Western Digital first had notice of the asserted claims in June 2024. Rather than filing a petition in the early stages of the case after knowing the asserted claims, Petitioners waited *for about seven months* and filed the petition in the last possible week after substantial work ensued. Petitioners did not explain this lengthy delay in the Petition. This inexcusable delay makes factor 3 weigh even more in favor of denying institution. *Next Caller*, IPR2019-00961, Paper 10 at 16. It also makes a stay less likely. *Supra* Section II.A.1.

4. Factor 4 favors denial because there is substantial overlap between the IPR grounds and the invalidity contentions in the district court case.

The fourth *Fintiv* factor—overlap between issues raised in the petition and in the parallel proceeding—favors denying institution. “[I]f the petition includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding, this fact has favored denial.” *Fintiv*, 12. “Conversely, if the petition includes materially different grounds, arguments, and/or evidence than those presented in the district court, this fact has tended to weigh against exercising discretion to deny institution” *Id.*, 12-13.

vacated on other grounds.

Petitioners have relied on the same references in this IPR as the references in its invalidity contentions, showing that parallel proceedings would result in substantial overlap and duplicative work. The IPR grounds include four references: (1) U.S. Patent Application Pub. No. 2011/0078496 to Jeddeloh; (2) U.S. Patent No. 5,950,225 to Kleiman; (3) U.S. Patent No. 8,341,332 to Ma *et al.*; and (4) U.S. Patent No. 5,787,460 to Yashiro *et al.* Pet., 15-16. The top three claim charts in Western Digital’s invalidity contentions (A1, A2, and A3) rely on the same references in ground 1, as shown below. The only reference not in Western Digital’s invalidity contentions (Yashiro) is used only for claims 4 and 17, which are not asserted in district court. *See* Pet., 15-16; EX2008, *3.

Claim Charts in the Invalidity Contentions

Claim Chart	Reference
Chart A1	U.S. Patent Application Pub. No. 2011/0078496 to Jeddeloh
Chart A2	U.S. Patent No. 5,950,225 to Kleiman
Chart A3	U.S. Patent No. 8,341,332 to Ma <i>et al.</i>

Western Digital’s invalidity contentions rely on additional references (EX2008, *17-18), but “Petitioner’s assertion of additional invalidity contentions in the District Court is not relevant to the question of the degree of overlap for this factor.” *Fintiv II*, 15. “[B]ecause the identical claims are challenged based on the

same prior art in both the Petition and in the District Court, this factor weighs in favor of discretionary denial in this case.” *Id.*

Western Digital has also not submitted any stipulation limiting the art that it can present at trial, which indicates that it intends to raise the same invalidity positions in district court. *See Sand Revolution II*, IPR2019-01393, Paper 24 at 12 (“Petitioner’s stipulation, however, mitigates to some degree the concerns of duplicative efforts between the district court and the Board, as well as concerns of potentially conflicting decisions.”); *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (P.T.A.B. Dec. 1, 2020) (precedential as to II.A) (“such a broad stipulation better addresses concerns of duplicative efforts and potentially conflicting decisions in a much more substantial way.”). Even if Western Digital were to submit a stipulation, it is too late—the Board’s discretionary panels should consider stipulations only if they are filed with sufficient time for a patent owner to address the impact of the stipulation in its discretionary denial brief. *See* FAQs for Interim Process for PTAB Workload Management, FAQ14; PTAB Boardside Chat on Interim Process for PTAB Workload Management (Apr. 17, 2025) (petitioners “*must*” file a stipulation within one month of the notice of filing date for consideration). Petitioners have had ample time to file a stipulation and have chosen not to. Factor 4 weighs in favor of denial on this basis alone.

Factor 4 also weighs in favor of denial because Western Digital relies on

system prior art in its invalidity contentions, which prevents this case from being a “true alternative” to the district court proceeding. *Cf. Motorola Solutions, Inc. v. Stellar, LLC*, IPR2024-01205, Paper 19 at 3-4 (P.T.A.B. Mar. 28, 2025). In *Motorola*, the Director denied institution under 35 U.S.C. § 314(a) because “Petitioner’s invalidity arguments in the district court are more expansive and include combinations of the prior art asserted in these proceedings with unpublished system prior art” *Id.*, 4.³ Similar here, Western Digital’s invalidity contentions include combinations of the asserted art with system prior art. *See* EX2008, *18-20 (relying on system prior art from numerous companies). For example, Western Digital has alleged invalidity based on: “Micron Technology, Inc. products embodying US Patent Application Publication No. 2011/0078496 to Jeddeloh;” “Super Talent Electronics, Inc. products embodying US Patent No. 8,341,332 to Ma;” and “Network Appliance, Inc. (also known as NetApp, Inc.) products embodying US Patent No. 5,950,225 to Kleiman.”

³ In *Motorola*, the Director suggested that the petitioner’s stipulation “is not likely to moot” a combination of prior art asserted in the IPR proceeding and system prior art. *Motorola*, IPR2024-01205, Paper 19 at 4. Patent Owner takes no position whether a *Sotera* stipulation is not likely to moot such a combination of prior art. Regardless, Petitioners have not offered such stipulations here.

EX2008, *18-19. Accordingly, this IPR would not be a “true alternative” to the district court case but instead litigate the same or (at best) substantially similar invalidity grounds.

The risk of duplicative litigation is even higher here because Western Digital Corporation is not a named petitioner, RPI, or privy, and may still try to raise the identical invalidity positions in the district court case. Petitioners appear to have strategically omitted the defendant Western Digital Corporation—the parent corporation of Western Digital Technologies, Inc.⁴—from the petition to evade estoppels.⁵ When Polaris raised this issue in briefing in the district court case

⁴ If the Board determines that Western Digital Corporation is an unnamed real party in interest or privy of Petitioners, Petitioners’ gamesmanship favors denying institution. *See* 35 U.S.C. §§ 312(a)(2).

⁵ Estoppels under 35 U.S.C. § 315(e)(2) apply only to a petitioner, real party in interest, or privy of the petitioner. Western Digital Corporation is not a petitioner, and is not listed as an RPI or privy of the petitioner. So Western Digital Corporation appears to be reserving an argument that it is not estopped in district court from raising the same grounds presented in the IPR, which further demonstrates that this IPR is not a “true alternative” to litigating validity before the district court.

(EX2007, *16), Western Digital Corporation tried to cure the issue by agreeing to estoppels. EX2011, *5. But it did so conditionally, stating: “[S]hould a stay be granted, Western Digital Corporation agrees to be bound under 35 U.S.C. § 315(e)(2).” *Id.* (emphasis added). If the court does not grant a stay, Western Digital Corporation could try to litigate the same grounds in district court.

For these reasons, the fourth *Fintiv* factor weighs strongly in favor of denying institution. *Fintiv*, 12. This inefficiency and duplication of efforts is precisely what the Board’s discretionary authority is intended to prevent. *NHK Spring*, IPR2018-00752, Paper 8 at 19-20; H.R. Rep. No. 112-98 at 39-40 (2011). And the Board should not permit Western Digital Corporation’s gamesmanship.

5. Factor 5 favors denial because the parties in the IPR overlap with the parties in the district court litigation.

Under the fifth *Fintiv* factor, “[i]f a petitioner is unrelated to a defendant in an earlier court proceeding, the Board has weighed this fact against exercising discretion to deny institution” *Fintiv*, 13-14. But here, both of the Petitioners are or are related to a defendant in the co-pending litigation. Western Digital Technologies, Inc. is a defendant in the litigation. SanDisk Technologies, Inc. is a related party and real party in interest because it was owned by Western Digital as of the filing date of the petition. See EX2014 (announcing on February 24, 2025 its separation from Western Digital); Pet., 80 (“The real parties-in-interest (‘RPI’) are SanDisk Technologies, Inc. and Western Digital Technologies, Inc.

(‘Petitioner’).”). Even if SanDisk were unrelated to a defendant, “if the issues are the same as, or substantially similar to, those already or about to be litigated, or other circumstances weigh against redoing the work of another tribunal, the Board may, nonetheless, exercise the authority to deny institution.” *Fintiv*, 14.

This factor therefore weighs in favor of denial. *Fintiv*, 13-14. And, if the Board deems SanDisk unrelated, it should still deny institution. *Id.*

6. Factor 6 favors denial, but Polaris will raise its merits arguments in the POPR.

Under the sixth *Fintiv* factor, the Board may consider other circumstances that impact the Board’s exercise of discretion, including the merits. *Fintiv*, 14-15. Polaris’s merits arguments will be in its Patent Owner Preliminary Response (POPR), which will explain why the grounds fail to disclose the claim elements. The Director should consider these arguments when determining whether to exercise its discretion to deny institution under 35 U.S.C. § 314(a). See FAQs for Interim Process for PTAB Workload Management, FAQ8 (“The Director will receive each . . . POPR”), FAQ12 (“the Director will consider the merits in the merits briefing if the parties ask the Director to do so.”).

B. Other considerations also favor discretionary denial.

The Board’s Memorandum on the Interim Process for PTAB Workload Management presents additional considerations for discretionary denial, including:

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Whether the PTAB or another forum has already adjudicated the validity or patentability of the challenged patent claims;

Whether there have been changes in the law or new judicial precedent issued since issuance of the claims that may affect patentability;

The strength of the unpatentability challenge;

The extent of the petition's reliance on expert testimony;

Settled expectations of the parties, such as the length of time the claims have been in force;

Compelling economic, public health, or national security interests; and

Any other considerations bearing on the Director's discretion.

Interim Processes for PTAB Workload Management at 2 (Mar. 26, 2025). There are several considerations that weigh in favor of discretionary denial here.

1. Instituting an IPR would not reduce the number of issues for the judge and jury to decide in the district court case.

The Board should also deny institution because the Petitioners have not explained how instituting an IPR would reduce the number of issues adjudicated by the district court judge and decided by a jury. For example, Petitioners have not represented or indicated that they would present fewer references or grounds to the jury if an IPR is instituted. Instead, Western Digital's extensive 3,000-page invalidity contentions show the opposite—that it will present as many grounds and references to the jury as the court allows. In the invalidity contentions, Western Digital charted ten references for the '346 patent. EX2008, *17-18. It also served a list of approximately **140** different “References and Exemplary Combinations of

References” for the ’346 patent that it reserves the right to present to the jury.

EX2008 (Appendix A).

Western Digital also cited product art from numerous companies. EX2008, *18-20. Even if the three references in the petition were removed from the candidate pool (EX1005, EX1006, EX1007), Western Digital would still have many references to combine with product art. *See* 35 U.S.C. § 315(e) (estoppels do not apply to product prior art). Instituting an IPR would therefore not reduce the number of references or grounds but instead merely shift which references and grounds the defendants decide to present to the jury.

Instituting an IPR would also not resolve other invalidity theories such as Western Digital’s arguments under 35 U.S.C. §§ 101 and 112. “Where the petitioner is relying on corresponding system art in a co-pending proceeding *and/or several other invalidity theories*, a stipulation may not be particularly meaningful because the efficiency gained by any AIA proceeding will be limited.” FAQs for Interim Process for PTAB Workload Management, FAQ14 (emphasis added). Western Digital has raised, and is continuing to pursue, other invalidity theories under § 101 and § 112. EX2008, *26-32. Since these invalidity theories cannot be resolved in an IPR (35 U.S.C. § 311(b)), instituting an IPR would not resolve all the invalidity defenses at issue in the district court case and therefore not serve as a “true alternative” to the district court proceeding. *Motorola*,

IPR2024-01205, Paper 19 at 3-4.

Instituting an IPR would also not reduce issues for claim construction. In the IPR, Petitioners proposed a construction for only one term: “without storing each data block in a data buffer.” Pet., 12-15. Western Digital initially identified this term in the district court for construction (EX2009, *4), but it has subsequently dropped the term. EX2015, *3-4. The Board’s resolution of a dispute about the term would therefore not reduce the claim-construction issues for the district court. Additionally, Petitioners in the IPR alleged that the other terms should be construed according to their ordinary and customary meaning. Pet., 12. However, Western Digital in the district court has identified four other terms of the ’346 patent for construction. EX2015, *3-4. Since the grounds do not address any of the constructions the defendants intend to present in the district court, it is unclear how instituting an IPR would help the district court resolve these disputes. To the contrary, instituting an IPR may complicate claim construction issues because Petitioners appear to be taking inconsistent positions—ordinary and customary meaning for terms in the IPR but more narrow constructions in the district court, including indefiniteness.

2. The expert declaration does not provide adequate, independent analysis that should accompany a petition.

When deciding whether to deny institution under § 314(a), the Board should also consider the substantial overlap between the petition and the expert

declaration. When the declaration “merely repeats, *verbatim*, the conclusory assertion for which it is offered to support” and “does not cite to any additional supporting evidence or provide any technical reasoning to support [the] statement,” the testimony is entitled to little weight. *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (P.T.A.B. Aug. 24, 2022) (precedential); *see also* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

Petitioners submitted a declaration by Dr. Paul Min to support the arguments in the petition. But like the expert declaration in *Xerox*, Dr. Min’s declaration merely repeats, *verbatim*, conclusory assertions in the petition. He does not provide additional technical reasoning to support many of the substantive statements.

Some examples of Dr. Min’s repeating the petition (or vice versa) are provided below. Dr. Min repeats, *verbatim*, the arguments from the petition. He even uses the same italicized, bolded, and underlined styling and repeats legal conclusions with verbiage lifted straight from the petition. When Dr. Min’s declaration varies, it merely provides longer or additional block quotations that are cited in the petition.

Petition	Dr. Min Declaration
A POSITA would have been motivated to utilize Kleiman’s on-the-fly	A POSITA would have been motivated to utilize Kleiman’s on-the-fly

technique because it provides various benefits. • First, Kleiman’s on-the-fly technique “performs XOR operations on data transferred to and from the disk drives without requiring separate transfers.” Ex.1006, 1:67-2:2. • Second, the on-the-fly technique “dynamically computes a set of parity information for the RAID stripe, without requiring additional resources from any part of the system 100.” Ex.1006 3:17-20; Ex.1003, ¶67. Pet., p. 23.	technique because the on-the-fly technique “performs XOR operations on data transferred to and from the disk drives without requiring separate transfers.” Kleiman, 1:67-2:2. Additionally, the on-the-fly technique “dynamically computes a set of parity information for the RAID stripe, without requiring additional resources from any part of the system 100.” Kleiman 3:17-20. Min Declaration, ¶67.
Given that Jeddeloh’s switch may be a DMA module, a POSITA would have found it obvious to look to known techniques for DMA operations between a switch and a plurality of memory controllers. Ex.1003, ¶79. In other words, by referring to DMA techniques, Jeddeloh explicitly suggests the combination. <i>See In re Kahn</i>, 441 F.3d 977, 986 (Fed. Cir. 2006) (obviousness may be established by combining or modifying prior art elements when there is a teaching, suggestion, or motivation to do so). Ma provides an example of such known techniques. In particular, Ma provides evidence that it was known for a memory controller to request data from the host when processing write commands in a queue. Like both	Given that Jeddeloh’s switch may be a DMA module, a POSITA would have found it obvious to look to known techniques for DMA operations between a switch and a plurality of memory controllers. Ma provides an example of such known techniques. In particular, Ma provides evidence that it was known for a memory controller to request data from the host when processing write commands in a queue. Like both Jeddeloh and the ’346 patent, Ma “relates to flash-memory solid-state-drive (SSD) devices.” Ma, 1:52-53. Min Declaration, ¶79.

Jeddeloh and the '346 patent, Ma “relates to flash-memory solid-state-drive (SSD) devices.” Ex.1007, 1:52-53. Pet., 26.	
POSITA would have had a reasonable expectation of success when combining the teachings of Ma with those of Jeddeloh. Both Jeddeloh and Ma relate to solid-state storage devices that stripe data across multiple storage devices. <i>See e.g.</i>, Ex.1005, [0036] (“The non-volatile memory control circuitry 222 can be configured to operate a number of non-volatile memory devices associated with the number of memory channels as a RAID.”); Ex.1007, 2:56-58 (“It is further desired that the smart storage switch interleaves and stripes data accesses to the multiple channels of single-chip flash-memory devices.”). Accordingly, a POSITA would have expected Ma’s DMA techniques to work similarly within Jeddeloh’s system. Ex.1003, ¶82. Pet., 27-28.	A POSITA would have had a reasonable expectation of success when combining the teachings of Ma with those of Jeddeloh. Both Jeddeloh and Ma relate to solid-state storage devices that stripe data across multiple storage devices. <i>See e.g.</i>, Jeddeloh, [0036] (“The non-volatile memory control circuitry 222 can be configured to operate a number of non-volatile memory devices associated with the number of memory channels as a RAID.”); Ma, 2:56-58 (“It is further desired that the smart storage switch interleaves and stripes data accesses to the multiple channels of single-chip flash-memory devices.”). Accordingly, a POSITA would have expected Ma’s DMA techniques to work similarly within Jeddeloh’s system. Min Declaration, ¶82.
First, Jeddeloh’s control circuitry 208 includes non-volatile memory control circuitry 222, which includes a plurality of channel memory control circuits 338 (“<i>plurality of command processing units</i>”). “The memory system control circuitry 208 can include ... non-volatile memory control circuitry 222.” Ex.1005, [0024]. “The	First, Jeddeloh’s control circuitry 208 includes non-volatile memory control circuitry 222, which includes a plurality of channel memory control circuits 338 (“<i>plurality of command processing units</i>”). <u>The memory system control circuitry 208 can include</u>

non-volatile memory control circuitry 222 can be configured to write data in a first stripe across a number of memory channels as described herein.” Ex.1005, [0036]. Pet., 31.	host interface circuitry 214, host-memory translation circuitry 216, memory management circuitry 218, a switch 220, <u>non-volatile memory control circuitry 222</u>, and/or volatile memory control circuitry 224. As described herein, the memory system control circuitry 208 can be provided in the form of an ASIC, however, embodiments are not so limited. Jeddeloh, [0024]. <u>The non-volatile memory control circuitry 222 can be configured to write data in a first stripe across a number of memory channels as described herein.</u> The non-volatile memory control circuitry 222 can be configured to write updated data in a second stripe across the number of memory channels without reading or copying the data in the first stripe. In one or more embodiments, the non-volatile memory control circuitry 222 can be configured to read portions of a stripe on a page-basis without reading a remainder of the stripe. The non-volatile memory control circuitry 222 can be configured to operate a number of non-volatile memory devices

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	associated with the number of memory channels as a RAID. At least one of the number of memory channels can be operated as a parity channel and accordingly, one or more memory devices associated with the at least one of the number of memory channels can be operated as a parity memory device(s). Additional detail on stripe-based memory operation is provided in conjunction with the discussion of FIG. 4 below and throughout the present disclosure. Jeddeloh, [0036]. Min Declaration, ¶93.
Additionally, a POSITA would have found it obvious to use parity write commands when writing parity data. It was known in the art to use a parity write command when writing parity data to memory. <i>See e.g.</i>, Ex.1014, 3:3-5 (“The current proposed ANSI standard for “XOR commands” on SCSI disk drives includes read (READ), data update (XDWRITE), parity update (XPWRITE)”); Ex.1003, ¶103. Accordingly, it would have been obvious to use a parity update command, such as XPWRITE, when writing parity data to a dedicated parity channel. Pet., 36.	Additionally, a POSITA would have found it obvious to use parity write commands when writing parity data. It was known in the art to use a parity write command when writing parity data to memory. <i>See e.g.</i>, Hodges, 3:3-5 (“The current proposed ANSI standard for “XOR commands” on SCSI disk drives includes read (READ), data update (XDWRITE), parity update (XPWRITE)”); Ex.1003, ¶103. Accordingly, it would have been obvious to use a parity update command, such as XPWRITE, when writing parity data to a dedicated parity channel. Min Declaration, ¶103.

As explained above at X.C.5, it would have been obvious for Jeddeloh's memory control circuitry 208 to utilize DMA operations. See e.g., Jeddeloh, [0033]; Ex.1003, ¶107. A POSITA would have understood that when a particular channel memory control circuit processes the next command in the queue, it would request that data when ready, as taught by Ma: "flash-memory device 73 ... sends a DMA activate back to host 10 to indicate that it is ready for the DMA transfer to begin." Ex.1007, 11:40-44. Pet., 37-38.	As explained above at VIII.A.5, it would have been obvious for Jeddeloh's memory control circuitry 208 to utilize DMA operations. See e.g., Jeddeloh, [0033]. A POSITA would have understood that when a particular channel memory control circuit processes the next command in the queue, it would request that data when ready. This is evidenced by Ma: Single-chip flash-memory device 73 at endpoint-1 responds by setting up for the direct-memory access (DMA) transfer, and sends a DMA activate to smart storage switch 30, <u>which then sends a DMA activate back to host 10 to indicate that it is ready for the DMA transfer to begin.</u> Ma, 11:40-44. Min Declaration, ¶107.
Thus, because Jeddeloh describes RAID XOR circuitry, and a POSITA would have found it obvious for the RAID XOR circuitry to include a XOR buffer with XOR accumulators, Jeddeloh and Kleiman render this limitation obvious. ¶¶118-25 Pet., 44.	Thus, because Jeddeloh's memory control circuit 208 includes RAID XOR circuitry for calculating parity data, and the RAID XOR circuitry is connected to the channel memory circuitry 338 of the non-volatile memory control circuitry, Jeddeloh renders obvious "<i>a parity calculator coupled to the plurality of command processing units</i>" as claimed. Min Declaration, ¶117.

Thus, because Kleiman's on-the-fly technique uses a XOR operation, which is a Boolean logical operation, Jeddeloh and Kleiman render this limitation obvious. Ex.1003, ¶¶142-43. Pet., 49.	Thus, because Kleiman's on-the-fly technique uses a XOR operation, which is a Boolean logical operation, Jeddeloh and Kleiman render obvious <i>"wherein the parity calculator is further configured to update the data block stored in the page frame by performing a logical operation on the data block stored in the page frame and a data block following the first data block in the sequence of data blocks."</i> Min Declaration, ¶143.
A POSITA would have found it obvious to look to known techniques for determining when "all data for the recognized memory buffer has been transferred" as described by Kleiman. Ex.1006, 3:65-67; Ex.1003, ¶224. Yashiro provides one example of a known technique in which a counter is used for determining when the parity block is complete. In particular, Yashiro further describes using a counter to determine when the parity block is complete. "The counter N has been cleared to N=0 in the initial state." Ex.1008, 14:31-32. As the system processes write commands (described in the text accompanying Fig. 12), the "count value of the count N ... is increased by 1." Ex.1008, 14:30-31. If the counter N has not yet reached the "set [] number of [] times" (i.e., a threshold), then the method returns to processing the next write command with respect to Fig. 12.	A POSITA would have found it obvious to look to known techniques for determining when "all data for the recognized memory buffer has been transferred" as described by Kleiman. Yashiro provides one example of a known technique in which a counter is used for determining when the parity block is complete. In particular, Yashiro further describes using a counter to determine when the parity block is complete. "The counter N has been cleared to N=0 in the initial state." Yashiro, 14:31-32. As the system processes write commands (described in the text accompanying Fig. 12), the "count value of the count N ... is increased by 1." Yashiro, 14:30-31. If the counter N has not yet reached the "set number of times" (i.e., a threshold), then the method returns to processing the next write command with respect to Fig. 12. However, once the counter reaches the threshold, the

However, once the counter reaches the threshold, the parity block is complete and the parity block can be stored on the disk in Step 8. See Ex.1008, 14:28-55. Pet., 71.	parity block is complete and the parity block can be stored on the disk in Step 8. See Yashiro, 14:28-55. Min Declaration, ¶224.

Interestingly, Dr. Min's declaration follows the same formatting and verbiage as a declaration from a different expert (Dr. Lara Dolecek), which was filed by the same law firm. *SanDisk Technologies, Inc. et al. v. Polaris PowerLED Techs., LLC*, IPR2025-00515, Exhibit 1003 (P.T.A.B. Jan. 29, 2025).

Petitioners have also not established that Dr. Min has the requisite expertise specific to data stripe operations on data blocks for the memory systems at issue in this IPR. Dr. Min's declaration explains that he has a background in electrical engineering (¶¶9, 14), has developed semiconductor devices and circuits (¶10), and has expertise in networks and wireless cellular communications (¶¶11, 13, 18, 20, 21). One paragraph of the background section of his declaration refers to memory, but even this is silent with respect to parity data generation at issue in this case:

Many of the integrated circuit chips I have developed incorporates high speed memory modules interacting with the memory controllers to perform various types of operations including pointer processing, pattern matching, tree-searching, and mathematical manipulation that require extremely fast read/write/bulk-transfer from/to the memory contents. For example, the latest generations of the switching fabric that

I developed incorporated what is known in the switching field as the virtual output queue based on shared memory. In the switch fabric based on the virtual output queue based on shared memory architecture, there is no space-division switching, and rather, the switching is performed from the shared memory that takes in all of the incoming packets, which are manipulated by the pointers that organized the packets in the memory.

Min Declaration, ¶19.

The lack of supporting evidence and additional technical reasoning from an expert who does not appear to have background experience specific to technology at issue in this case is yet another reason why the Board should deny institution. The standard for what qualifies as independent expert testimony and its use within IPRs should be higher; the declaration should not merely “cop[y], word-for-word, Petitioner’s conclusory assertions.” *Xerox*, IPR2022-00624, Paper 9 at 5. When it does, the Board should deny institution.

3. The ’346 patent issued over eleven years ago.

Under the interim process, the Director can consider “[s]ettled expectations of the parties, such as the length of time the claims have been in force” when deciding whether to exercise discretion to deny institution. Interim Processes for PTAB Workload Management at 2 (Mar. 26, 2025). Here, the ’346 patent issued on December 3, 2013—over eleven years ago. Had Petitioners objected to the issuance of the ’346 patent, they could have raised challenges over a decade ago.

35 U.S.C. §§ 302 (permitting any person at any time to file a request for reexamination), 321 (permitting post-grant review challenges up to 9-months after issuance). Instead, Petitioners waited until after Polaris relied on the issued claims in its complaint for patent infringement. This extended delay in challenging the claims also favors denying institution.

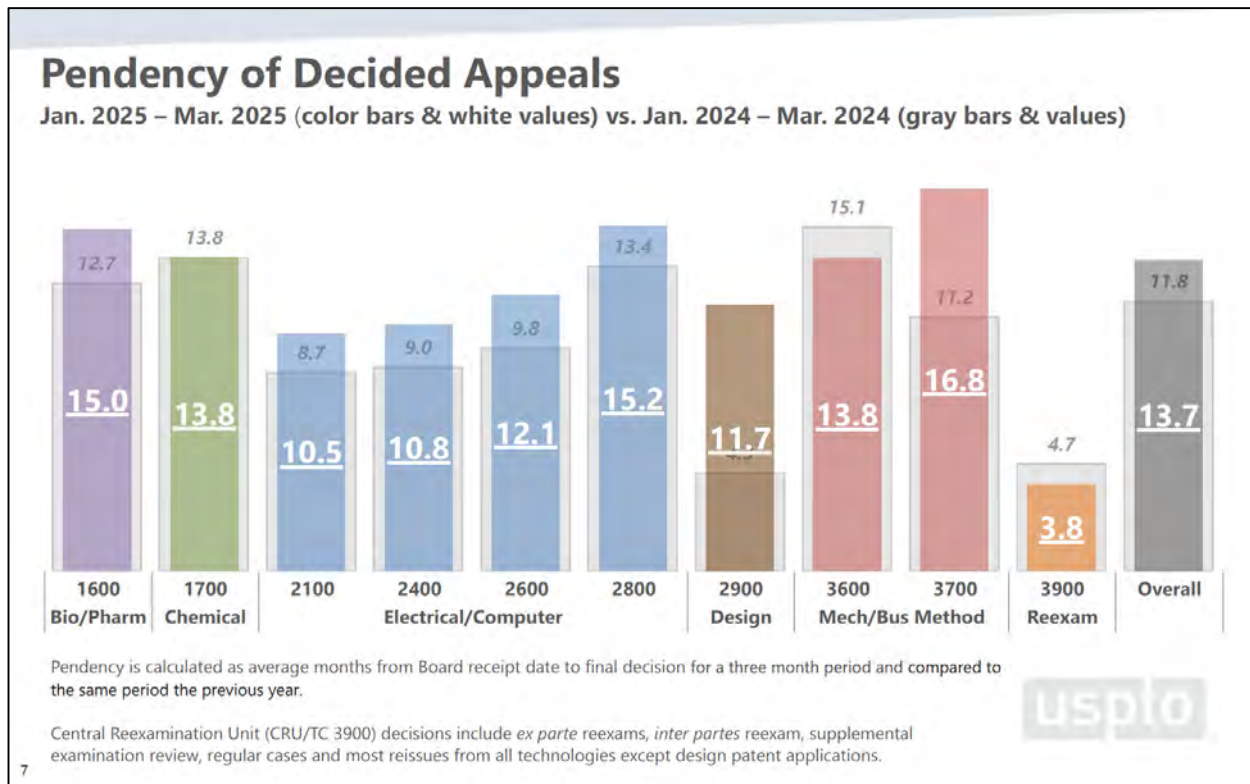
4. PTAB resources are better spent on *ex parte* appeals.

The Board should also deny institution because its limited resources are better spent on the growing backlog of *ex parte* appeals. In 35 U.S.C. § 6(b)(1), the Board is tasked with “review[ing] adverse decisions of examiners upon applications for patent pursuant to section 134(a).” Congress also tasked the Board with reviewing appeals of reexaminations, derivation proceedings, IPRs, and PGRs. 35 U.S.C. § 6(b)(2)-(4). But current Office policy is to focus on *ex parte* appeals: “To ensure that the PTAB continues to meet its statutory obligations as to *ex parte* appeals, while continuing to maintain its capacity to conduct AIA proceedings, the Director will exercise her discretion on institution of AIA proceedings” Interim Processes for PTAB Workload Management at 1 (Mar. 26, 2025). The Board should exercise that discretion here because the pendency of *ex parte* appeals has increased (EX2012, 7), nearly a quarter of *ex parte* appeals have been pending more than eleven months (EX2013), and the backlog is growing month-over-month in almost all technology centers (EX2012, 4).

According to the latest data published by the USPTO, roughly a quarter of all *ex parte* appeals have been pending for over eleven months. EX2013.⁶ In 2025, the pendency has increased in almost every technical center. Shown below, the time (in months) to a final decision has increased in 2025 (shown with the color bars and white values) compared to the same data from 2024 (shown with the gray bars and gray values). For the technology center of the '346 patent—2100⁷—the pendency has increased from 8.7 months to 10.5 months, a 20.7% increase.

⁶ The latest data on the PTAB Dashboard is from November 2023. However, the data from FY24 and FY25 also indicates that a substantial number of cases have been pending for over eleven months.

⁷ The '346 patent describes systems and methods for generating parity data in a nonvolatile memory controller. Patents for “Memory Access and Control” are under 2130 and patents for “Computer Error Control, Reliability, & Control Systems” are under 2110, both of which are within tech center 2100 (Computer Architecture Software and Information Security).



EX2012, 7.

In the current fiscal year (FY25), the PTAB's backlog of *ex parte* appeals in the 2100 technology center has also increased. Shown below, in FY25, the PTAB's starting inventory of *ex parte* appeals in the technology center 2100 was 367 cases. EX2012, 4. In FY25 (October 2024 through March 2025), 225 appeals have been filed, whereas the PTAB decided 181 appeals. *Id.* This has increased the backlog for technology center 2100 by 12% (44 cases)—the highest increase in number of cases outstanding for any technology center during FY25. *See id.*

Receipts & Dispositions (Fiscal Year through Mar. 31, 2025)												
Technology Center	Starting Inventory	Appeals Filed	Affirmed	Affirmed -in-Part	Reversed	Panel Remand	Admin Remand	Dismissed	Appeals Decided	Ending Inventory	Inventory Change	% of Inventory
1600	442	191	125	8	66	0	0	7	206	427	▼ -15	9.3%
1700	843	330	210	28	102	0	0	4	344	829	▼ -14	18.1%
2100	367	225	108	22	46	0	3	2	181	411	▲ 44	9.0%
2400	323	164	90	20	47	0	0	0	157	330	▲ 7	7.2%
2600	257	135	69	7	19	0	0	0	95	297	▲ 40	6.5%
2800	346	149	71	14	56	0	0	0	141	354	▲ 8	7.7%
2900	28	5	16	0	4	0	0	0	20	13	▼ -15	0.3%
3600	1,072	384	417	22	89	0	1	1	530	926	▼ -146	20.2%
3700	951	356	183	51	88	0	1	2	325	982	▲ 31	21.4%
3900 (Ex Parte)	12	23	13	0	4	0	1	0	18	17	▲ 5	0.4%
3900 (Sup. Exam)	0	0	0	0	0	0	0	0	0	0	— 0	0.0%
3900 (Reissue)	7	12	10	0	5	0	0	0	15	4	▼ -3	0.1%
3900 (Regular)	2	0	0	0	0	0	0	0	0	2	— 0	0.0%
Board Total	4,650	1,974	1,312	172	526	0	6	16	2,032	4,592	▼ -58	100.0%

% Decisions					
Affirmed	Affirmed-in-Part	Reversed	Panel Remand	Admin Remand	Dismissed
64.6%	8.5%	25.9%	0.0%	0.3%	0.8%

EX2012, 4 (annotated).

To reduce the average time to final decision, the 411 currently pending *ex parte* appeals in technology center 2100, the 12% backlog growth in the 2100 technology center during FY25, and the 4,592 currently outstanding *ex parte* appeals overall, the PTAB should focus its efforts on the pending *ex parte* appeals—not this IPR, especially since the district court is already scheduled to adjudicate validity months *before* the Board reaches its final decision.

In total, the other considerations also favor discretionary denial.

III. CONCLUSION

Litigating the same or similar issues at the Board as the issues that are already scheduled to get resolved in the district court would be duplicative and contrary to the intent of IPRs for “providing a more efficient system for challenging patents” and “reducing unwarranted litigation costs.” H.R. Rep. No. 112-98 at 39-40 (2011); *see also NHK Spring*, IPR2018-00752, Paper 8 at 19-20. The Board’s limited resources would be better spent elsewhere.

Respectfully submitted,

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Date: April 25, 2025

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CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

1. This Patent Owner's Brief on Discretionary Denial complies with the type-volume limitation of 14,000 words, comprising 7,814 words, excluding the parts exempted by 37 C.F.R. § 42.24(a)(1).

2. This Patent Owner's Brief on Discretionary Denial complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word 2016 in 14-point Times New Roman font.

Respectfully submitted,

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Case IPR2025-00516
U.S. Patent No. 8,601,346

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

I certify that the above-captioned **PATENT OWNER'S BRIEF ON
DISCRETIONARY DENIAL** and associated Exhibits 2001-2015 were served in
their entireties on April 25, 2025, upon the following parties via electronic mail:

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND
WESTERN DIGITAL TECHNOLOGIES, INC.
Petitioner,

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner.

IPR2025-00516
U.S. Patent No. 8,601,346

**PETITIONER'S OPPOSITION TO PATENT OWNER'S
REQUEST FOR DISCRETIONARY DENIAL**

Opposition to Patent Owner's Request for Discretionary Denial
IPR2025-00516 (U.S. Patent 8,601,346)

I. Introduction

Petitioner respectfully requests that the Director decline to exercise her discretion to deny institution and advance the Petition to a merits panel for consideration.

Petitioners Western Digital Technologies, Inc. and Sandisk Technologies Inc. (together "Petitioner") oppose Patent Owner's Request for Discretionary Denial (Paper 9, "PO Brief") because denial is inappropriate under *Fintiv* and the additional factors set forth in the Acting Director's "Interim Processes for PTAB Workload Management" ("Director Memo").

With respect to *Fintiv*, five of the six *Fintiv* factors strongly weigh against denial. Because the parallel litigation has been stayed and in view of Petitioner's "*Sotera*" stipulation, this IPR is a "true alternative" to the parallel litigation.

The additional factors listed in the Director Memo similarly weigh against denial. Petitioner has a compelling interest in having access to cost-effective PTAB review when accused of infringement by entities that do not manufacture or innovate. Patent Owner (Polaris PowerLED) has no compelling interest or expectation sufficient to avoid PTAB review, because unlike the original owner of the '346 patent, Patent Owner is an assertion entity who appears to have acquired the patent three years ago solely for the purpose of litigation—which changes everything with respect to settled expectations. Further, the Petition does not rely

Opposition to Patent Owner's Request for Discretionary Denial
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on expert testimony for gap-filling any claim elements. Instead, all claim elements are shown in the printed publication prior art, and the petition relies upon expert testimony to the extent necessary under Federal Circuit precedent to show how a POSITA would read and understand these references.

This IPR is one of three IPRs challenging three patents asserted in the stayed parallel litigation. Ex.1031, 1. These three patents are from different families and address three distinct and well-established technologies associated with memory systems respectively: Error Correcting Coding (ECC), redundant array of independent disks (RAID), and interrupt handling. Therefore, they are better suited for PTAB review, where the Board's technical expertise is well-suited to assess the distinctions and technical details of the asserted claims and the prior art presented in the obviousness grounds. The District Court in the parallel litigation agrees, having stayed the litigation so that the PTAB can handle this accordingly.

II. Discretionary denial under *Fintiv* is not warranted.

The *Fintiv* factors, considered as a whole, do not warrant denial. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential). Every factor either favors institution or is neutral.

A. Factor 1 weighs strongly against denial: A stay was granted.

The parallel Litigation "is still in early stages of litigation" and has been stayed. Ex.1031, 4. The Court granted Petitioner's Motion to Stay Pending IPRs on

Opposition to Patent Owner's Request for Discretionary Denial
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June 24, 2025. *Id.*, 1. The stay remains in effect pending resolution of the IPR proceedings. With the parallel litigation stayed, this IPR is a true alternative to district court litigation. Thus, this factor strongly weighs against denial.

B. Factor 2 weighs strongly against denial: The parallel litigation was stayed.

While the scheduling originally indicated a trial date around the same time as the projected Final Written Decision (“FWD”), this previously scheduled trial date, together with other scheduled dates, was “**VACATED** and taken off the calendar.” Ex.1031, 9. No trial date is scheduled.

Accordingly, Factor 2 strongly weighs against denial in view of the stay in the parallel litigation.

C. Factor 3 weighs strongly against denial: Minimal relevant investment and diligent filing.

Factor 3 weighs strongly against discretionary denial because, at institution, investment by the court and parties will have been minimal as to the activities pertinent to *Fintiv*. Patent Owner's Request for Discretionary Denial includes a laundry list of activities allegedly showing substantial investment, but very few relate to invalidity of the '346 patent. *See* PO Brief, 7-9. Under *Fintiv*, “[i]f, at the time of the institution decision, the district court has not issued orders ***related to the patent at issue in the petition***, this fact weighs against exercising discretion to deny institution.” *Fintiv*, 10. Not only is there no order, no claim construction

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briefing has been done. The Court confirmed that “the case is in its *early* stages and there is still more work ahead of the parties and the Court than behind them.” Ex.1031, 4 (citations omitted, emphasis added).

This factor also weighs against denial because the Petitioner worked diligently to file the instant petition after receiving Patent Owner's infringement contentions and diligently filed the now-grated motion for stay. *Fintiv*, 11. Petitioner received Plaintiff's infringement contentions on October 2, 2024 (Ex.1022), and worked diligently to file three IPR petitions, including the instant petition, *within four months*. At the time of the filing, the parallel litigation was in its early stages and claim construction briefing had yet to begin. The Board has recently agreed that similar diligence is reasonable and weighs against denial. *See Samsung Elecs. Co., Ltd. v. Mullen Industries LLC*, IPR2024-01472, Paper 9 at 10 (Mar. 31, 2025) (“Petitioner's diligence in filing its Petition (a) less than five months after receiving Patent Owner's infringement contentions and (b) prior to the parties briefing claim construction issues weighs against exercising discretionary denial.”).

Accordingly, Factor 3 weighs strongly against denial.

D. Factor 4 weighs strongly against denial: Petitioner's “Sotera” stipulation.

Factor 4 weighs strongly against discretionary denial. First, the Court, in staying the parallel litigation, explained the benefits of PTAB review, including

Opposition to Patent Owner's Request for Discretionary Denial
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simplification of issues and trial in the parallel litigation. The Court reasoned that there is “a likelihood that ‘the outcome of the [IPR] could eliminate the need for trial if the claims are cancelled or, if the claims survive, facilitate trial by providing the court with expert opinion of the [Patent and Trial Office] and clarifying the scope of the claims.’” Ex.1031, 6. And “[i]f the PTAB cancels or narrows a portion of the asserted claims, the scope of this litigation may be significantly reduced.” Ex.1031, 5 (citations omitted).

Second, Petitioner has made a *Sotera* stipulation in district court. See Ex.1018 (stipulation filed in parallel district court proceeding). Specifically, Petitioner stipulated that:

[I]f the PTAB institutes an IPR in response to Defendant's petition against Plaintiff's U.S. Patent No. 8,601,346 (IPR2025-00516), Defendant will not pursue in this litigation against the claims challenged in IPR2025-00516, (i) the specific grounds raised in IPR2025-00516, or (ii) any other grounds that could have reasonably been raised before the PTAB in that instituted proceeding (i.e., any ground that could have reasonably been raised under §§ 102 or 103 on the basis of prior art patents or printed publications).

Ex.1018, 1-2.

Petitioner's *Sotera* stipulation was timely under the procedures in place when the petition was filed. At the time of filing on January 23, 2025, PTAB precedent provided that the “appropriate time for a petitioner to offer a stipulation

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related to the *Fintiv* factor 4 analysis is prior to the Board's decision of whether to institute review." *NXP USA, Inc. v. Impinj, Inc.*, IPR2021-01556, Paper 13 at 4 (Sept. 7, 2022) (de-designated precedential Apr. 25, 2025); *see also Nike, Inc. v. ADIDAS AG*, 955 F.3d 45, 52 (Fed. Cir. 2020) ("In interpreting the APA's notice provisions in the context of IPR proceedings, we have cautioned that an agency may not change theories in midstream without giving respondents reasonable notice of the change and the opportunity to present argument under the new theory.") (citation and quotation marks omitted).

Patent Owner argues that this stipulation is "too late" under the procedures defined in the FAQs. PO Brief, 13. The FAQs state: "A petitioner should file a *Sotera* or *Sand* stipulation as soon as practicable, so that a patent owner may address the impact of the stipulation in its discretionary denial brief." Ex.1020, FAQ 14. Petitioner filed this *Sotera* stipulation as soon as practicable on April 28, 2025—three days after the FAQs were issued. In an apparent attempt to preclude consideration of a stipulation, Patent Owner filed their brief on April 25, 2025—almost one month before their due date of May 24, 2025. Had Patent Owner filed on their actual due date, Patent Owner would have had nearly one month to consider and brief the *Sotera* stipulation—provided there is anything to be said. Patent Owner's early filing should not preclude consideration of Petitioner's *Sotera* stipulation. And Patent Owner had ample opportunity to brief the expected

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Sotera stipulation in their discretionary denial brief or any supplemental briefing they could have asked for.

Petitioner respectfully submits that this stipulation outweighs all other *Fintiv* factors as it eliminates overlap with invalidity issues raised in the parallel proceeding. Petitioner's stipulation is consistent with the scope of estoppel under 35 U.S.C. § 315(e)(2). See *Ingenico Inc. v. IOENGINE, LLC*, No. 2023-1367, 2025 WL 1318188, at *8 (Fed. Cir. May 7, 2025) ("IPR estoppel did not preclude Ingenico from relying on the DiskOnKey System with related printed publications at trial...").

This case is distinguishable from the *Motorola Solutions* case cited by Patent Owner. PO Brief, 14. In *Motorola Solutions*, the Director found that the *Sotera* stipulation did not outweigh the substantial investment in the district court proceeding, where "the parties had served extensive infringement and invalidity contentions, served opening and rebuttal expert reports, filed claim construction briefs, and conducted several deposition," and the "court also had held a claim construction hearing and construed the disputed claim terms," before the litigation was stayed after institution. See *Motorola Solutions, Inc. v. Stellar, LLC*, IPR2024-01205, Paper 19 at 3-4 (P.T.A.B. Mar. 28, 2025). Here however, the parallel litigation is in early stages when the stay was issued.

Also weighing against denial under Factor 4 is that Petitioner's challenge

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encompasses claims 12 and 18, which are not at issue in the litigation. And only the asserted claims are the subject of Petitioner’s invalidity contentions on the parallel litigation. *See* Ex.2008, 1 (asserting invalidity “***only to the asserted claims identified by Polaris in its Infringement Contentions.***”). Petitioner elected to challenge additional, unasserted claims for efficiency reasons—for example, to avoid filing a second IPR in the event Patent Owner asserts additional claims in the parallel litigation.

These additional challenged (but unasserted) claims differ in claim scope from the asserted claims, meaning that key issues in the petition will not be resolved by the district court—further reducing the degree of overlap under Factor 4. *See Fintiv*, 13 (examining whether the district court will “resolve key issues in the petition”).

Petitioner’s *Sotera* stipulation also moots Patent Owner’s argument that “Petitioners appear to have strategically omitted the defendant Western Digital Corporation—the parent corporation of Western Digital Technologies, Inc.—from the petition to evade estoppels.” PO Brief, 15. Western Digital Corporation has explicitly agreed to be bound by Petitioner’s *Sotera* stipulation. Ex.1018, 1. Additionally, Western Digital Corporation has explicitly “agree[d] to be bound by the estoppel effect of the IPRs” in its Reply for Motion to Stay. Ex.2011, 2 (“Western Digital Corporation agrees to be bound by statutory estoppel ***to the***

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same extent as Western Digital Technologies"). Western Digital Corporation's agreement to be bound by estoppel effect of the IPR is not conditioned upon the stay being granted. Western Digital Corporation is thus not "evad[ing] estoppel" as Patent Owner argues. PO Brief, 15. Ex.1031, 6.

Accordingly, Factor 4 weighs strongly against denial because of (i) Petitioner's *Sotera* stipulation and (ii) key issues in the Petition that will not be resolved by the district court.

E. Factor 5 is neutral: Petitioner is a defendant in the parallel litigation.

Petitioner Western Digital Technologies, Inc. is a defendant in the parallel litigation. That is true of most IPR petitioners, making this factor neutral. *See HP Inc. v. Slingshot Printing LLC*, IPR2020-01084, Paper 13 at 9 (Jan. 14, 2021); *see also NVIDIA Corp. v. Invensas Corp.*, IPR2020-00603, Paper 11 at 23 (Sept. 3, 2020) (this factor weighs against discretionary denial where the district court trial and IPR final written decision are expected "around the same time").

F. Factor 6 weighs against denial: The merits of the Petition are particularly strong.

Factor 6 favors institution because the Petition plainly shows that the challenged claims of the '346 patent claims are unpatentable. In its PO Brief, Patent Owner does not raise any specific merits arguments other than stating that it will present merits arguments in its Patent Owner Preliminary Response (POPR).

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However, as discussed in detail below at III.A, Patent Owner's merits arguments in its POPR do not hold up under scrutiny. Thus, the merits of the Petition are particularly strong, favoring institution.

G. The *Fintiv* factors as a whole weigh against denial.

In summary, each *Fintiv* factor is either neutral or weighs against denial:

Factor	Weight	Reason
1 (stay)	against denial	a stay has been granted
2 (trial gap)	strongly against denial	A stay has been granted and thus there is no scheduled trial date
3 (investment)	against denial	Parallel litigation in early stages and no court orders regarding invalidity of the '346 patent
4 (overlap)	strongly against denial	<i>Sotera</i> stipulation; key issues not resolved by district court
5 (same party)	neutral	Petitioner is defendant
6 (merits)	strongly against denial	Strength of the patentability challenge is strong

In light of all the *Fintiv* factors as a whole, the Director should not discretionarily deny institution under §314(a).

III. The additional factors set forth in the Memorandum favor institution

The Director Memo invites the parties to “address all relevant [discretionary denial] considerations” and provides a list of potential factors. Director Memo, 2-3. Each of the potential factors favors institution:

- The unpatentability challenges in the Petition are particularly strong given that the prior art shows the same on-the-fly parity calculation techniques that are claimed.

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- The Petition relies upon expert testimony to the extent necessary under Federal Circuit precedent, and such expert testimony is supported by evidence as required under 37 CFR § 42.65 and *Xerox*.
- Patent Owner cannot reasonably allege settled expectations regarding the '346 patent based on a few years of ownership and the lack of any post-issuance validity challenge.
- Neither the PTAB nor another forum has adjudicated the validity of the '346 patent.
- Patent Owner does not allege that any changes in the law or new judicial precedent issued since issuance of the claims affects patentability.
- The United States has a compelling economic and national security interest in ensuring Sandisk and Western Digital, leading domestic technology innovators, have access to efficient AIA proceedings when faced with meritless lawsuits by non-practicing entities.

Several of these factors are of particular importance to the Director's discretion and are addressed individually below.

A. The merits of the Petition are particularly strong because the prior art teaches the same on-the-fly technique that is claimed.

The '346 patent should not have issued because it claims no more than well-known concepts related to the parity calculation techniques described and claimed in the '346 patent. The '346 patent is thus one of the patents Congress referred to when discussing the purpose of the America Invents Act—"improving patent quality and providing **a more efficient system for challenging patents that**

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should not have issued." House Report (H.R. Rep. 112-98, 2011), 39-40.

As stated in the Petition, the '346 patent was allowed after amending the claims to cover the concept in which "the parity calculator generates the parity block **on the fly** as the command processing units and the parity calculator are receiving the data blocks for the data stripe operation." Ex.1001, 4:7-11; Ex.1002, 146; Petition, 1.

However, it was already known to calculate parity data in this manner. The Jeddeloh reference describes using "RAID XOR circuitry [to] calculate parity data" and distribute commands among a plurality of "channel memory control circuit[s] 338-1, ...338-N." Ex.1005, [0027], [0038]. And the Kleiman reference (entitled "Fly-by XOR for Generating Parity for Data Gleaned from a Bus) shows that it was known to use RAID XOR circuitry "for performing fly-by XOR." Ex.1006, 3:38; Petition, 1.

Patent Owner's merits-based arguments do not hold up under scrutiny and thus the merits of the case remain strong, favoring institution. Patent Owner argues that the director should consider their POPR arguments "when determining whether to exercise its discretion to deny institution." PO Brief, 6. But the POPR does not refute the analysis in the Petition.

For example, the Petition cites to Jedelloh's data stripe operation—which is performed on several memory pages—as teaching the claimed "*performing a data*

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stripe operation on a plurality of data blocks." Petition, 28-31; Ex.1005, [0012], [0040]. Patent Owner argues that "Petitioners have not shown that such a broad construction of 'block' is supported by the record." POPR, 7. But this argument ignores that the claim itself supports this interpretation by reciting that the blocks are stored one-at-a-time in a "page frame." See Ex.1001, claim 1; Petition, 43-48.

Because Patent Owner has not effectively disputed the Petition's analysis, the strength of the patentability challenge remains strong. Petitioner respectfully requests that the Director pass this case to a merits panel and requests that the Board institute trial.

B. The Petition properly relies on expert testimony

The Petition's compliance with Federal Circuit precedent should not be a reason for discretionary denial. And Dr. Min's opinions are fully supported by the evidence of record.

1. Federal Circuit precedent requires that the Petition rely on expert testimony.

Petitioner's reliance on expert testimony as required by Federal Circuit precedent should not be a reason for discretionary denial. The foundational decisions upon which patent law is based—*Phillips*, *KSR*, etc.—require the adjudicator to evaluate the patent and prior art from perspective of a POSITA. That perspective is established with evidence, often in the form of expert declarations. Attorney argument is insufficient.

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It is well established that patent claims are construed based on the understanding of a POSITA. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (“We have made clear, moreover, that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.”) (citing *Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004) (“A court construing a patent claim seeks to accord a claim the meaning it would have to a person of ordinary skill in the art at the time of the invention.”)); *Home Diagnostics, Inc. v. LifeScan, Inc.*, 381 F.3d 1352, 1358 (Fed. Cir. 2004) (“customary meaning” refers to the “customary meaning in [the] art field”); *Ferguson Beauregard/Logic Controls v. Mega Sys., LLC*, 350 F.3d 1327, 1338 (Fed. Cir. 2003) (claim terms “are examined through the viewing glass of a person skilled in the art”); see also *PC Connector Solutions LLC v. SmartDisk Corp.*, 406 F.3d 1359, 1363 (Fed. Cir. 2005) (meaning of claim “must be interpreted as of [the] effective filing date” of the patent application); *Schering Corp. v. Amgen Inc.*, 222 F.3d 1347, 1353 (Fed. Cir. 2000) (same)).

Obviousness grounds are likewise evaluated from the perspective of a POSITA. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007) (“If a person of ordinary skill can implement a predictable variation, §103 likely bars its

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patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.”), 418 (“[I]t can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.”), 421 (“A person of ordinary skill is also a person of ordinary creativity, not an automaton.”).

The Federal Circuit has also made it clear that attorney argument alone is not evidence and should be given little weight. *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1043 (Fed. Cir. 2017) (“Attorney argument is not evidence.”) (citing *Gemtron Corp. v. Saint-Gobain Corp.*, 572 F.3d 1371, 1380 (Fed. Cir. 2009) (“[U]nsworn attorney argument . . . is not evidence and cannot rebut . . . other admitted evidence . . .”)); see also *Elbit Sys. Of Am., LLC, v. Thales Visionix, Inc.*, 881 F.3d 1354, 1359 (Fed. Cir. 2018) (“Elbit fails to present any evidence supporting this contention beyond attorney argument . . . and ‘[a]ttorney argument is not evidence’ and cannot rebut other admitted evidence.”).

Because attorney argument is not evidence, expert testimony is *necessary* to properly support a petition’s claim construction and obviousness positions, which are evaluated from the perspective of a POSITA. This is precisely how the Petition

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presents and uses the testimony of Dr. Min. *See generally* Petition, (relying on testimony of Dr. Min to support obviousness grounds). The unpatentability grounds set forth in the Petition are fully supported by the references themselves—Dr. Min's testimony serves to confirm, support, and explain the disclosures of the references from the perspective of a POSITA. *See generally* Ex.1003.

Importantly, Dr. Min was a POSITA as of the critical date of the '346 patent. Ex.1003, ¶¶7-24. Dr. Min defines a POSITA as someone with “a working knowledge of the memory system art that is pertinent to the '346 patent, including memory systems and memory controllers.” Ex.1003, ¶22. Dr. Min has such experience, as he “implemented a number of semiconductor integrated circuit chips” including “switch fabrics, processors, high speed interfaces, protocol transposers, controllers, content search engine, pattern matching, and memory cells and arrays.” Ex.1003, ¶19.

Patent Owner nevertheless argues that Dr. Min “does not appear to have background experience specific to technology at issue in this case.” PO Brief, 28. But Patent Owner has not argued for or proposed a different definition of a POSITA. And the specific details Patent Owner refers to of “data stripe operations” and “parity calculation” are encompassed by Dr. Min's more general definition of a POSITA and his experience with memory systems. And in any event, disputes over the definition of a POSITA should not be a reason for

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discretionary denial.

Further, Dr. Min's testimony is supported by corroborating evidence in the form of the disclosure of the references relied upon in the unpatentability grounds (e.g., Ex.1005, Ex.1006, Ex.1007, Ex.1008) and several tertiary references (e.g., Ex.1009, Ex.1011, Ex.1012, Ex.1013, Ex.1014). *See generally*, Ex.1003. Further still, Dr. Min repeatedly provides technical reasoning to support his statements and understandings of the references. *See generally*, Ex.1003.

Further, the Federal Circuit has recognized that "when the technology is complex and 'beyond the comprehension of laypersons,' expert testimony is 'sometimes essential.'" *Synopsys, Inc. v. Mentor Graphics Corp.*, 814 F.3d 1309, 1320 (Fed. Cir. 2016) (internal quotations removed); *see also Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1330 (Fed. Cir. 2009) ("If the relevant technology were complex, the court might require expert opinions."). This is precisely the situation here. Dr. Min's expertise is utilized to explain the technical background of complicated concepts relevant to the '346 patent (*see, e.g.*, Ex.1003, ¶¶29-34). Dr. Min also provides detailed explanations regarding how a POSITA would have understood the technical descriptions found in the '346 patent and the prior art references (*see, e.g.*, Ex.1003, ¶¶29-235). Dr. Min's testimony serves these essential purposes and is a strength of the Petition.

2. Patent Owner's arguments based upon Xerox are misplaced.

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Patent Owner argues that “Dr. Min’s declaration merely repeats, verbatim, conclusory assertions in the petition.” PO Brief, 21 (citing *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15-17 (August 24, 2022) (precedential)). *Xerox*, however, does not stand for the proposition that a Petition and supporting declaration cannot be similar. *Xerox* instead focuses on whether the expert testimony cites to “supporting evidence or provide[s] any technical reasoning.” *Xerox*, 15. Expert testimony is only afforded less weight if it “adds little to the conclusory assertion for which it is offered to support.” *Id.* Here, Dr. Min’s analysis is fully supported by evidence, and does not rely on improper gap filling. Accordingly, the Petition’s proper reliance on expert testimony to support the unpatentability grounds favors institution.

C. Patent Owner’s “settled expectations” argument is inconsistent with the purpose of the AIA.

Patent Owner has no compelling interest or expectation sufficient to avoid PTAB review because they only acquired the ’346 patent three years ago and they appear to have done so solely for the purpose of litigation. Patent Owner notes that “the ’346 patent issued on December 3, 2013—over eleven years ago.” PO Brief, 29. But as a non-practicing entity, Patent Owner cannot claim it has any settled expectations arising from practicing the ’346 patent. Patent Owner appears to have acquired the ’346 patent in 2022 solely for the purpose of attempting to monetize it through litigation, significantly decreasing any potential relevance of this factor.

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Moreover, Patent Owner has not made any meaningful attempt at engaging with Petitioner for licensing discussions. Instead, Patent Owner filed a complaint asserting the '346 patent against Petitioner only seven days after sending a notice letter, which predictably triggered this IPR challenge. Ex.1015, ¶45. The '346 patent is not entitled to immunity from IPR review. And regarding expectations of validity, no tribunal has ever adjudicated the validity of the '346 patent after it issued.

Accordingly, the lack of settled expectations weighs against denial.

D. The PTAB has sufficient resources to handle IPR proceedings and ex parte proceedings

The Board's statutorily defined tasks of handling both *ex parte* appeals and post-grant proceedings should not be a reason for discretionary denial. Patent Owner argues that the Board's "limited resources are better spent on the growing backlog of *ex parte* appeals." PO Brief, 30. Patent Owner further notes that the *ex parte* appeal backlog has increased. See PO Brief, 30-32.

But Patent Owner has not provided any evidence to show that the Board cannot handle both its *ex parte* appeal docket and its post-grant proceeding docket. Nor could they, given that the Board has recently publicly acknowledged that "[w]e do have enough staff so we can handle both the appeals and the trials with the judges and staff on board." Ex.1032. Accordingly, the existence of an *ex parte* appeal docket (increasing or not) is not a reason to discretionarily deny this

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specific case.**E. Compelling economic and national security interests favor institution.**

Petitioners Western Digital and Sandisk together play a multifaceted role in bolstering the US economy. As a leading provider of digital storage solutions, the companies drive significant revenue generation—with billions in annual sales that not only bolster its own financial health but also support a vast network of suppliers, service providers, and ancillary industries. Ex.1035, 4 (“Western Digital is a leading developer, manufacturer and provider of data storage devices and solutions based on both hard disk drive and NAND flash technologies. With a differentiated innovation engine driving advancements in storage and semiconductor technologies, our broad and ever-expanding portfolio delivers powerful hard disk drives (‘HDD’) and flash-based products (‘Flash’) storage solutions for everyone from students, gamers and home offices, to the largest enterprises and public clouds to capture, preserve, access and transform an ever-increasing diversity of data.”). This economic activity injects substantial funds into local communities through payrolls, tax revenues, and the multiplier effects that come with a robust manufacturing and technology ecosystem.

Moreover, Western Digital’s and Sandisk’s contributions extend to their impact on job creation and workforce development. With operations that span manufacturing, research and development, and engineering, the companies create

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skilled job opportunities and support local communities by fostering a demand for specialized talent. In doing so, they energize the broader US technology sector—promoting innovation in digital storage technologies that underpin critical infrastructure like data centers, cloud computing services, and enterprise IT systems. This technological backbone not only facilitates business operations nationwide but also reinforces American leadership in the rapidly evolving digital age. This type of advanced domestic engineering capacity is critical to U.S. economic interests.

The United States thus has a compelling economic and national security interest in providing Western Digital and Sandisk an opportunity to challenge the '346 patent under the more efficient IPR framework. As leading American technology companies, it is critical that Western Digital and Sandisk have the ability to invest and innovate without being encumbered by invalid patents. Petitioner's right to seek review of such patents by the U.S. Patent and Trademark Office is similarly critical.

It is vital that companies like Western Digital and Sandisk are provided an effective and efficient mechanism for challenging invalid patents asserted against them. Congress created the AIA for this purpose. 77 F. Reg. No. 157, 48612 (Aug. 14, 2012) ("The purpose of the AIA ... is to establish a more efficient and streamlined patent system that will improve patent quality and limit unnecessary

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and counterproductive litigation costs.”); *see also General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 16-17 (Sept. 6, 2017) (“[W]e recognize that an objective of the AIA is to provide an effective and efficient alternative to district court litigation.”). AIA proceedings create cost savings for its participants via “reductions in legal fees incurred and the greater probability of a settlement or early-stage resolution.” Ex.1037 (study of AIA economic benefits), 2, 8 (“[T]he total economic benefits of *inter partes* reviews resulting in stay of litigation in district court included **an increase in US business activity of \$1.87 billion in gross product and 8,530 job-years of employment**”; “In situations where an *inter partes* review was conducted parallel to a district court proceeding, the economic benefits of [*inter partes* reviews] include estimated **increases of \$135.4 million in US gross product and 617 person-years of employment**”).

Petitioners Western Digital and Sandisk are seeking review of the '346 patent consistent with the purpose of AIA post-grant proceedings: an efficient, technically reliable assessment of validity. And Petitioner's *Sotera* stipulation demonstrates that it desires a true district court alternative. Denying Petitioners access to IPR in this scenario would frustrate the purpose of the AIA and deny Petitioner the specific economic benefits envisioned by Congress.

These economic interests are particularly compelling as Petitioners have

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been accused of infringement by a non-practicing entity, Polaris. For these reasons, compelling economic and national security interests favor institution.

IV. The new Interim Process should not govern the decision to institute.

Petitioner respectfully requests that the USPTO Director maintain the standards for institution that were in place when this Petition was filed. While the briefing above addresses the new Interim Process as best understood by Petitioner, this IPR should be governed by the procedures that were in place when it was filed, as in the June 21, 2022 Interim Procedure for Discretionary Denials issued by the Office (the "June 2022 Procedures").

Since the Petition was filed, the USPTO rescinded the June 2022 Procedures through a short posting on the USPTO website. The Office then followed up with the March 24, 2025 Memorandum of Chief Administrative Patent Judge Scott Boalick (the "Boalick Memo"). Two days later, on March 26, Acting Director Stewart issued a Memorandum (the "Director Memo") introducing an entirely new "interim procedure" that bifurcates institution between "(i) discretionary considerations and (ii) merits and other non-discretionary statutory considerations." Director Memo, 1. Three weeks after the Director Memo issued (and after approximately forty patent owners had filed briefs requesting discretionary denial), the USPTO held an oral webcast setting forth additional substantive details of the new interim procedure not found in the Director Memo.

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Then, eight days after the webcast, the USPTO posted on its website “FAQs for Interim Processes for PTAB Workload Management” with even more substantive details. The recission notice, the Boalick Memo, the Director Memo, the oral webcast, and the FAQs (together, the “Announcements”) fall short of satisfying the requisite statutory and constitutional obligations of the USPTO.

The Announcements make sweeping changes to PTAB procedures without going through notice-and-comment rulemaking. This is made more problematic given that the Office has represented to the public that they intend to make any further changes to the institution process through notice-and-comment rulemaking. See 88 Fed. Reg. 24,503 (April 21, 2023). The Announcements violate the notice-and-comment requirements under the APA and are arbitrary and capricious.

Moreover, the additional discretionary denial considerations proposed in the director memo are so broad and vague that they fail to set “forth the standards for the showing of sufficient grounds to institute review.” 35 U.S.C. § 316(a). For example, it is unclear as to how the director will consider “[s]ettled expectations,” “reliance on expert testimony,” “workload,” and “[c]ompelling economic, public health, or national security interests.”

The Director's justification for these announcements similarly falls short of statutory and constitution obligations. The Supreme Court has held that an agency's change in position must be accompanied by sufficient reasons for doing

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so. *See Food & Drug Admin. v. Wages & White Lion Invs., L.L.C.*, 145 S. Ct. 898, 906 (2025) (explaining that when an agency changes position, it must “offer ‘good reasons for the new policy’”); *see also F.C.C. v. Fox Television Stations, Inc.*, 556 U.S. 502 (2009) (agency changing position must show “that the new policy is permissible under the statute, that there are good reasons for it, and that the agency believes it to be better, which the conscious change of course adequately indicates”).

The agency's purported justifications of “efficiency” and “workload management” do not hold up under scrutiny. Providing additional discretionary denial factors increases the Office's workload by investing their time in consideration of more issues other than the validity of the patents challenged in IPR. This additional workload becomes more problematic given that the Office appears to be voluntarily *reducing* the number of judges. Ex.1033 (Law 360 article). The Office cannot claim they are resource constrained and at the same time reducing the number of PTAB judges.

Applying the Announcements retroactively to petitions filed prior to issuance of the new policies unduly prejudices petitioners. Petitioner has based their district court and PTAB proceeding based on previously-in-place procedures in order to best seek review of the patents Petitioner believes to be invalid. In light of these and other deficiencies in the Announcements, Petitioner respectfully

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requests that the Board and Director consider whether to institute based on the standards articulated in the June 2022 Procedures until such time as the Board issues new regulations in accordance with 35 U.S.C. § 316 and the rulemaking procedures of the APA.

V. Conclusion

For the above reasons, Petitioner respectfully requests that the Director refrain from exercising her discretion to deny this petition, and instead pass it to a merits panel for consideration

Respectfully submitted,

Date: June 24, 2025

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PETITIONER'S EXHIBIT LIST

Ex.1001	U.S. Patent No. 8,601,346
Ex.1002	Prosecution History of U.S. 8,601,346
Ex.1003	Declaration of Paul Min under 37 C.F.R. § 1.68
Ex.1004	Curriculum Vitae of Paul Min
Ex.1005	U.S. Patent Publication No. 2011/0078496A1 to Jeddeloh ("Jeddeloh")
Ex.1006	U.S. Patent No. 5,950,225 to Kleiman ("Kleiman")
Ex.1007	U.S. Patent No. 8,341,332 to Ma et al. ("Ma")
Ex.1008	U.S. Patent No. 5,787,460 to Yashiro et al. ("Yashiro")
Ex.1009	U.S. Patent No. 6,161,165 to Solomon et al. ("Solomon")
Ex.1010	Reserved
Ex.1011	The Authoritative Dictionary of IEEE Standards Terms: Seventh Edition; ("IEEE")
Ex.1012	U.S. Patent No. 8,074,149 to Stolowitz ("Stolowitz")
Ex.1013	U.S. Patent No. 8,819,699 to Cota-Robles ("Cota-Robles")
Ex.1014	U.S. Patent No. 6,092,215 to Hodges et al. ("Hodges")
Ex.1015	Complaint, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)
Ex.1016	District Court Trial Statistics
Ex.1017	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel

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	District Court Litigation, June 22, 2022
Ex.1018 (New)	Notice of Sotera Stipulations, Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al. 2:24-cv-02864 (C.D. CA)
Ex.1019	Reserved
Ex.1020 (New)	FAQs for Interim Processes for PTAB Workload Management, available at https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management (retrieved May 13, 2025).
Ex.1021 (New)	'346 Patent Assignment Recordation
Ex.1022 (New)	Plaintiff's Disclosure of Asserted Claims and Infringement Contentions, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA) (Served October 2, 2024)
Ex.1023-1030	Reserved
Ex.1031 (New)	Order Granting Defendants' Motion to Stay, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA) (issued June 23, 2025)
Ex.1032 (New)	"Chief Patent Board Judge Waves Off Workforce Attrition Concerns," Bloomberg Law, May 7, 2025.
Ex.1033 (New)	"PTAB Judges Told To Get Ready For Layoffs," Law 360 (March 21, 2025). https://www.law360.com/articles/2314328/ptab-judges-told-to-get-ready-for-layoffs
Ex.1034	Reserved
Ex.1035 (New)	Western Digital Investor Report
Ex.1036 (New)	Judge Wright Markman Orders

Opposition to Patent Owner’s Request for Discretionary Denial
IPR2025-00516 (U.S. Patent 8,601,346)

Ex.1037 (New)	“An Assessment of the Impact of the Inter Partes Review Process under the Patent Trial and Appeal Board on the US Economy,” The Perryman Group, available at https://www.perrymangroup.com/publications/report/2021/9/23/an-assessment-of-the-potential-impact-of-expanding-inter-partes-review-ipr-under-the-america-invents-act-on-the-us-economy/

Opposition to Patent Owner's Request for Discretionary Denial
IPR2025-00516 (U.S. Patent 8,601,346)

CERTIFICATE OF SERVICE

The undersigned certifies, under 37 C.F.R. § 42.6, that service was made on the Patent Owner as detailed below.

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Documents served **Petitioner's Opposition to Patent Owner's Request for Discretionary Denial; Exhibits Ex.1018; Ex.1020-Ex.1022; Ex.1031-Ex.1033 and Ex.1035-Ex.1037.**

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND
WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner

Case IPR2025-00516
U.S. Patent No. 8,601,346

**PATENT OWNER POLARIS POWERLED TECHNOLOGIES, LLC'S
REPLY BRIEF ON DISCRETIONARY DENIAL**

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Case IPR2025-00516
U.S. Patent No. 8,601,346

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I. INTRODUCTION

The Director should exercise discretion to deny institution. Settled expectations strongly favor denial for three reasons. First, the '346 patent issued over *eleven years* ago, and Polaris has owned it since April 2021. Second, Petitioners waited until Polaris relied on its property right before filing a challenge. And third, the patent has been licensed in Petitioners' technology space. Further, the *Fintiv* factors continue to favor discretionary denial. The district court is a better forum to resolve the parties' dispute in this proceeding and the related IPRs.

II. POLARIS HAS SETTLED EXPECTATIONS TO ITS PROPERTY RIGHT IN THE '346 PATENT.

Petitioners' arguments on settled expectations miss the point—settled expectations are *not* based on when a patent was acquired. *Contra* Opp., 18-19. Rather, this factor is concerned with “the length of time the claims have been in force.” Interim Process Memo, 2. Indeed, “the longer the patent has been in force, the more settled expectations should be.” *Dabico Airport Solutions v. AXA Power Aps*, IPR2025-00408, Paper 21 at 3 (P.T.A.B. June 18, 2025).

The '346 patent has been in force since December 3, 2013—well over eleven years. The patent has been publicly available and Petitioners—large, sophisticated technology companies—could have availed themselves of resources, such as the Office's automated search system and publicly available resources, to easily locate the '346 patent. *See Dabico* at 3. And the patent has been licensed in

Petitioners' technology space. *Cf. Intel v. Proxense*, IPR2025-00327, Paper 12 (P.T.A.B. June 26, 2025). Petitioners' failure to file an early challenge to a patent that issued in 2013, waiting instead until Polaris relied on its property right by filing a complaint to enforce its rights, strongly favors denying institution. *See iRhythm Tech. v. Welch Allyn*, IPR2025-00363, Paper 10 (P.T.A.B. June 6, 2025) (denying institution based on settled expectations where Petitioner was aware of patent as early as 2013); *Dabico* (denying institution based on settled expectations; challenged patent in force for almost eight years).

Additionally, Polaris has settled expectations in the two other patents involved in the district court proceeding and challenged in related IPR2025-00515 and -00517. In the -517 IPR, the challenged '968 patent has been in force since October 8, 2013, and Western Digital was aware of it, having cited it in *ten* of its own applications. *See, e.g., -517 IPR*, EX2017.¹ In the -515 IPR, the challenged '085 patent has been in force since November 10, 2015, and SanDisk was aware of

¹ The '968 patent was also cited in at least U.S. Patent Nos. 10,452,278; 10,466,903; 10,509,569; 10,719,267; 10,725,835; 10,817,182; 11,169,704; 11,487,434; and 11,635,898. And in the '835 patent, the Examiner identified the '938 patent as "pertinent art" in an June 26, 2018 Office Action.

that patent, having cited in two of its applications. *See e.g.*, -515 IPR, EX2015.²

All three proceedings warrant denial based on settled expectations.

III. THE *FINTIV* FACTORS FAVOR DENIAL.

Fintiv makes clear that the factors are evaluated holistically “in view of whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv* at 6. Here, the factors favor denial.

The district court’s issuance of a stay should not be weighed strongly against denial here. The parties have an obligation to notify the court “after the PTAB issues **any** rulings” as to the pending IPR within seven days. EX1031, 9. Because the district court has indicated that the stay will be lifted soon after a denial of institution decision, factor 1 weighs, at most, slightly against denial.³

The expected date of the discretionary decision in this IPR is July 27, 2025. If institution is denied, the district court has indicated the stay will be lifted soon

² The ’085 patent was also cited during the prosecution of U.S. 9,411,669.

³ To the extent *Snap v. SRK Tech.*, IPR2020-00820, Paper 15 (P.T.A.B. Oct. 21, 2020) (precedential) dictates that a stay must always be weighed “strongly against” denial—making a “stay” an outcome determinative factor—Polaris requests the Director clarify or reconsider its designation. Weighing one factor as a “super factor” has no place in the balanced assessment. *Cf. Fintiv* at 5.

after denial by ordering the parties to apprise the court within seven days of developments that warrant lifting the stay. *See* EX1031, 9. And prior to the stay, the case was moving faster than initially scheduled (*see* DD. Br., 3-5), making it likely the litigation will resume quickly.

The original trial date was set for June 16, 2026—over 2 months before the FWD. Because it is highly likely the stay will be lifted immediately upon denial, the trial is still likely to occur before, or around, the FWD date of August 27, 2026. In fact, given the accelerated pace of the litigation prior to the stay, the original trial date could even remain in place. Thus, factor 2 weighs in favor of denial.

Factors 3-6 strongly favor denial for the reasons discussed in Polaris’s initial brief. *See* DD. Br. 9-18. Although the district court noted there is more work ahead, that does not negate the substantial investment before the stay—including exchanging claim constructions and related expert reports. And Petitioners have no reasonable excuse here for waiting seven months to file the Petition.

Further, the *Sotera* stipulation should not be considered as Petitioners provide no reason it could not have been submitted earlier (e.g., with the Petition), but instead fault Polaris for filing its brief by the original deadline and not unnecessarily delaying the filing. *See* Opp. 5-7. And the *Sotera* stipulation does not mitigate concerns of duplicate effort because Western Digital relies on system art in its invalidity contentions. *See* Opp. 7 (quoting *Ingenico* to signal it may assert

invalidity based on systems). Even if this IPR is instituted, the district court will still have substantial overlap, and the district court remains a better forum for adjudicating the priority issues of the '968 patent. *See* -517 IPR, Paper 9 at 19-24.

Additionally, the merits remain weak. Despite having Polaris's POPR in hand (which Polaris continues to request the Director consider), Petitioners give short shrift to those arguments and do not even attempt to address most of the weaknesses pointed out by Polaris. *See* Opp. 12-13. Specifically, Petitioners address only the "data blocks" argument in Section III.A of the POPR, but not the arguments in Sections III.B and III.C. *Compare* Opp., 12-13 with POPR, 4-17.

Considered as a whole, the *Fintiv* factors weigh in favor of denial. Five factors strongly favor, or favor, denial; and only one factor slightly weighs against denial. Instituting this IPR would result in duplicative effort and cause additional cost to litigate in two forums. Accordingly, the Director should exercise discretion to deny institution in view of the parallel litigation.

IV. CONCLUSION

Polaris has strong settled expectations that its property right to the claims of the '346 patent—which have been in force for well over eleven years—are enforceable. And because the *Fintiv* factors favor denial, institution of this IPR would be duplicative and an inefficient use of the Board's limited resources. Thus, this proceeding, and the related IPRs, should not be instituted.

Case IPR2025-00516
U.S. Patent No. 8,601,346

Respectfully submitted,

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Case IPR2025-00516
U.S. Patent No. 8,601,346

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

I certify that the above-captioned **PATENT OWNER'S REPLY BRIEF**
ON DISCRETIONARY DENIAL was served in its entirety on June 30, 2025,
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND
WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner,

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner.

IPR2025-00516
U.S. Patent No. 8,601,346

**PETITIONER'S SUR-REPLY BRIEF ON DISCRETIONARY
DENIAL**

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00516 (U.S. Patent 8,601,346)

I. Introduction.

The Director should *not* exercise discretion to deny. Patent Owner has *no* settled expectations because (i) **Patent Owner acquired the '346 patent in August 2022¹** solely for the purpose of litigation—which changes everything with respect to settled expectations; (ii) there is no actual evidence of commercialization, marking, or licensing of the '346 patent, let alone any such activities before the filing of the IPR petition; and (iii) the '346 patent had ***not*** been asserted for over 10 years after its issuance, and the IPR petition was filed within 1 year from its ***first*** assertion in 2024. Further and importantly, the District Court in the parallel litigation has found that “[t]his case is still in early stages of litigation,” and stayed the case because of the benefits of PTAB review for the litigation.

Ex.1031, 4, 5-6.

II. Polaris has *no* settled expectations.

Polaris repeatedly asserts that “the patent has been licensed in Petitioners’ technology space.” PO Reply, 1-2. However, Polaris failed to provide any

¹ Polaris asserts ownership “since April 2021” without any supporting evidence, while the assignment record indicates transfer to Polaris in August 2022. Ex.1021, 1. Either way, the IPR petition was filed within 3-4 years from Polaris’ acquisition, and within 1 year of the first assertion.

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00516 (U.S. Patent 8,601,346)

supporting evidence of such a license, especially **when** the patent was licensed.

There is no public information of recordation of such licenses. There is, however, public information about a lawsuit over these patents between Polaris and Micron² that was filed after the present IPRs were filed, but has since settled. If this is the only license being referenced, it would actually weigh **against** discretionary denial because it happened **after** the filing of the IPR petition. As the Director stated in *Intel-Proxense*:

[P]ersuasive reasons why the Board should review challenged claims several years after their issue date [include as] example, a patent may have been in force for years but may not have been commercialized, asserted, marked, licensed, or otherwise applied in a petitioner's particular technology space, if at all.

IPR2025-00327, Paper 12, 2-3 (P.T.A.B. June 26, 2025).

This example of persuasive reasons applies to the present case: (i) there is no evidence of commercialization, licensing, and marking at all, much less any such activities **before** the filing of the present IPR petitions; and (ii) the first assertion of the '346 patent was over 10 years after its issuance, after Polaris acquired the it in 2022, and the IPR petition was filed within 1 year from the **first** assertion in 2024.

² *Micron Tech. Inc et al. v. Polaris PowerLED Techs., LLC*, No. 1-25-cv-00073 (D. Idaho), filed February 7, 2025 and voluntarily dismissed April 4, 2025.

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00516 (U.S. Patent 8,601,346)

Additionally, Polaris argues that merely because the patent has been publicly available, Petitioner should have considered challenging it earlier. PO Reply, 1.

What Polaris does not point out is that Western Digital and Sandisk combined have had over 10,000 U.S. patent issue since 2010. If on average each of these patents have 25 prior art patent citations, that would be over 250,000 citations. Filing IPRs for even 1/100 of these would be untenable, and in the present case, should have no bearing on settled expectations. In fact, and to the contrary of Polaris' assertion, it would have been an inefficient use of the PTAB's resources to challenge these patents back then, because there was no active litigation. *Google et al. v. Mullen*, IPR2025-00227, Paper 13, 4 ("it is an inefficient use of Board resources to review [a] patent that has been dismissed from the litigation.")

Finally, Polaris's comparison of the already-vacated previously scheduled trial date and a FWD date "upon denial" is non-sensical, because there would be no projected FWD date with denial. PO Reply, 4.

Respectfully submitted,

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Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00516 (U.S. Patent 8,601,346)

PETITIONER'S EXHIBIT LIST

Ex.1001	U.S. Patent No. 8,601,346
Ex.1002	Prosecution History of U.S. 8,601,346
Ex.1003	Declaration of Paul Min under 37 C.F.R. § 1.68
Ex.1004	Curriculum Vitae of Paul Min
Ex.1005	U.S. Patent Publication No. 2011/0078496A1 to Jeddeloh ("Jeddeloh")
Ex.1006	U.S. Patent No. 5,950,225 to Kleiman ("Kleiman")
Ex.1007	U.S. Patent No. 8,341,332 to Ma et al. ("Ma")
Ex.1008	U.S. Patent No. 5,787,460 to Yashiro et al. ("Yashiro")
Ex.1009	U.S. Patent No. 6,161,165 to Solomon et al. ("Solomon")
Ex.1010	Reserved
Ex.1011	The Authoritative Dictionary of IEEE Standards Terms: Seventh Edition; ("IEEE")
Ex.1012	U.S. Patent No. 8,074,149 to Stolowitz ("Stolowitz")
Ex.1013	U.S. Patent No. 8,819,699 to Cota-Robles ("Cota-Robles")
Ex.1014	U.S. Patent No. 6,092,215 to Hodges et al. ("Hodges")
Ex.1015	Complaint, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)
Ex.1016	District Court Trial Statistics
Ex.1017	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00516 (U.S. Patent 8,601,346)

	District Court Litigation, June 22, 2022
Ex.1018	Notice of Sotera Stipulations, Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al. 2:24-cv-02864 (C.D. CA)
Ex.1019	Reserved
Ex.1020	FAQs for Interim Processes for PTAB Workload Management, available at https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management (retrieved May 13, 2025).
Ex.1021	'346 Patent Assignment Recordation
Ex.1022	Plaintiff's Disclosure of Asserted Claims and Infringement Contentions, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA) (Served October 2, 2024)
Ex.1023-1030	Reserved
Ex.1031	Order Granting Defendants' Motion to Stay, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA) (issued June 23, 2025)
Ex.1032	"Chief Patent Board Judge Waves Off Workforce Attrition Concerns," Bloomberg Law, May 7, 2025.
Ex.1033	"PTAB Judges Told To Get Ready For Layoffs," Law 360 (March 21, 2025). https://www.law360.com/articles/2314328/ptab-judges-told-to-get-ready-for-layoffs
Ex.1034	Reserved
Ex.1035	Western Digital Investor Report
Ex.1036	Judge Wright Markman Orders
Ex.1037	"An Assessment of the Impact of the Inter Partes Review Process under the Patent Trial and Appeal Board on the US Economy," The Perryman Group, available at

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00516 (U.S. Patent 8,601,346)

	https://www.perrymangroup.com/publications/report/2021/9/23/an-assessment-of-the-potential-impact-of-expanding-inter-partes-review-ipr-under-the-america-invents-act-on-the-us-economy/

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00516 (U.S. Patent 8,601,346)

CERTIFICATE OF SERVICE

The undersigned certifies, under 37 C.F.R. § 42.6, that service was made on the Patent Owner as detailed below.

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TECHNOLOGIES, INC.,
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v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner.

IPR2025-00517
U.S. Patent No. 8,554,968

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

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PETITIONER'S EXHIBIT LIST

Ex.1001	U.S. Patent No. 8,554,968 to Onufryk et al.
Ex.1002	Prosecution History of U.S. 8,554,968
Ex.1003	Declaration of Paul Min under 37 C.F.R. § 1.68
Ex.1004	Curriculum Vitae of Paul Min
Ex.1005	U.S. Patent Publication No. 2010/0262979 to Borchers et al. ("Borchers")
Ex.1006	PCI Local Bus Specification 3.0 (February 3, 2004) ("PCI")
Ex.1007	PCI Express 2.0 Base Specification Revision 0.9 (September 11, 2006), ("PCIe")
Ex.1008	U.S. Patent Publication No. 2011/0197003 to Serebrin et al. ("Serebrin")
Ex.1009	U.S. Provisional Patent No. 61/301,937, ("Serebrin Provisional"), Ex.1009
Ex.1010	Excerpts from the IEEE Dictionary
Ex.1011	Complaint, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)
Ex.1012	District Court Trial Statistics
Ex.1013	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, June 22, 2022
Ex.1014	Internet Archive – PCI Express
Ex.1015	Internet Archive – PCI
Ex.1016	U.S. Patent Publication No. 2007/0245061
Ex.1017	U.S. Patent No. 7,924,914

IPR2025-00517 Petition
Inter Partes Review of 8,554,968

Ex.1018	U.S. Patent Publication No. 2010/0185719

I. INTRODUCTION

The prior art presented in this Petition describes the same interrupt coalescing technique that is described and claimed in U.S. Patent 8,554,968 (the “’968 patent,” Ex.1001). The ’968 patent relates to communication between a memory controller and a host system. In conventional systems, the host sends read/write commands to the memory controller. *See* Ex.1001, 1:26-35. Upon completing those commands, the memory controller reports a response back to the host. *See id.* The reported responses are then placed into a response queue managed by the host. *See e.g.*, Ex.1005, [0017]. Upon placing an entry into the host’s response queue, the memory controller also sends an interrupt signal to let the host know there is a new item in that response queue for processing. Ex.1005, [0035].

The purported novelty of the ’968 patent is to hold off on sending the interrupt signal until certain conditions (e.g., by a timer or response counter) are met. *See* Ex.1001, 1:38-2:41. But this technique—referred to as interrupt coalescing—was already known as of the filing date of the ’968 patent. *See generally*, Ex.1005. The Borchers reference, describes using a “ResponseNew Counter 280” and a “LastResponse Timer 282” to determine when to send an interrupt signal to the host. Ex.1005, Fig. 2. As shown in this Petition, and supported by the declaration of Dr. Paul Min (Ex.1003), Borchers renders obvious claims 1-18 (hereinafter, the “Challenged Claims”) of the ’968 patent.

Accordingly, pursuant to 35 U.S.C. §§ 311, 314(a), and 37 C.F.R. § 42.100, Petitioner respectfully requests that the Board review and cancel as unpatentable under (pre-AIA) 35 U.S.C. § 103(a) the Challenged Claims of the '968 patent.

II. GROUNDS FOR STANDING

Petitioner certifies that the '968 patent is eligible for IPR and that Petitioner is not barred or estopped from requesting IPR challenging the patent claims. 37 C.F.R. § 42.104(a).

III. NOTE

Petitioner cites to exhibits' original page numbers. Emphasis in quoted material has been added.

IV. BACKGROUND

Dr. Min's declaration provides a background section on memory systems, command and response queues, circular queues, doorbell registers, and interrupt signals that are relevant to the '968 patent. Ex.1003, ¶¶28-41.

V. SUMMARY OF THE '968 PATENT

The '968 patent describes and claims known concepts related to a memory controller that triggers interrupt signals in a host system. The '968 patent relates to communication between a non-volatile memory controller 105 and a host processing unit 110, as shown in Fig. 1 below.

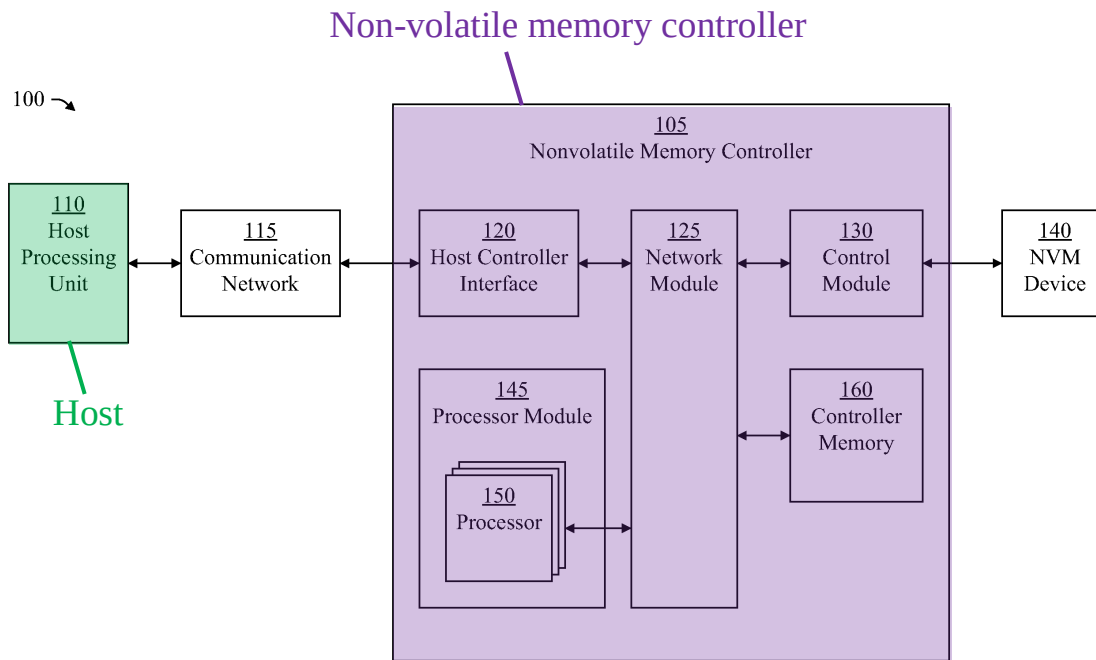


FIG. 1

Ex.1001, Fig. 1 (annotated); Ex.1003, ¶43.

To process read or write commands from the host 110 to the controller 105, the host processing unit 110 “includes submission queues 520 and completion queues 525” shown in Fig. 2. Ex.1001, 9:38-39. “The submission queues 520 store nonvolatile memory commands for controlling operation of the nonvolatile memory controller 105.” Ex.1001, 9:39-41. “The completion queues 525 store completion statuses corresponding to nonvolatile memory commands stored in the submission queues 520.” Ex.1001, 9:41-44. The completion and submission queues are shown in Fig. 5 below.

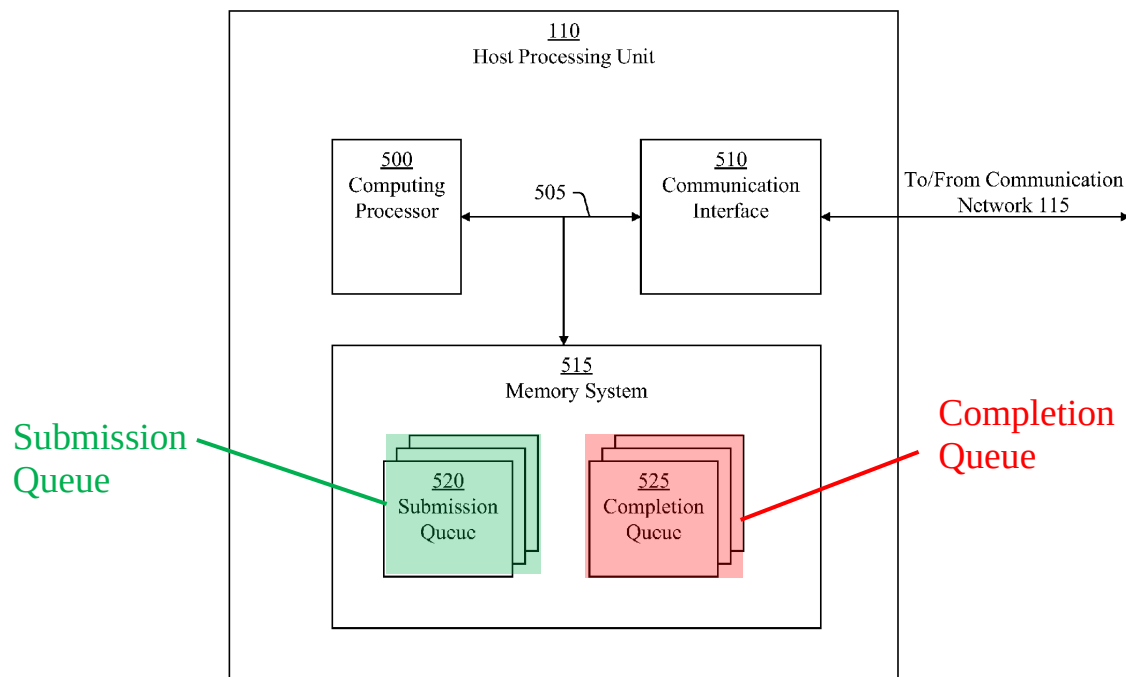


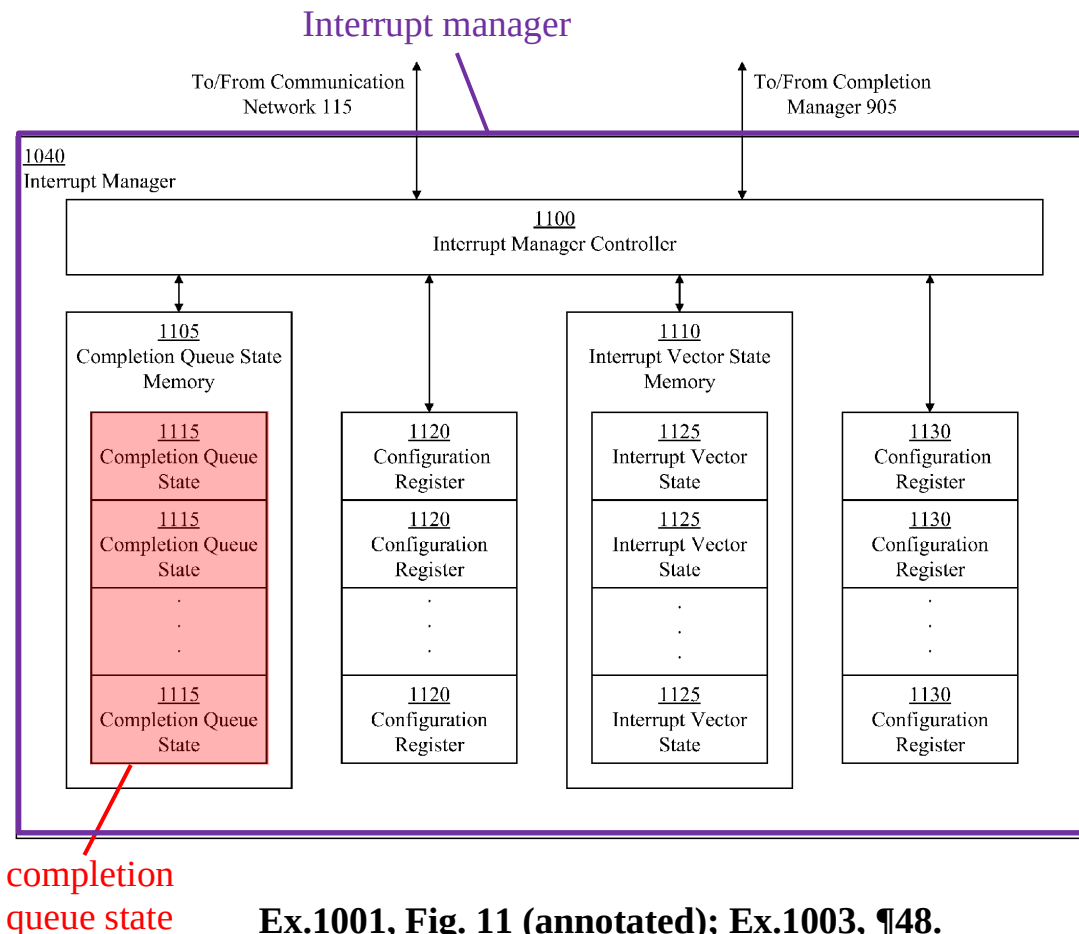
FIG. 5

Ex.1001, Fig. 5 (annotated); Ex.1003, ¶44.

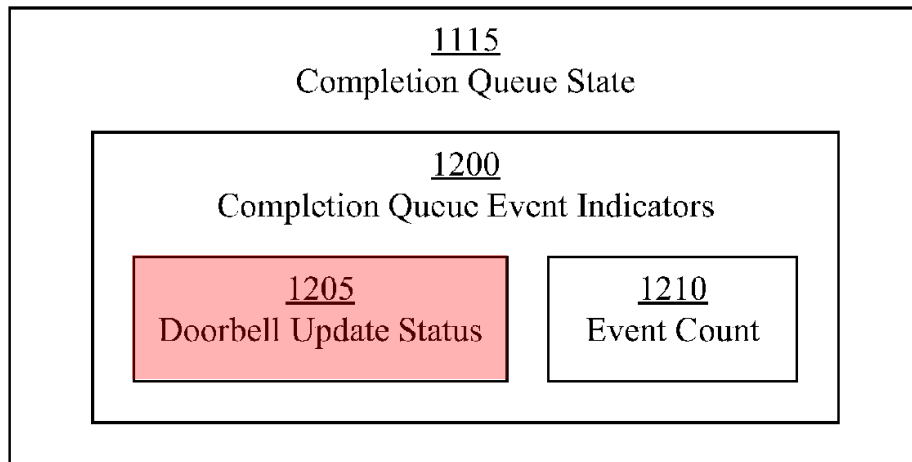
The completion queue is used to manage completion notifications from the memory controller. After the memory controller completes a command, “the host processing unit 110 receives a request packet including a completion status from the host controller ... [and] writes the completion status into the storage location 700 at the tail 710 of the completion queue 525.” Ex.1001, 10:43-48. Then, after being notified through an interrupt signal, “the host processing unit 110 reads completion statuses from storage locations 700 starting at the head 705 of the completion queue 525 to determine the status of the nonvolatile commands associated with the completion statuses that have been processed by the nonvolatile memory controller 105.” Ex.1001, 10:48-53.

To notify the host that there are items within the completion queue to be processed, the memory controller sends an interrupt signal to the host. The claims of the '968 patent are directed to this interrupt process. For example, claim 1 recites “[a] nonvolatile memory controller for alerting a host processing unit to an unprocessed completion status contained in a completion queue of the host processing unit.” The memory controller refrains from sending an interrupt until certain conditions are met.

To determine whether certain conditions are met, the memory controller receives information as to the status of the completion queue. The '968 patent calls this information a “completion queue state.” Claim 1 recites, for example, “an interrupt manager configured to generate a completion queue state for indicating the occurrence of a completion queue event associated with the completion queue.” An interrupt manager 1040 that receives completion queue states 1115 is shown in Fig. 11 below.



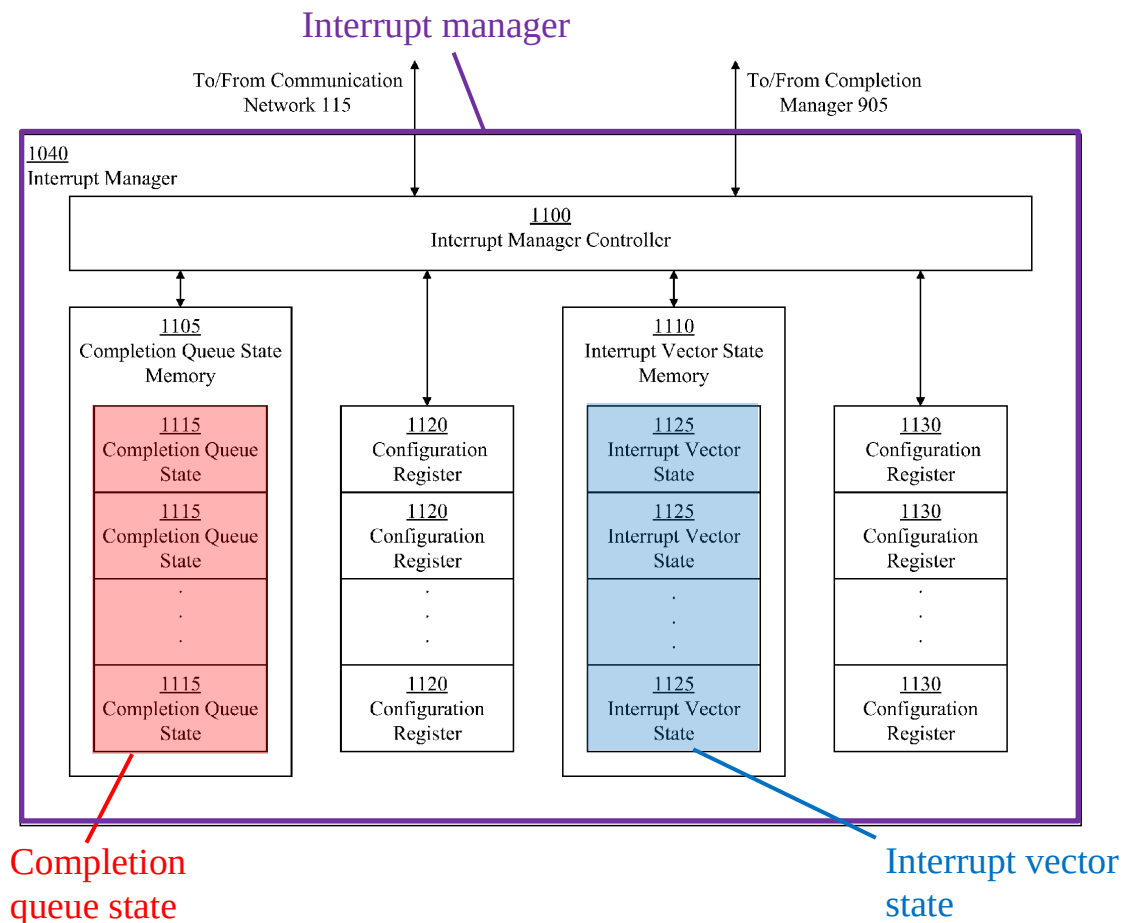
The completion queue state indicates the status of the completion queue. The “interrupt manager 1040 (e.g., the interrupt manager controller 1100) monitors completion queue events and generates completion queue states 1115.” ’968 patent, 15:13-15. Some examples of completion queue states are “completion queue event indicators 1200 [which] include a doorbell update status 1205 and an event count 1210.” Ex.1001, 18:1-2. The doorbell update status 1205 is shown in Fig. 12 below.

**Ex.1001, Fig. 12 (annotated); Ex.1003, ¶49.**

The “doorbell update status 1205 indicates whether the host processing unit 110 has performed a doorbell update event since the last time the interrupt manager 1040 cleared the completion queue state 1115.” Ex.1001, 18:3-6. A doorbell update event is when the host updates the head pointer of the completion queue: “In the doorbell update event, the host processing unit 110 updates the completion queue head pointer 1025 of the completion queue 525 associated with the completion queue state 1115.” Ex.1001, 18:6-10. The doorbell update event concept is claimed as follows: “*and wherein the completion queue state includes a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue.*”

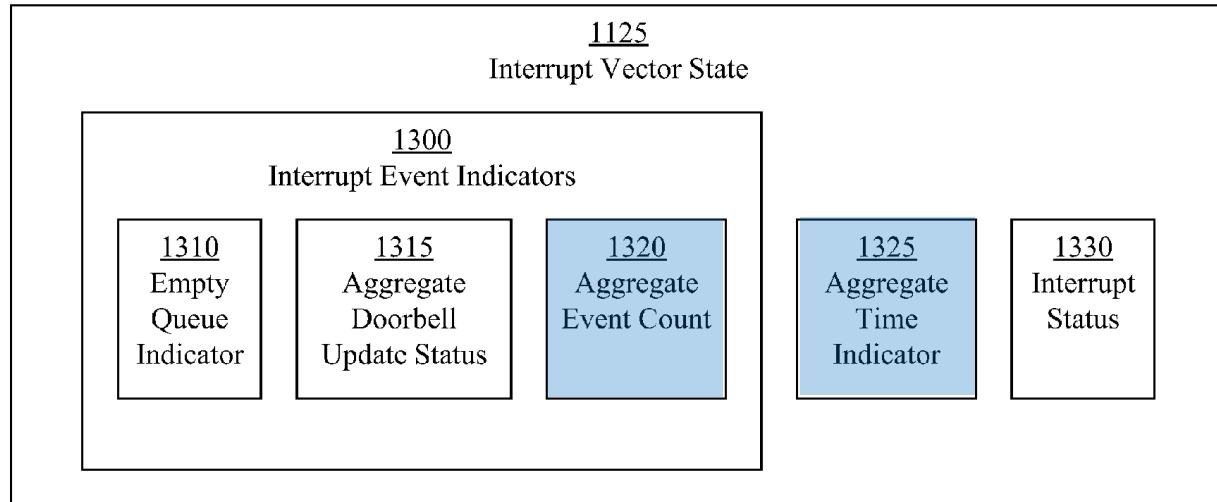
The completion queue state is used by an “*interrupt vector state*” to maintain

the set of conditions for determining whether to generate an interrupt. Ex.1001, 17:21-23. The claims of the '968 patent recite this concept as “*generate an interrupt vector state based on the completion queue state.*” The interrupt vector state is also shown in Fig. 11.



Ex.1001, Fig. 11 (annotated); Ex.1003, ¶51.

The interrupt vector state includes timers and counters, as illustrated in Fig. 13, shown below.

**Ex.1001, Fig. 13 (annotated); Ex.1003, ¶52.**

The aggregate event count 1320 may be used to trigger an interrupt when the number of unprocessed completion packets sent reaches a threshold. See Ex.1001, 19:15-33. “In this way, the interrupt manager 1040 controls a transmission rate of interrupt message packets to the host processing unit 110 based on the aggregate event count threshold.” Ex.1001, 19:28-32. As another example, “[w]hen the aggregate time indicator 1325 is enabled, the interrupt manager 1040 controls a transmission rate of interrupt message packets to the host processing unit 110 based on the aggregate time threshold.” Ex.1001, 19:49-52.

Accordingly, the interrupt vector state is used to determine that there are unprocessed completion events in the completion queue and that the conditions have been met for triggering an interrupt. Claim 1 recites this concept as “*determine the completion queue of the host processing unit contains an*

unprocessed completion status based on the interrupt vector state.” The ’968 patent explains that “[t]he interrupt manager 1040 determines based on the interrupt vector state 1125 whether any completion queue 525 associated with the interrupt vector state 1125 contains an unprocessed completion status.” Ex.1001, 16:3-6. “[T]he interrupt manager 1040 refrains from generating further interrupt message packets unless one or more conditions in the interrupt vector state 1125 are satisfied.” Ex.1001, 16:11-14.

When the conditions are satisfied, “[t]he interrupt manager 1040 transmits the interrupt message packet to the host processing unit 110 through the communication network 115.” Ex.1001, 16:18-20. This concept is recited in claim 1 as “*generate an interrupt message packet for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue.*” Thus, by waiting until certain conditions have been met before sending more interrupt signals, the interrupt manager 1040 performs a technique known as interrupt coalescing.

However, the concept of interrupt coalescing, as well as the other concepts recited in the claims of the ’968 patent, were already known as of the time of filing. Ex.1003, ¶¶42-56.

VI. PROSECUTION HISTORY OF THE ’968 PATENT

The ’968 patent was filed on March 21, 2011 and claims priority to a

provisional application filed August 16, 2010. In a first Office Action, the USPTO rejected several claims based on 25 U.S.C. 112 as being indefinite. Ex.1002, 115-118. There were no prior art rejections. In response, the Applicant amended the claims to address the Office’s 112 rejection. Ex.1002, 136-145.

However, for the reasons explained below, the prior art teaches the interrupt coalescing techniques recited in the ’968 patent. Ex.1003, ¶¶57-63.

VII. LEVEL OF ORDINARY SKILL IN THE ART

A person of ordinary skill in the art (“POSITA”) in the field of the ’968 patent, as of its earliest possible filing date of August 16, 2010, would have been someone knowledgeable and familiar with memory systems. A POSITA would have had a bachelor’s degree in electrical engineering, or an equivalent, and approximately two years of professional working in the field of memory systems. Lack of professional experience can be remedied by additional education, and vice versa. Ex.1003, ¶¶21-23.

VIII. CLAIM CONSTRUCTION

Claim terms in IPR are construed according to their “ordinary and customary meaning” to those of skill in the art. 37 C.F.R. § 42.100(b). Petitioner submits that, for the purposes of this proceeding and the Grounds presented herein, no claim term requires express construction. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Ex.1003, ¶64.

IX. RELIEF REQUESTED AND THE REASONS FOR THE REQUESTED RELIEF

Petitioner asks that the Board institute a trial for *inter partes* review and cancel the Challenged Claims in view of the analysis below.

X. IDENTIFICATION OF HOW THE CLAIMS ARE UNPATENTABLE**A. Challenged Claims**

Petitioner challenges claims 1-18.

B. Statutory Grounds for Challenges

Grounds	Claims	Basis
#1	1-18	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Borchers
#2	1-18	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Borchers and the PCI Standards
#3	1-18	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Borchers, the PCI Standards, and Serebrin

U.S. Patent Publication No. 2010/0262979 to Borchers et al. (“Borchers”) was filed on April 8, 2010 and published on October 14, 2010. Borchers is thus prior art to the ’968 patent under at least (pre-AIA) 35 U.S.C. 102(e).

The PCI standards include the PCI Local Bus Specification Revision 3.0 (Ex.1006) dated February 3, 2004. The PCI standards also include the PCI Express 2.0 Based Specification Revision 0.9 (Ex.1007) dated September 11, 2006. Indeed, the background section of the ’968 patent acknowledges that PCI and PCIe

standards were known. *See* Ex.1001, 1:15-25. Moreover, the '968 patent explains that interrupt signals may comport with the "PCI Specification 3.0" and the "PCIe specification." Ex.1001, 16:61-67. Ex.1003, ¶204.

Dr. Min explains that POSITAs were aware of and relied on the PCI and PCIe standards documents (Ex.1006 and 1007). Ex.1003, ¶205. POSITAs knew that the standards documents could be obtained from the PCI website (www.pcisig.com). *See* Ex.1014; Ex.1015; Ex.1003, ¶206. Additionally, various patents that predate the '968 patent refer to the PCI local bus specification 3.0 and the PCI express specification 2.0. *See* Ex.1016; Ex.1017; Ex.1018; Ex.1003, ¶204.

The PCI standards (Ex.1006 and Ex.1007) are thus printed publications that were publicly available and known to POSITAs before the filing date of the '968 patent. Ex.1003, ¶¶201-06. Accordingly, the PCI standards are prior art to the '968 patent under (pre-AIA) 35 U.S.C. 102(b).

U.S. Patent Publication No. 2011/0197003 to Serebrin et al. ("Serebrin," Ex.1008) was filed on December 6, 2010. Serebrin claims priority to provisional application 61/301,937 (Ex.1009) filed February 5, 2010. The Serebrin provisional application is nearly identical to the specification of the Serebrin publication and provides support for at least one claim. *See Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1380 (Fed. Cir. 2015). As such, Serebrin is entitled to its provisional filing date and is prior art to the '968 patent under pre-AIA 35

U.S.C. 102(e).

C. Ground 1: Claims 1-18 are obvious in view of Borchers.

1. Summary of Borchers.

Borchers, like the '968 patent, describes techniques for interrupt coalescing. Borchers describes communication between a host 106 and a controller board 102 of a data storage device 100, as shown in Fig. 1 below.

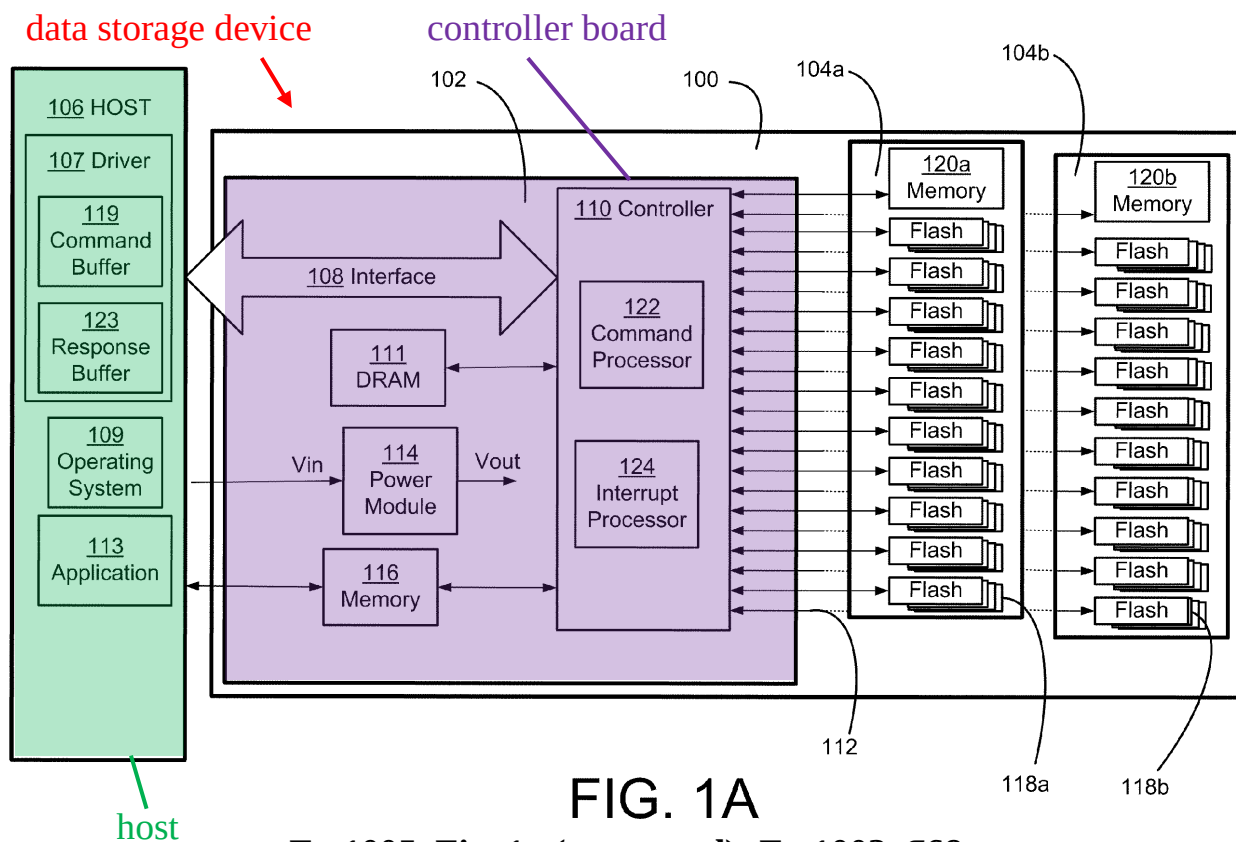
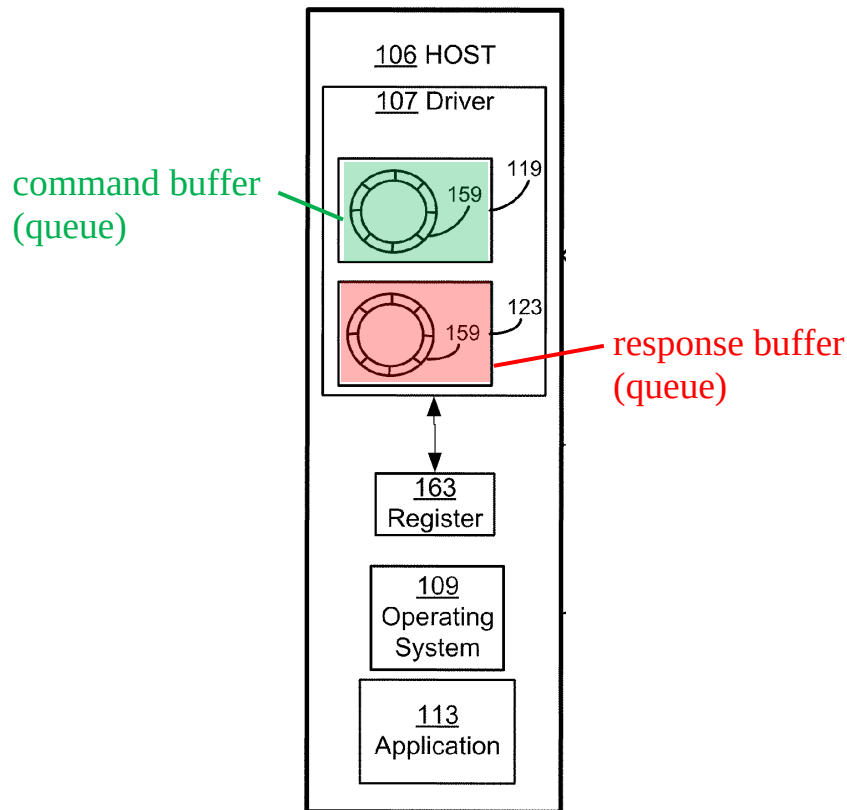


FIG. 1A
Ex.1005, Fig. 1a (annotated); Ex.1003, ¶68.

Like the '968 patent, the host includes two queues: a command buffer (queue) 119 and a response buffer (queue) 123. The response buffer 123 “is populated with responses by the data storage device for retrieval by the host

device.” Ex.1005, [0004]. “The response buffer 123 also can be configured as a circular queue.” Ex.1005, [0030].



Ex.1005, Fig. 1c (partial, annotated); Ex.1003, ¶69.

Borchers explains that “[e]ach of the circular queues 159 of the command buffer 119 and the response buffer 123 include a head pointer and a tail pointer.” Ex.1005, [0030]. “Commands and responses may be inserted into the circular queue 159 at the tail pointer and removed at the head pointer.” Ex.1005, [0030]. For example, when the host seeks to read or write to memory, “[t]he host 106 may write a command to the command buffer 119 and update the command tail

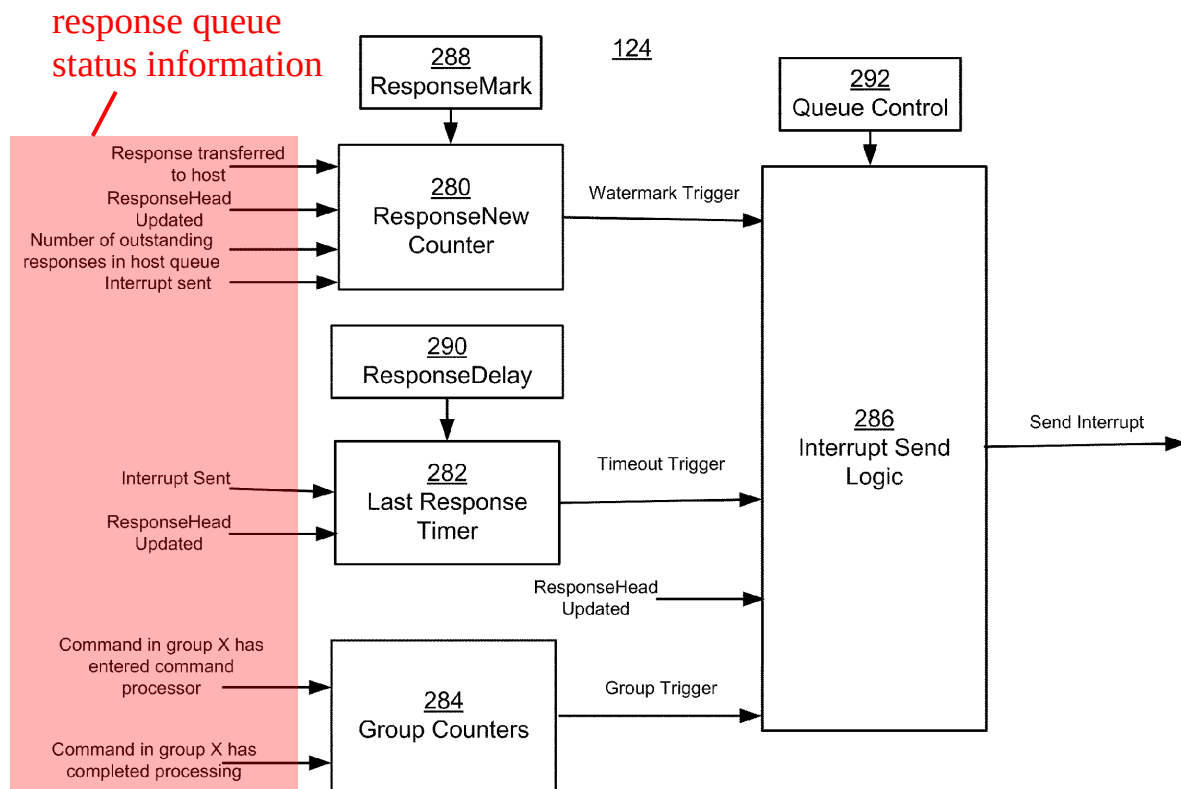
pointer.” Ex.1005, [0034]. Then, when the memory controller is ready to process those commands, it will “read the command out of the command buffer 119 [and] update the head pointer ... to indicate to the host 106 that the command processor 122 has received the command.” Ex.1005, [0034].

After the memory controller has processed a command, it sends a response command back to the host. It does so by writing “a response to the host” at the tail end of the response queue. Ex.1005, [0035]. The memory controller then “updates the response tail pointer ... to indicate that the command is finished.” Ex.1005, [0035].

In some examples, “[t]he interrupt processor 124 is configured to signal the host 106 with an interrupt when new responses are available in the response buffer 123.” Ex.1005, [0035]. However, in some cases, the controller may refrain from sending an interrupt until certain conditions have been met (i.e., interrupt coalescing). In particular, “the host 106, through its driver 107, may control when the interrupt processor 124 should generate interrupts.” Ex.1005, [0036].

To determine whether to send interrupts, the memory controller receives information that indicates the status of the response queue. This response queue status information may include “when a packet is transferred to the host 106, when the ResponseHead is updated, the number of outstanding responses in the host response buffer 123 and when an interrupt has been sent.” Ex.1005, [0060].

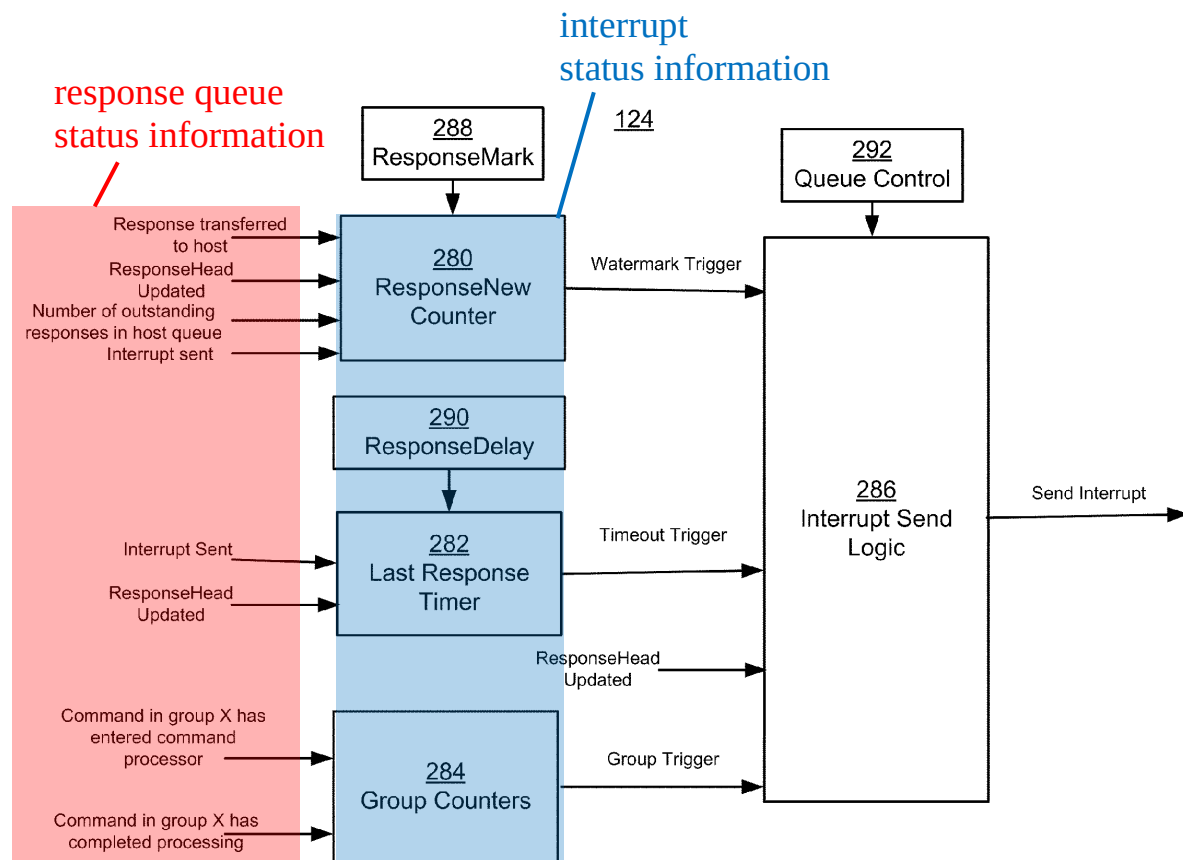
Determining whether the ResponseHead (head pointer of the response queue) has been updated is referred to as a doorbell status update. *See e.g.*, Ex.1006, 308.



Ex.1005, Fig. 2 (annotated); Ex.1003, ¶73.

The response queue status information can then be used to determine the status of interrupt mechanisms, which keep track of the conditions used to trigger an interrupt. For example, Borchers explains that the response queue status information can be used to update a ResponseNew Counter 280. “The ResponseNew Counter 280 is configured to track the number of responses transferred to the host 106 that the host has yet to process.” Ex.1005, [0060].

“When the counter 280 reaches or exceed the watermark level set by the host 106, i.e., the ResponseMark 288, then a watermark trigger is generated and sent to the interrupt send logic 286.” Ex.1005, [0060]. Borchers also describes other interrupt mechanisms such as a timer 282 or a group counter 284. As illustrated in Fig. 2 below, these interrupt mechanisms maintain status information (i.e., count of responses or time since last response).



Ex.1005, Fig. 2 (annotated); Ex.1003, ¶74.

Accordingly, as will be explained in detail in the analysis below, Borchers describes the same interrupt coalescing technique described in the '968 patent.

Borchers uses the state of the response queue (“*completion queue state*”) to update interrupt status information (“*interrupt vector state*”). That interrupt status information keeps track of the conditions for triggering an interrupt signal. When those conditions are met (i.e., a watermark or expired timer), then the interrupt signal is sent. Ex.1003, ¶¶68-76.

2. The PCI Standards Represent Background Knowledge of a POSITA.

The PCI Standards represent the background knowledge of a POSITA because their subject matter is critical for designing memory systems that are compliant with industry standards. Given that the PCIe standard is “an enhancement to the PCI architecture” which was “the most widely accepted and implemented expansion standard in the world” as of 2004 (Ex.1007, 21; Ex.1006, 15), POSITAs in the field of memory systems would have been familiar with their teachings and would have sought to design their memory systems in accordance with such standards. Ex.1003, ¶77.

3. Claim 1

The present Ground describes how the challenged claims are obvious over a single reference, Borchers, with additional reference to the PCIe Standard, which is explicitly called out in Borchers. Grounds 2 and 3 present alternative challenges for the claims based on Borchers in view of the PCIe Standard (Ground 2), and

further in view of Serebrin (Ground 3).

[1.0] A nonvolatile memory controller for alerting a host processing unit to an unprocessed completion status contained in a completion queue of the host processing unit, the nonvolatile memory controller comprising:

The language that comes after the phrase “A *nonvolatile memory controller for ...*” of the preamble [1.0] describes a purpose, or intended use, of the controller. To the extent that the preamble is deemed limiting, Borchers teaches the entire preamble.

First, Borchers describes a controller board 102 (“*non-volatile memory controller*”) for a data storage device 100 that stores data for a host 106 (“*host processing unit*”). “FIG. 1A illustrates a block diagram of a data storage device 100 and a host 106. The data storage device 100 may include a controller board 102 and one or more memory boards 104a and 104b.” Ex.1005, [0018]. “The controller board 102 may include a controller 110, a DRAM 111, multiple channels 112, a power module 114, and a memory module 116.” Ex.1005, [0019].

Fig. 1A is shown below.

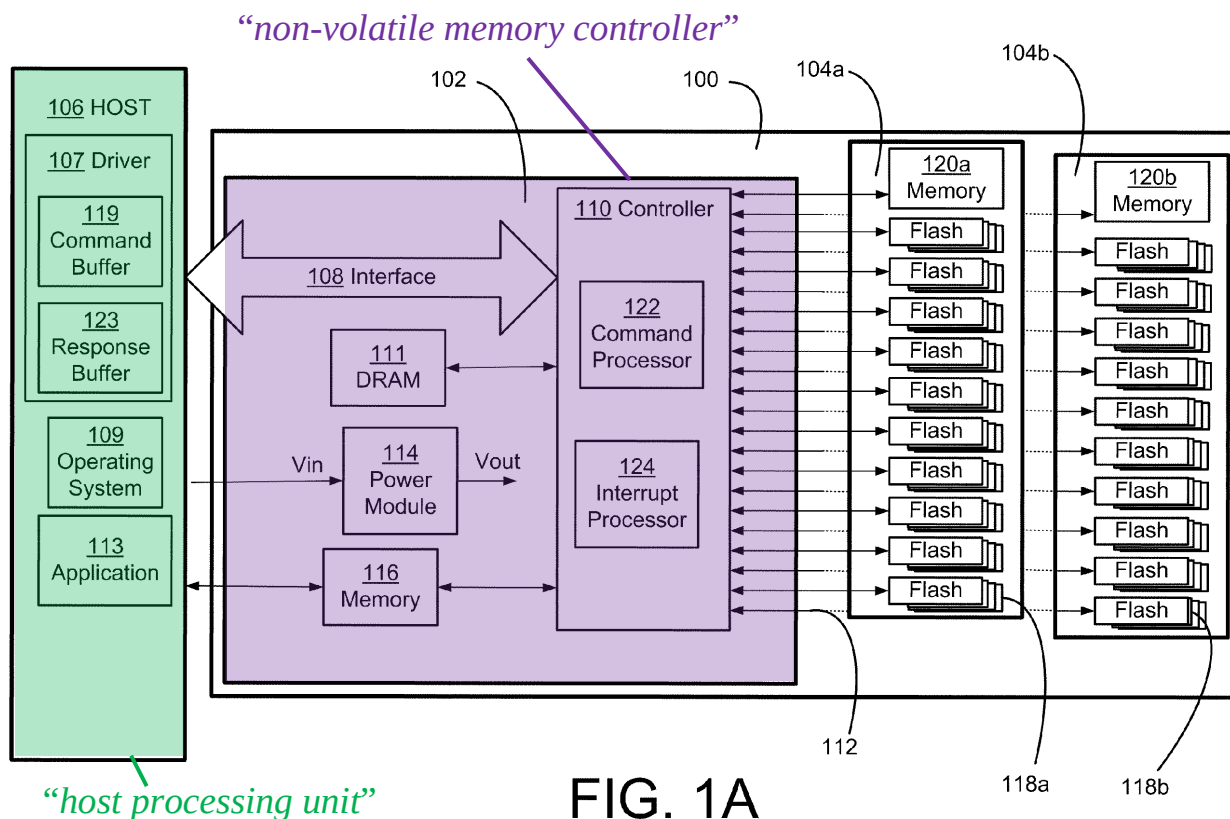


FIG. 1A
Borchers, Fig. 1a (annotated); Ex.1003, ¶79.

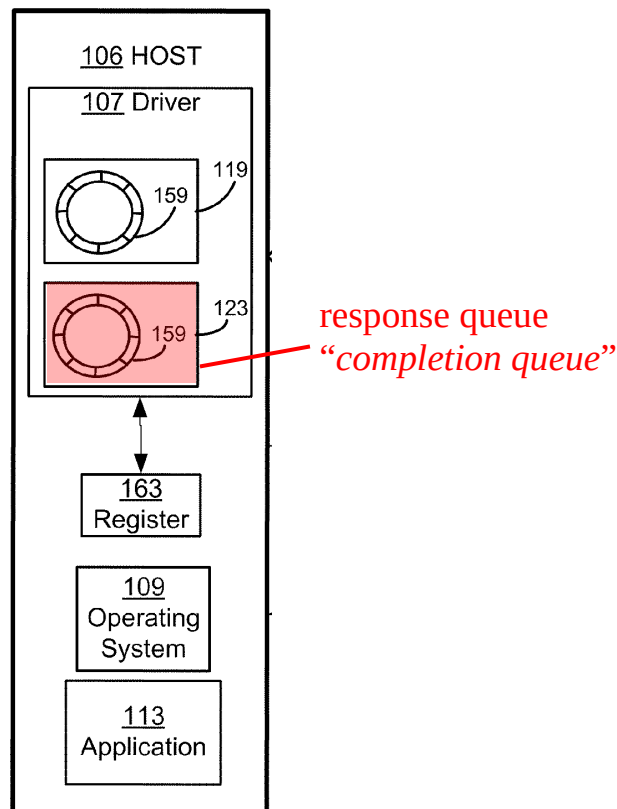
Borchers' controller board 102 is a non-volatile memory controller because it is responsible for controlling flash memory. Ex.1005, [0019]. Fig. 1A illustrates the memory devices 104a as flash memory and explains that "the memory boards 104a and 104b may include multiple flash memory chips 118a and 118b on each of the memory boards." Ex.1005, [0019]; *see also* Ex.1005, [0125]. Flash memory is described as a non-volatile type of memory. Ex.1005, [0128] ("**forms of non-volatile memory**, including by way of example semiconductor memory devices, e.g., EPROM, EEPROM, and **flash memory devices**"). Accordingly, because the controller board 102 serves as a controller for non-volatile flash memory, it is a

“*nonvolatile memory controller*” as claimed.

Furthermore, Borchers’ host 106 is a “*host processing unit*” because it processes instructions from an application. “The application 113 may be operably coupled to the operating system 109 and/or to the driver 107. The application 113 may generate the commands and communicate the commands to the operating system 109.” Ex.1005, [0020].

Second, the host 106 (“*host processing unit*”) includes a response buffer 123¹ (“*completion queue*”). “For example, a command buffer 119 may be used for commands and a response buffer 123 may be used for responses or results to the commands.” Ex.1005, [0027]. The response queue 123 may be “configured as a circular queue.” Ex.1005, [0030]. Fig. 1C (partial) is shown below.

¹ In, Borchers, “the terms **buffer** and **queue** are used interchangeably.” Borchers, [0027].



Ex.1005, Fig. 1c (partial, annotated); Ex.1003, ¶83.

The response queue 123, like the claimed completion queue, receives completion responses from the memory controller board 102. “For example, a command buffer 119 may be used for commands and **a response buffer 123 may be used for responses or results to the commands.**” Ex.1005, [0027]. “When the command processor 122 **completes** the command, **the command processor 122 writes a response to the host** using a DMA operation **and updates the response tail pointer** with another DMA operation to indicate that the command is finished.” Ex.1005, [0035].

Borchers explains that the response queue uses the producer-consumer

model. *See* Ex.1005, [0030]. “The host 106 may be ... the consumer of the response buffer 123. The data storage device 100 may be the producer of the response buffer 123.” Ex.1005, [0030]. In other words, the “data storage device 100 may write the command head pointer and the response tail pointer and may read the command tail pointer and the response head pointer.” Ex.1005, [0030].

Accordingly, because the response queue stores the notifications of completed commands, it is a “*completion queue*” as claimed. Borchers’ response queue performs a similar function as does the completion queue described in the ’968 patent. *Compare* Ex.1005, [0030]-[0035] *with* Ex.1001, 10:43-53.

Third, the non-volatile memory controller is configured to alert the host processing unit when there are new (i.e., unprocessed) events in the response queue (“*alerting a host processing unit to an unprocessed completion status contained in a completion queue*”). Borchers explains that the “interrupt processor 124 is configured to signal the host 106 with an interrupt when new responses are available in the response buffer 123.” Ex.1005, [0035].

Thus, because Borchers describes a non-volatile memory controller that alerts a host when there are new items in a response queue, Borchers renders this claim element obvious, to the extent the preamble is limiting. Ex.1003, ¶¶78-87.

[1.1] an interrupt manager configured to generate a completion queue state for indicating the occurrence of a completion queue event associated with the completion queue,

First, Borchers' memory controller board 102 includes an interrupt processor 124 (*"interrupt manager"*). "The controller board 102 may include a controller 110." Ex.1005, [0019]. "The controller 110 may include a command processor 122 and an interrupt processor 124." Ex.1005, [0019].

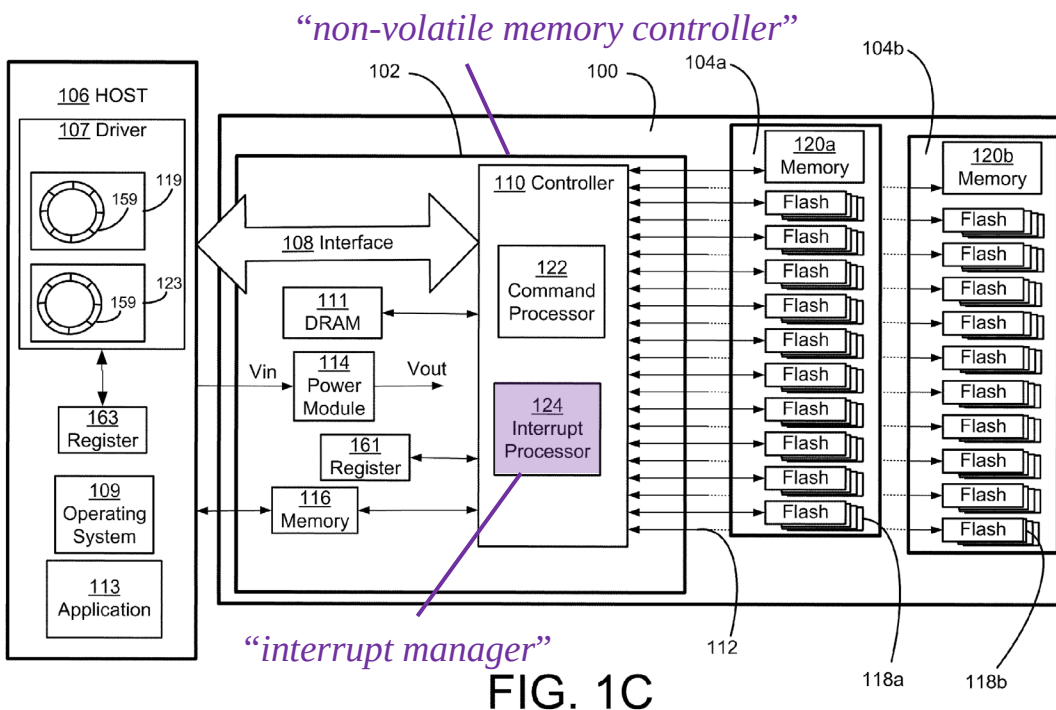


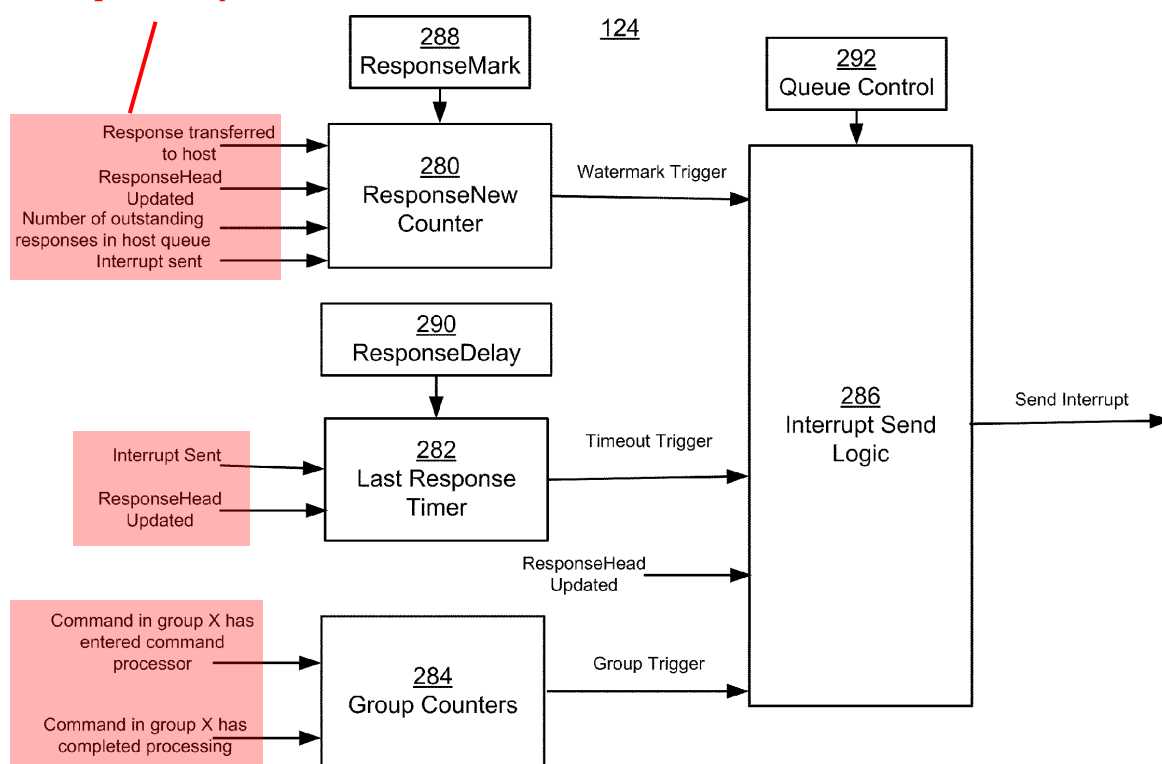
FIG. 1C

Ex.1005, Fig. 1C (annotated); Ex.1003, ¶88.

Second, Borchers' interrupt processor 124 (shown in detail in Fig. 2) receives information from the host system as to the status of the response queue (*"completion queue"*). To *"indicate[] the occurrence of a completion queue event associated with the completion queue,"* the response queue status information includes an updated response queue head pointer, and the number of outstanding

items in the response queue: “The ResponseNew counter 280 receives as inputs information including when a packet is transferred to the host 106, when the ResponseHead is updated, the number of outstanding responses in the host response buffer 123 and when an interrupt has been sent.” Ex.1005, [0060].

“completion queue state”



Ex.1005, Fig. 2 (annotated); Ex.1003, ¶89.

Accordingly, because the updated head pointer and updated number of outstanding responses indicates the status of the response queue (“completion queue”) that information is a “completion queue state” as claimed. In other words, the updated head pointer and updated number of outstanding responses “indicat[e]

the occurrence of a completion queue event associated with the completion queue.

The status information received and relied upon by the interrupt controller 124 “*indicat[es] the occurrence of a completion queue event associated with the completion queue*” as claimed. For example, an update to the head pointer of the response queue is a “*completion queue event associated with the completion queue*” because it is an event that directly affects and relates to the response queue (“*completion queue*”).

Further, the information received by the interrupt processor (i.e., “when the ResponseHead is updated” or “the number of outstanding responses in the host response buffer”) represents a “*completion queue state*” because it represents the *status* of the completion queue.

This status information is “*generate[d]*” by the interrupt processor when it is received and/or stored by Borchers’ interrupt processor 124 as illustrated in Fig. 2. To the extent the claims are interpreted such that the *completion queue state* is to be stored, a POSITA would understand that Borchers’ status information would be stored in some type of memory such as a buffer, register, flag, or other form of storage.² In other words, a POSITA would have recognized that Borchers’

² Ex.1003, ¶93. Note that Ground 3 presents an alternative obviousness challenge for this point.

response queue status information (“*completion queue state*”) is not merely transitory signals. Rather, a POSITA would have recognized that the response queue status information would be stored somewhere by the interrupt processor until such information was needed or ready to be processed. Ex.1003, ¶93. Indeed, it was known for memory controllers and interrupt managers to use such types of storage. *See e.g.*, Ex.1008, Figs. 2 & 5, [0057], [0090]-[0091]; Ex.1009, Figs. 2 & 5, [0051], [0083], [0084] (describing how an interrupt manager uses various forms of memory such as cache or registers to store state information). And a POSITA would have found it obvious for the response queue status information to be generated/stored by the interrupt processor given that the ResponseHead being updated is on the controller side: “The command tail pointer and the response head pointer may be stored in registers of the data storage device.” Ex.1005, [0031]; Ex.1003, ¶93. Accordingly, because Borchers’ interrupt processor receives and uses the response queue status information, the interrupt processor “*generate[s]*” a “*completion queue state*” as claimed.

Thus, because Borchers’ interrupt manager receives and uses information as to the status of the response queue, Borchers renders this limitation obvious. Ex.1003, ¶¶88-94.

[1.2] *generate an interrupt vector state based on the completion queue state,*

First, Borchers’ interrupt processor generates an “*interrupt vector state*” by

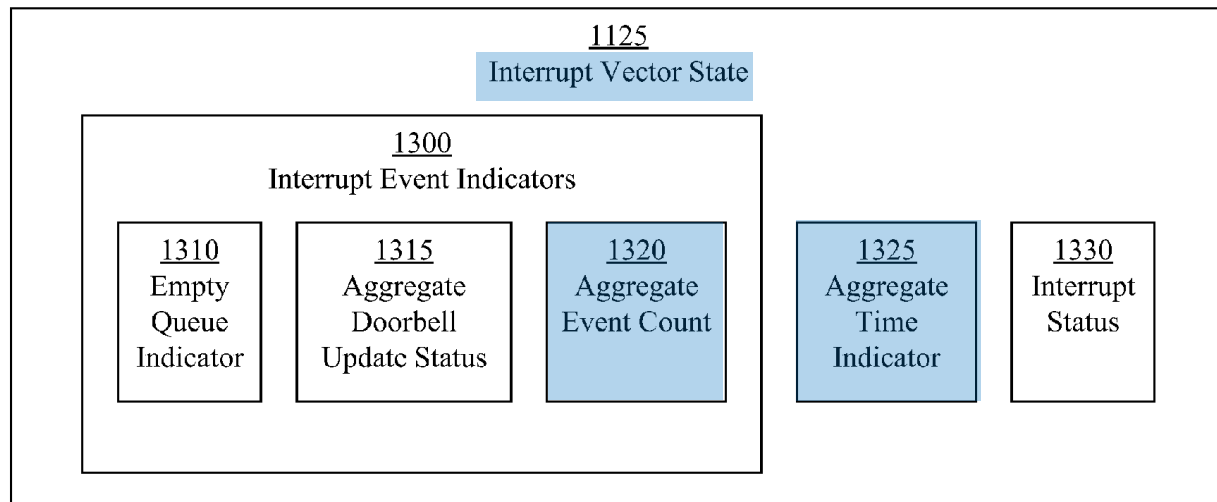
maintaining a set of conditions that determine whether to send an interrupt signal. These set of conditions are maintained by various interrupt mechanisms including “a ResponseNew counter 280, a last response timer 282, group counters 284 and interrupt send logic 286.” Ex.1005, [0059].

The ResponseNew Counter 280, for example, “is configured to track the number of responses transferred to the host 106 that the host has yet to process.” Ex.1005, [0060]. “When the counter 280 reaches or exceed the watermark level set by the host 106, i.e., the ResponseMark 288, then a watermark trigger is generated and sent to the interrupt send logic 286.” Ex.1005, [0060]. If the count is less than the threshold, an interrupt is not sent. Ex.1003, ¶96.

The last response timer 282, for example, is “configured to keep track of time since the last interrupt.” Ex.1005, [0062]. “In one exemplary implementation, the ResponseDelay 290 timeout may be the number of microseconds since the last interrupt, or since the last time that the host 106 removed new responses from the response buffer 123, before an interrupt is generated.” Ex.1005, [0062].

The group counters 284 track the number of unprocessed responses for a number of response queues so that an interrupt can be sent for the whole group. See Ex.1005, [0066]. “**In this manner, an interrupt is not generated for each of the individual commands but only for the group of commands.**” Ex.1005, [0066].

Accordingly, because the interrupt processor generates counters and timers (by incrementing the counters and tracking time) for determining whether to send an interrupt signal, Borchers' interrupt processor is configured to generate an “*interrupt vector state*” as claimed. Notably, the interrupt mechanisms of Borchers, which include timers and counters, are similar to how the '968 patent describes the interrupt vector states.



Ex.1001, Fig. 13 (annotated); Ex.1003, ¶99.

As can be seen from Fig. 13 of the '968 patent, the interrupt vector state includes items such as an aggregate event count 1320 or an aggregate time indicator 1325. The aggregate event count 1320 may be used to trigger an interrupt when the number of unprocessed completion packets sent reaches a threshold. See Ex.1001, 19:15-33 (“In this way, the interrupt manager 1040 controls a transmission rate of interrupt message packets to the host processing unit 110

based on the aggregate event count threshold.”). As another example, “[w]hen the aggregate time indicator 1325 is enabled, the interrupt manager 1040 controls a transmission rate of interrupt message packets to the host processing unit 110 based on the aggregate time threshold.” Ex.1001, 19:49-52.

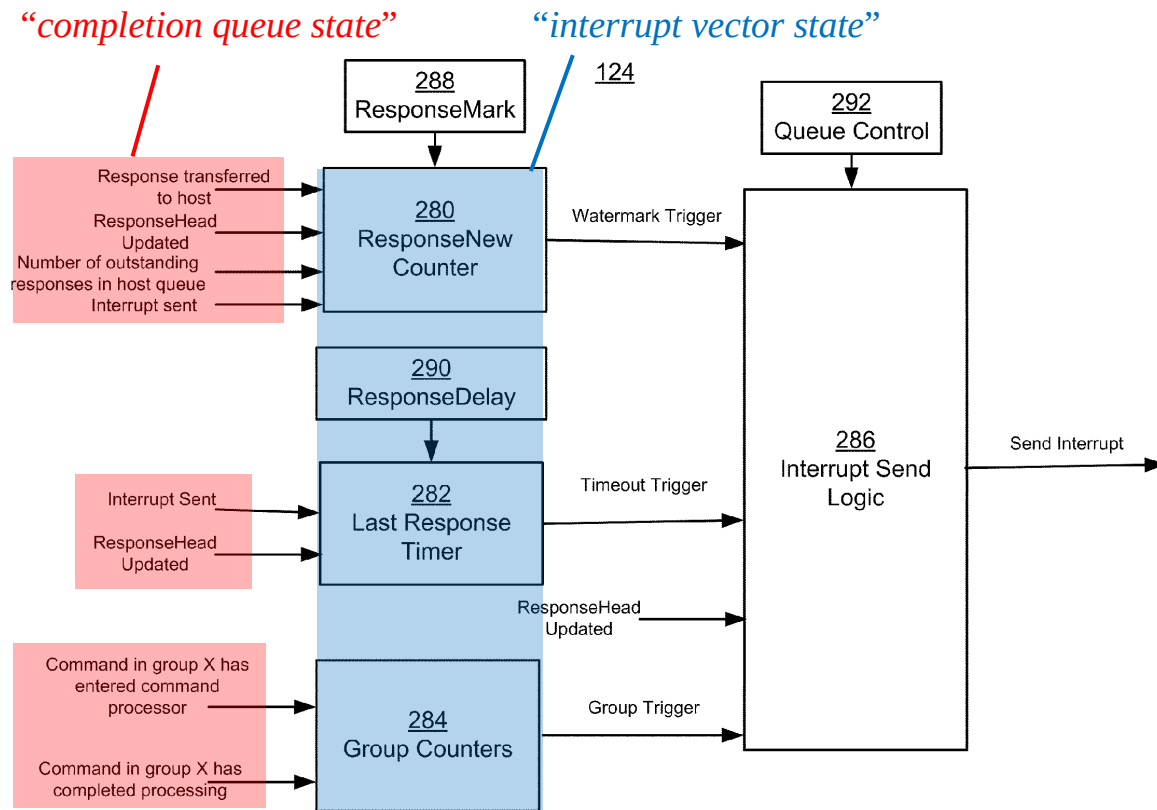
Thus, Borchers’ ResponseNew Counter 280 and last response timer 282 are analogous to the aggregate event count 1320 and aggregate time indicator 1325 which are examples of interrupt vector states described in the ’968 patent.

Second, Borchers’ interrupt mechanisms (e.g., ResponseNew Counter 280, last response timer 282, and group counters) teach an “*interrupt vector state*”. Specifically, Borchers teaches an embodiment in which its memory interface “include[s] a PCIe interface.” Ex.1005, [0110]. It was known that the PCIe standard was required to support Message Signaled Interrupts (MSI), which use interrupt vectors. *See* Ex.1007, 341 (“PCI Express requires support of MSI or MSI-X or both.”) “Message Signaled Interrupts (MSI)” includes “the message address and message data (from here on referred to as the “vector”).” Ex.1006, 231.

A POSITA would have thus recognized based on background knowledge that Borchers’ interrupt signals—as part of a PCIe interface—would be MSI signals that use interrupt vectors. Accordingly, the interrupt mechanisms that maintain the set of conditions for determining whether to send an interrupt signal teach an “*interrupt vector state*” as claimed. Again, Borchers’ interrupt mechanism

are analogous to the interrupt vector state described in the '968 patent. See Ex.1001, 19:15-52.

Third, Borchers' interrupt mechanisms such as timers and counters (“*interrupt vector state*”) are based on the response queue status information (“*completion queue state*”) because they receive the completion queue state information as inputs. For example, the “ResponseNew counter 280 receives as inputs information including when a packet is transferred to the host 106, when the ResponseHead is updated, the number of outstanding responses in the host response buffer 123 and when an interrupt has been sent.” Ex.1005, [0060].

**Ex.1005, Fig. 2 (annotated); Ex.1003, ¶104.**

Accordingly, because the interrupt mechanisms (e.g., timers and counters) (“*interrupt vector state*”) receive information (“*completion queue state*”) as to the status of the response queue (“*completion queue*”), Borchers’ interrupt mechanisms are generated “*based on*” that information. The interrupt mechanism information is *generated* when the timers or counters are updated. In some examples, the values of the timers or counters may be stored in a register. Indeed, a POSITA would have found it obvious for Borchers’ interrupt mechanism information to be stored in some type of memory such as a buffer, register, flag, or other form of storage. Ex.1003, ¶105. In other words, a POSITA would have

recognized that the timers and counters of the interrupt mechanisms (“*interrupt vector state*”) are not merely transitory signals. Indeed, it was known for memory controllers and interrupt managers to use such registers or caches for storage. See *e.g.*, Ex.1008, Figs. 2 & 5, [0057], [0090]-[0091]; Ex.1009, Figs. 2 & 5, [0051], [0083], [0084]] (describing how an interrupt manager uses various forms of memory such as cache or registers to store state information). Accordingly, because Borchers’ interrupt processor receives and uses the response queue status information to update the interrupt mechanism timers and counters, Borchers’ interrupt processor “*generate[s]*” an “*interrupt vector state*” as claimed.

Thus, because Borchers’ interrupt processor uses counters and timers to maintain the set of conditions used to determine whether to send an interrupt, and the counters or timers are updated with information as to the status of the response queue, Borchers renders this limitation obvious. Ex.1003, ¶¶95-107.

[1.3] *determine the completion queue of the host processing unit contains an unprocessed completion status based on the interrupt vector state, and*

First, as described above at [1.0], Borchers’ host unit includes a response queue (“*completion queue of the host processing unit*”).

Second, Borchers’ ResponseNew Counter 280 (“*interrupt vector state*”) “is configured to track the number of responses transferred to the host 106 that the host has yet to process” (“*unprocessed completion status*”). Ex.1005, [0060].

“Each time a response is transferred to the response buffer 123 the counter is incremented.” Ex.1005, [0060]. Accordingly, the ResponseNew counter 280 indicates the number of unprocessed events in the response queue (“*completion queue*”). “If the count of new responses in the response buffer 123 is equal to or greater than the ResponseMark, then an interrupt is generated by the interrupt processor 124 and the count is zeroed.” Ex.1005, [0037]. Accordingly, the interrupt processor determines there are unprocessed completion statuses in the response queue (“*the completion queue of the host processing unit*”) “based on” the receipt of the number of outstanding responses in the response queue by the ResponseNew counter (part of the “*interrupt vector state*”).

Thus, because the ResponseNew Counter 280 (an “*interrupt vector state*”) tracks the number of responses the host has yet to process, Borchers renders this limitation obvious. Ex.1003, ¶¶108-12.

[1.4] generate an interrupt message packet for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue, and

First, as explained above at [1.0], Borchers’ system sends an interrupt to alert the host processing unit of the unprocessed completion status in the response queue (“*completion queue*”). “The interrupt processor 124 is configured to signal the host 106 with an interrupt when new responses are available in the response buffer 123.” Ex.1005, [0035]. “The interrupt processor 124 is configured to signal

the host 106 with an interrupt when new responses are available in the response buffer 123.” The interrupt signal received by the host then causes the host to process the interrupt, thereby “*triggering the interrupt in the host processing unit.*” See e.g., Ex.1005, [0050] (“an interrupt may be received by an interrupt handler 225a-225n”).

Second, a POSITA would have found it obvious for Borchers’ interrupt signal to be an “interrupt message packet” consistent with PCI/PCIe standards. Ex.1003, ¶114. Borchers teaches an embodiment in which its memory interface “include[s] a PCIe interface” ([0110]), and as noted previously, the PCIe standard “requires” Message Signaled Interrupts (MSI) (see Ex.1006, 231, 249).

Accordingly, it would have been obvious to a POSITA that when Borchers describes sending interrupt signals, those signals would be embodied as MSI or MSI-X interrupts consistent with the PCI/PCIe standards. Borchers’ interrupt signals—embodied as MSI or MSI-x interrupts—are therefore “*interrupt message packets.*” Such MSI or MSI-x interrupt signals are within the scope of the claims. Indeed, the ’968 patent similarly describes the interrupt message packets as being MSI or MSI-x interrupts: “In some embodiments, the hardware interrupt generated in the host processing unit 110 is a message signal interrupt (MSI) or an extended message signal interrupts (MSI-X) as defined in the PCI Specification 3.0.” Ex.1001, 16:61-64.

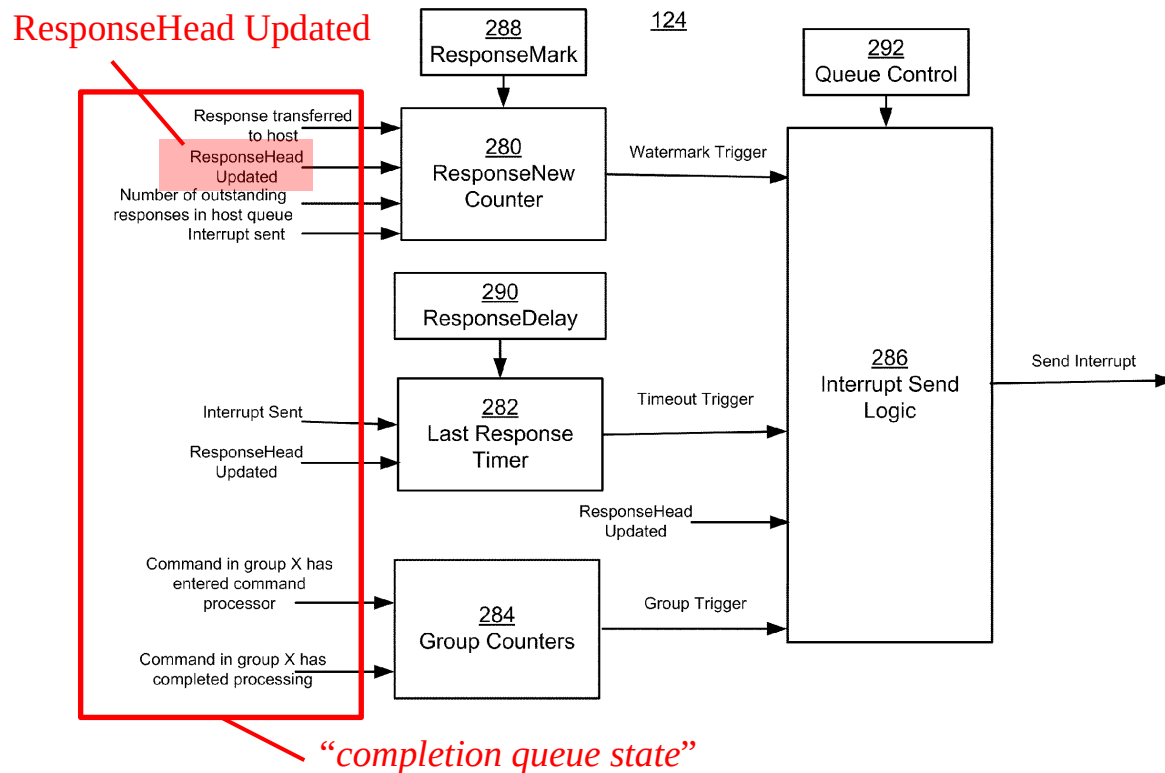
Thus, because Borchers' interrupt manager sends an interrupt signal to alert the host that there are unprocessed events in the response queue, Borchers renders this limitation obvious. Ex.1003, ¶¶113-16.

[1.5] wherein the completion queue state includes a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue.

First, as mentioned above at [1.1], Borchers' interrupt processor receives response queue status information ("*completion queue state*") from the host.

Second, Borchers' response queue status information ("*completion queue state*") indicates whether the host processing unit has updated the response head pointer ("*the host processing unit updates a head pointer*"). As explained above at [1.1], Borchers' interrupt processor 124 receives as information from the host system "when the ResponseHead is updated." Ex.1005, [0060].

During operation, "[t]he host 106 is configured to read the responses from the response buffer 123 and **update the head pointer** in the MMIO space of the data storage device to indicate that the host has received the response." Ex.1005, [0035].



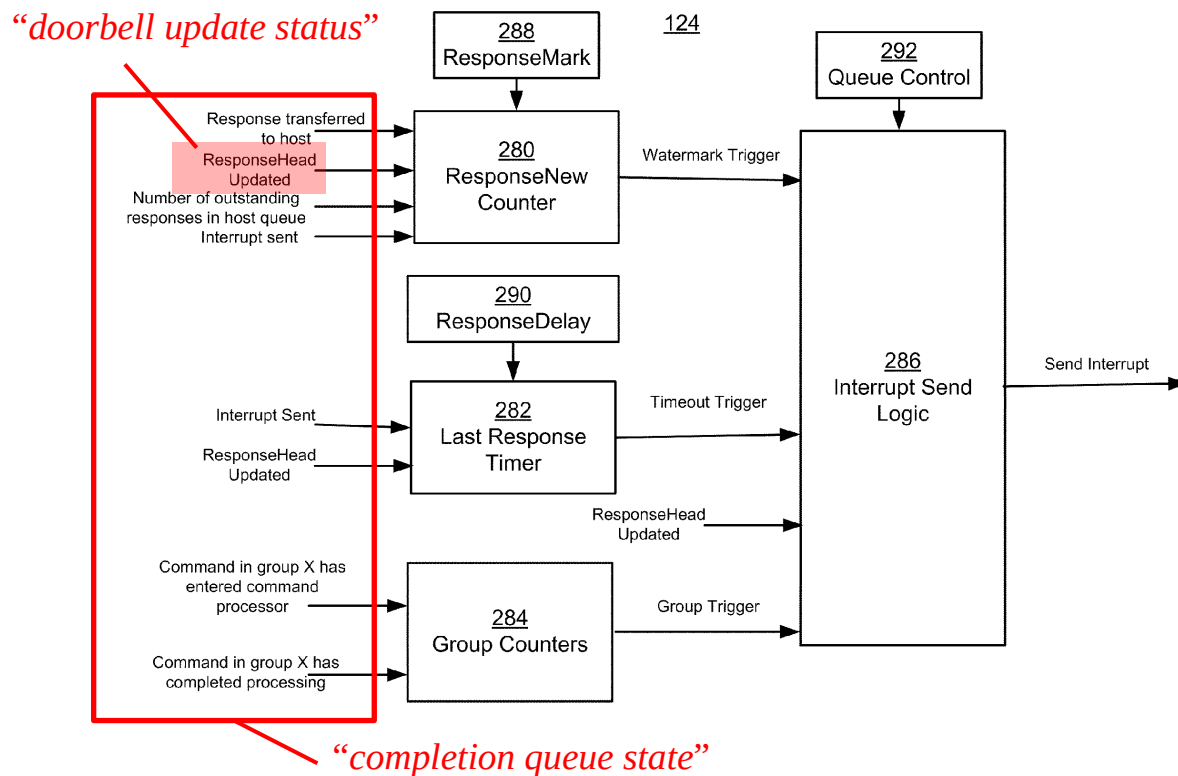
Ex.1005, Fig. 2 (annotated); Ex.1003, ¶119.

Third, the indication that the host has updated the response head pointer is a “doorbell update status” as claimed. Such a mechanism that indicates when the response head pointer has been updated is often referred to as a “doorbell” update status. Ex.1003, ¶120. Using a response queue that is produced by the memory controller and consumed by the host is referred to as the producer/consumer model. Ex.1003, ¶120. Indeed, Borchers explains that the “data storage device 100 may be the ... producer of the response buffer 123” and the “host 106 may be the ... consumer of the response buffer 123.” Ex.1005, [0030].

The PCI standard explains that in this Producer-Consumer model, a

notification of the head pointer being updated is a “doorbell” event. Ex.1006, 308; Ex.1003, ¶121. Thus, the host (consumer of the response queue) may “signal the Producer using an interrupt or **another doorbell register.**” Ex.1006, 308.

A POSITA would have thus recognized that the register that stores the head pointer is a doorbell update register. Ex.1003, ¶122. Accordingly, the notification that the head pointer of the response queue has been updated is a “*doorbell update status*” as claimed. Indeed, the claim language itself defines what a doorbell update status does—an indication “*in which the host processing unit updates a head pointer ... for the completion queue.*” Borchers does precisely that by sending a notification that the head pointer of the response queue (“*completion queue*”) has been updated. Accordingly, Borchers’ notification that the head pointer of the response queue is a “*doorbell update status*” as claimed.



Ex.1005, Fig. 2 (annotated); Ex.1003, ¶122.

Fourth, Borchers' head pointer is stored in a register on the storage device controller (*"head pointer stored in the nonvolatile memory controller for the completion queue"*). Borchers' "data storage device can include ... a fourth register configured to store responsehead pointer values." Ex.1005, [0005]; *see also* Ex.1005, [0030] (*"[A]nd values of the head pointer of the response buffer can be stored in a register on the data storage device 100."*). Borchers further explains that the register that stores the head pointer may be within the controller: "The command tail pointer and the response head pointer may be stored in registers of the data storage device 100 in memory mapped I/O space within the

controller 110.” Ex.1005, [0031].

Thus, because Borchers’ interrupt processor maintains information about the response queue, including that the response head pointer has been updated, and the head pointer is stored in a doorbell register within the memory controller, Borchers renders this limitation obvious. Ex.1003, ¶¶117-25.

4. Claim 2

[2.1] *The nonvolatile memory controller of claim 1, wherein the interrupt is a hardware interrupt.*

Borchers controller 110, which includes the interrupt processor 124, may be “implemented in hardware.” Ex.1005, [0113]. Thus, the interrupts sent by the interrupt processor are hardware interrupts.

Additionally, the specification of the ’968 patent refers to MSI and MSI-x interrupts as hardware interrupts: “In some embodiments, **the hardware interrupt generated in the host processing unit 110 is a message signal interrupt (MSI) or an extended message signal interrupts (MSI-X)** as defined in the PCI Specification 3.0.” Ex.1001, 16:61-64. For the reasons explained above at [1.4], a POSITA would have found it obvious for Borchers’ PCIe interrupts to be MSI or MSI-x signals associated with the PCI express standard.

Thus, because Borchers’ memory controller and interrupt processor may be implemented in hardware, and may be MSI or MSI-x interrupt signals, Borchers

renders this limitation obvious. Ex.1003, ¶¶126-28.

5. Claim 3

[3.1] *The nonvolatile memory controller of claim 1, wherein the interrupt message packet includes an interrupt vector associated with the completion queue for triggering the interrupt in the host processing unit.*

First, as explained above at [1.4], a POSITA would have found it obvious—based on background knowledge—for Borchers’ interrupt signals to be MSI or MSI-x interrupt signals. Such interrupt signals include both a message address and message data, which are referred to as an interrupt vector. See Ex.1006, 231 (“System software initializes the message address and message data (from here on referred to as the ‘vector’)”). Accordingly, Borchers’ interrupt signals include an “*interrupt vector.*”

Second, Borchers’ interrupt signals trigger an interrupt in the host processor. “The interrupt processor 124 is configured to signal the host 106 with an interrupt when new responses are available in the response buffer 123.” Ex.1005, [0035]. The interrupt signal received by the host then causes the host to process the interrupt, thereby “*triggering the interrupt in the host processing unit.*” See e.g., Ex.1005, [0050] (“an interrupt may be received by an interrupt handler 225a-225n”).

Thus, because it would have been obvious for Borchers’ interrupt signals, which trigger interrupts in the host, to include vectors consistent with PCI

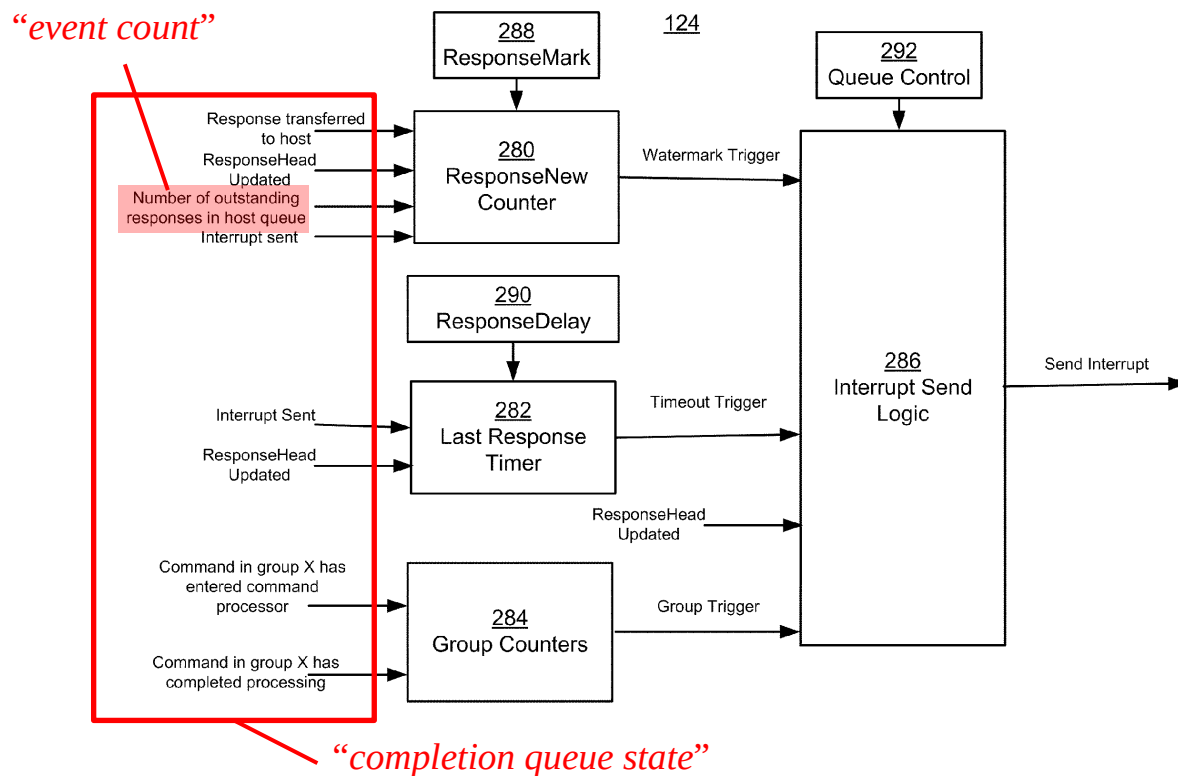
standards, Borchers renders this limitation obvious. Ex.1003, ¶¶129-32.

6. Claim 4

[4.1] *The nonvolatile memory controller of claim 3, wherein completion queue state includes an event count indicating a number of completion message packets received by the host controller interface for the completion queue associated with the completion queue state.*

First, as explained above at [1.1], Borchers' interrupt processor generates response queue status information ("*completion queue state*").

Second, that information includes the number of outstanding responses in the response queue ("*event count*"). "The ResponseNew counter 280 receives as inputs information including ... **the number of outstanding responses** in the host response buffer 123 and when an interrupt has been sent." Ex.1005, [0060].



Ex.1005, Fig. 2 (annotated); Ex.1003, ¶134.

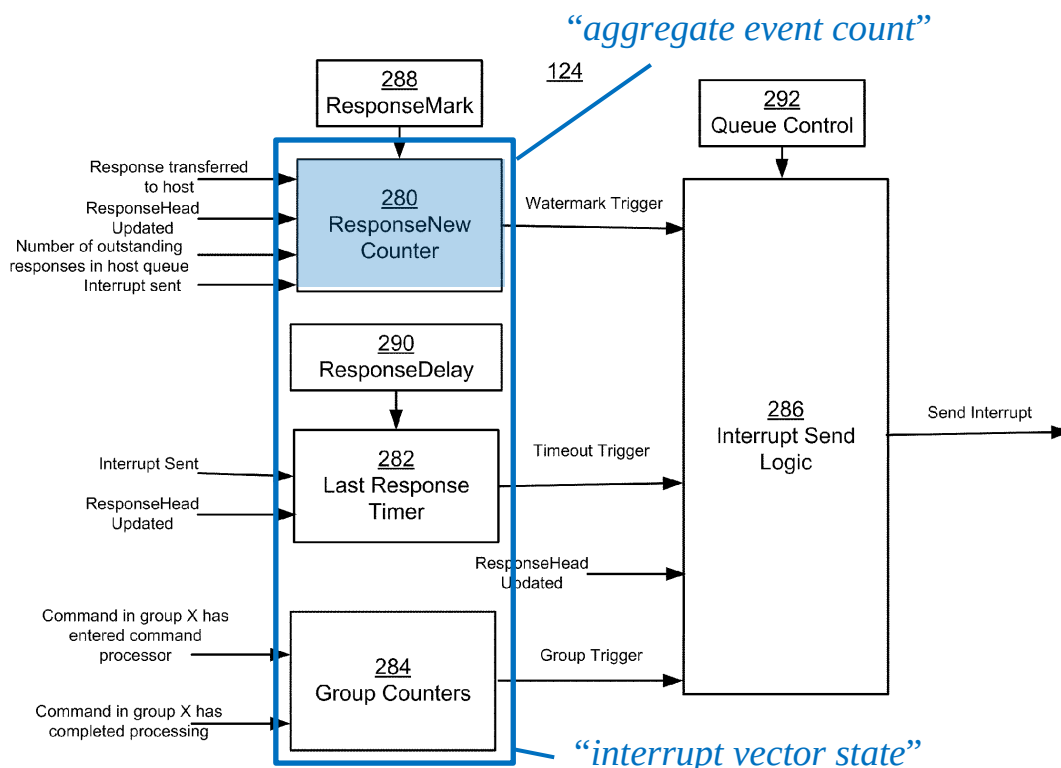
Thus, because Borchers maintains status information including the number of outstanding responses in the host’s response queue, Borchers renders this limitation obvious. Ex.1003, ¶¶133-35.

7. Claim 5

[5.1] The nonvolatile memory controller of claim 4, wherein the interrupt vector state includes an aggregate event count for aggregating event counts of the completion queue state over a plurality of update operations, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the aggregate event count is below an aggregate event count threshold.

First, Borchers’ interrupt mechanisms (“interrupt vector state”) include a ResponseNew Counter 280 (“aggregate event count”). See Ex.1005, [0060]. The

ResponseNew Counter receives as an input various pieces of information as to the status of the response queue (“*completion queue state*”). One such piece of information is when an event is sent to the host. “The ResponseNew Counter 280 is configured to track the number of responses transferred to the host 106 that the host has yet to process. Each time a response is transferred to the response buffer 123 the counter is incremented.” Ex.1005, [0060]. Accordingly, because the ResponseNew Counter 280 is incremented over multiple events, the ResponseNew counter 280 is for “*aggregating event counts of the completion queue state over a plurality of update operations.*”



Ex.1005, Fig. 2 (annotated); Ex.1003, ¶137.

Second, Borchers' interrupt processor 124 does not send an interrupt signal until the ResponseNew Counter 280 (*"aggregate event count"*) reaches a watermark level (*"the interrupt manager is inhibited from generating an interrupt message packet if the aggregate event count is below an aggregate event count threshold"*). "In one exemplary implementation, the host 106, through its driver 107, may control when the interrupt processor 124 should generate interrupts." Ex.1005, [0036] "For instance, the host 106 through the driver 107 may configure the interrupt processor 124 to use a water mark interrupt mechanism." Ex.1005, [0036]. "If the count of new responses in the response buffer 123 is equal to or greater than the ResponseMark [*"threshold"*], then an interrupt is generated by the interrupt processor 124 and the count is zeroed." Ex.1005, [0037].

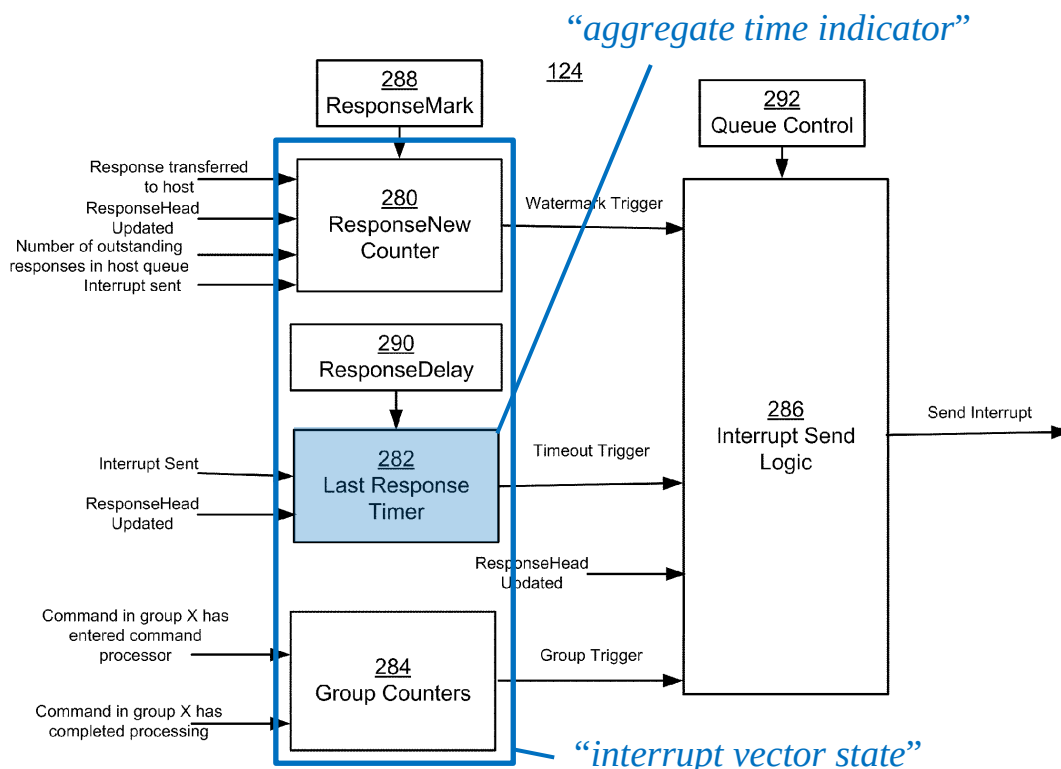
Thus, because the ResponseNew Counter gets incremented when the interrupt processor places events in the response queue, and does not send an interrupt until the watermark threshold is met, Borchers renders this limitation obvious. Ex.1003, ¶¶136-39.

8. Claim 6

[6.1] *The nonvolatile memory controller of claim 3, wherein the interrupt vector state includes an aggregate time indicator for indicating, a time period between the last time the interrupt manager generated an interrupt message packet for the completion queues associated with the interrupt vector state.*

Borchers' interrupt mechanisms (*"interrupt vector state"*) include a Last

Response timer 282 (“*aggregate time indicator*”). “The last response timer 282 may be configured to keep track of time since the last interrupt.” Ex.1005, [0062]. “The last response timer 282 also may receive a signal when the ResponseHead is updated, which indicates that the host 106 has removed responses from the response buffer 123.” Ex.1005, [0063]. When the timer reaches its ResponseDelay parameter (“*threshold*”), “and the response buffer 123 contains new responses, then a timeout trigger signal is sent to the interrupt send logic 286.” Ex.1005, [0064].



Ex.1005, Fig. 2 (annotated); Ex.1003, ¶140.

Accordingly, Borchers’ last response timer 282 is for keeping track of the

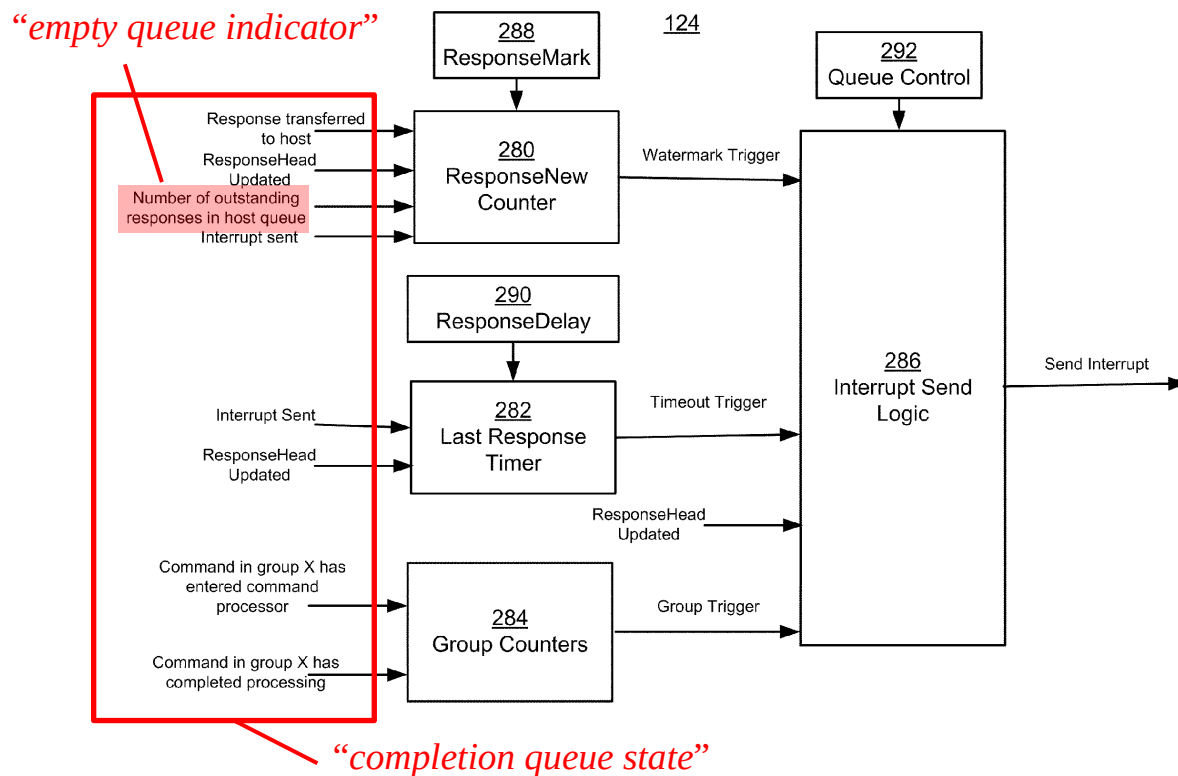
amount of time since the last interrupt was sent (“*for indicating, a time period between the last time the interrupt manager generated an interrupt message packet for the completion queues associated with the interrupt vector state.*”)

Thus, because Borchers’ Last Response Timer indicates the amount of time since the interrupt processor last sent an interrupt signal to the host, Borchers renders this limitation obvious. Ex.1003, ¶¶140-42.

9. Claim 7

[7.1] The nonvolatile memory controller of claim 3, wherein the completion queue state includes an empty queue indicator for indicating whether the completion queue is empty, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the empty queue indicator indicates the completion queue is empty.

First, as explained above at [4.1], Borchers’ response queue status information (“*completion queue state*”) includes the number of outstanding responses in the response queue. Ex.1005, [0060]. When that number is zero, it is an “*empty queue indicator*” that indicates the response queue (“*completion queue*”) is empty. Accordingly, the information that indicates the number of outstanding responses in the response queue acts as an empty queue indicator when the number is zero.



Ex.1005, Fig. 2 (annotated); Ex.1003, ¶143.

Second, Borchers' system does not send an interrupt if there are no outstanding responses in the response queue (*"wherein the interrupt manager is inhibited from generating an interrupt message packet if the empty queue indicator indicates the completion queue is empty"*). Rather, the interrupt send logic 286 generates interrupts only if the watermark level is reached, the timer is triggered, or the group counter is triggered. See Ex.1005, [0036]-[0037]. A POSITA would have further understood that there would be no reason to send an interrupt if there are no responses in the response queue for the host to process. Ex.1003, ¶144.

Thus, because the response queue status information includes the number of

outstanding responses in the host queue, which may be zero, and the processor does not needlessly send interrupts when there are no responses in the response queue to process, Borchers renders this limitation obvious. Ex.1003, ¶¶143-46.

10. Claim 8

[8.0] A *nonvolatile memory controller comprising:*

For the reasons explained at [1.0], Borchers teaches a “*nonvolatile memory controller*” as claimed. Ex.1003, ¶147.

[8.1] a *completion queue state memory configured to store a plurality of completion queue states corresponding to a plurality of completion queues in a host processing unit;*

First, as explained above at [1.1], Borchers teaches a “*completion queue state*” as claimed. Ex.1003, ¶148.

Second, the memory location where Borchers’ response queue status information is stored or buffered (e.g., RAM, a register, a flag), is “*a completion queue state memory*” as claimed. As one example, Borchers’ memory controllers includes “register 161” that may be used to store or buffer such status information. Ex.1005, [0030].

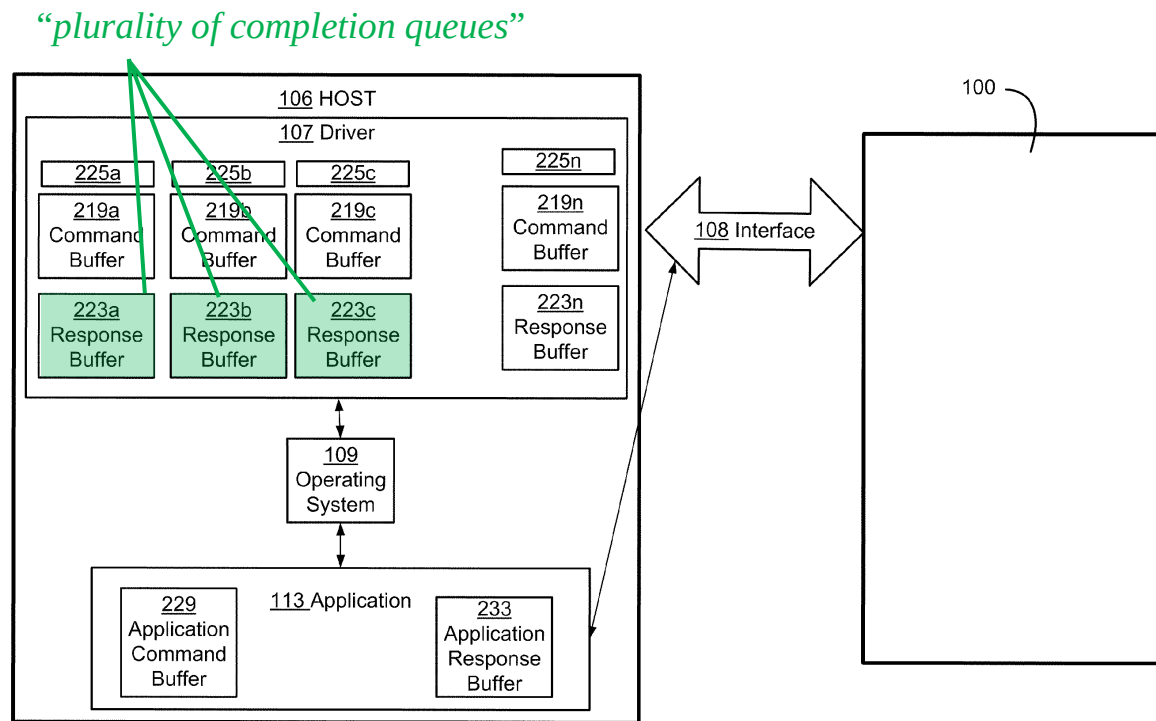
Given that the register stores items such as head and tail pointers, it would have been obvious for register 161 to buffer or temporarily store the response queue status information. Indeed, it was known to store such information in a buffer or register. *See e.g.*, Ex.1008, Figs. 2 & 5, [0057], [0090]-[0091]; Ex.1009,

Figs. 2 & 5, [0051], [0083], [0084] (describing how an interrupt manager uses various forms of memory such as cache or registers to store state information).

Accordingly, the storage location used by Borchers' interrupt processor to store the interrupt mechanism information is a *“a completion queue state memory configured to store a plurality of completion queue states.”*

Third, Borchers describes an example in which there are a plurality of response queues in the host (*“a plurality of completion queues in a host processing unit”*). “Although FIG. 1A illustrates one command buffer 119 and one response buffer 123, multiple pairs of buffers may be used, as illustrated in FIG. 1B.”

Ex.1005, [0028]; *see also* [0046]-[0058].

**FIG. 1B****Ex.1005, Fig. 1B (annotated); Ex.1003, ¶150.**

As also explained above, Borchers explains that the command and response queues of Fig. 1A may be implemented as circular queues: “In one exemplary implementation shown in FIG. 1C the command buffer 119 can be configured as a circular queue 159 that is used to communicate information from the host 106 and to the data storage device 100 of FIG. 1A.” Ex.1005, [0030]. Accordingly, it would have been obvious for Borchers’ host to include multiple buffer pairs (as shown in Fig. 1B and described in accompanying text) which are implemented as circular queues (as shown in Fig. 1C and described in accompanying text). Indeed, when describing the buffer pairs of Fig. 1B, Borchers explains that “Each of the buffer

pairs may include its own set of head and tail pointers. The use of the head and tail pointers may be the same as described above with respect to the command buffer 119 and the response buffer 123 of FIG. 1A.” Ex.1005, [0049].

As explained above at [1.1], Borchers describes that the interrupt processor 124 receives status information as to the response queue. Accordingly, in the example where there are multiple response queues, it would have been obvious that the interrupt processor receives status information for each of the response queues. The status information for each of the response queues thus teaches “*a plurality of completion queue states corresponding to a plurality of completion queues*” as claimed.

Thus, because Borchers’ interrupt controller receives and utilizes response queue status information for a plurality of buffers, Borchers renders obvious “*a completion queue state memory configured to store a plurality of completion queue states corresponding to a plurality of completion queues in a host processing unit*” as claimed. Ex.1003, ¶¶148-53

Additionally, Borchers teaches a “*plurality of completion queue states*” in that there are several pieces of status information, including that a Response has been transferred to the host, the response queue head pointer has been updated, and the number of outstanding responses in the host queue. See Ex.1005, Fig. 2; Ex.1005, [0060]; Ex.1003, ¶154.

[8.2] *an interrupt vector state memory configured to store a plurality of interrupt vector states corresponding to a plurality of interrupt vectors in the host processing unit; and*

First, as explained above at [1.2], Borchers teaches various interrupt mechanisms that teach an “*interrupt vector state*” as claimed. These interrupt mechanisms are used to determine whether to send an interrupt signal to alert the host that there are responses in the response queue that have yet to be processed. See Ex.1005, [0060].

Second, as explained above at [8.1], Borchers describes an example in which there are multiple response queues on the host. See Ex.1005, Fig. 1B, [0046]-[0048]. Accordingly, in such case, there would be multiple interrupt mechanisms—one for each response queue. For example, there would be a ResponseNew Counter 280 for each response queue. There would be a last response timer 282 for each response queue. The multiple ResponseNew Counters or last response timers thus teach “*a plurality of interrupt vector states*” as claimed.

Additionally, Borchers teaches “*a plurality of interrupt vector states*” in that there are multiple types of interrupt vector states. For example, the ResponseNew counter 280 and last response timer 282 together teach “*a plurality of interrupt vector states*” as claimed.

Third, as with the completion queue state memory described above at [8.1],

the memory used by the interrupt processor 124 to store the interrupt mechanism information (e.g., response count or time) teaches an “*interrupt vector state memory*” as claimed. For example, whether the interrupt mechanism information is stored in register 161 or some other register or location, such storage location teaches an “*interrupt vector state memory*” as claimed.

Fourth, for the reasons explained above at [1.2], it would have been obvious for Borchers’ interrupt signals to be implemented as interrupt vectors consistent with the PCI standard. Accordingly, each of Borchers’ interrupt mechanisms corresponds to a different interrupt vector (“*a plurality of interrupt vector states corresponding to a plurality of interrupt vectors*”).

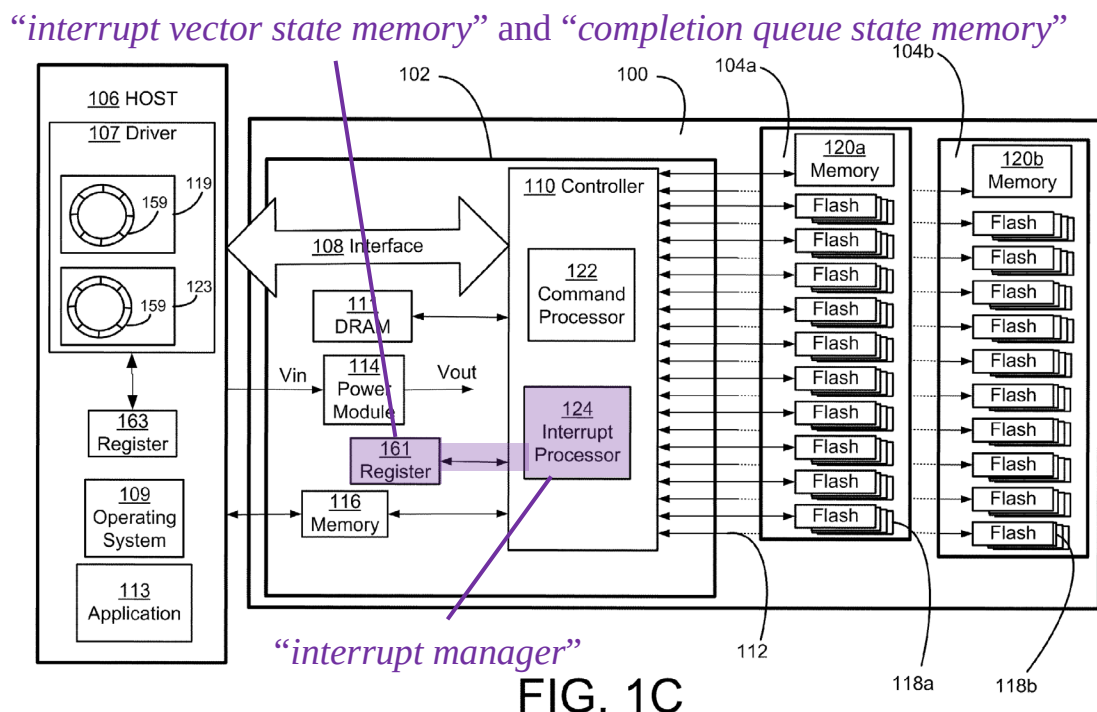
Thus, because Borchers’ host includes a plurality of response buffers, and the memory controller utilizes interrupt mechanisms that determine when to send an interrupt signal for unprocessed responses in those buffers, Borchers renders this limitation obvious. Ex.1003, ¶¶155-60.

Additionally, Borchers teaches a “*plurality of interrupt vector states*” in that there are multiple interrupt mechanisms. These multiple interrupt mechanisms include a ResponseNew Counter 280, a last response timer 282, and a group counter 284. See Ex.1005, Fig. 2; Ex.1005, [0060]; Ex.1003, ¶161.

[8.3] an interrupt manager controller coupled to the completion queue state memory and the interrupt vector state memory,

First, as described above at [1.1], Borchers' memory controller includes an interrupt processor 124 (*"interrupt manager controller"*).

Second, the interrupt manager controller utilizes the response queue status information (*"completion queue state"*) and interrupt mechanisms (*"interrupt vector state"*). Accordingly, the interrupt processor is "coupled to" the storage locations of the status information and interrupt mechanism information. For example, the interrupt processor is coupled with register 161, which is one option where the response queue status information and interrupt mechanism information may be stored.



Ex.1005, Fig. 1C (annotated); Ex.1003, ¶163.

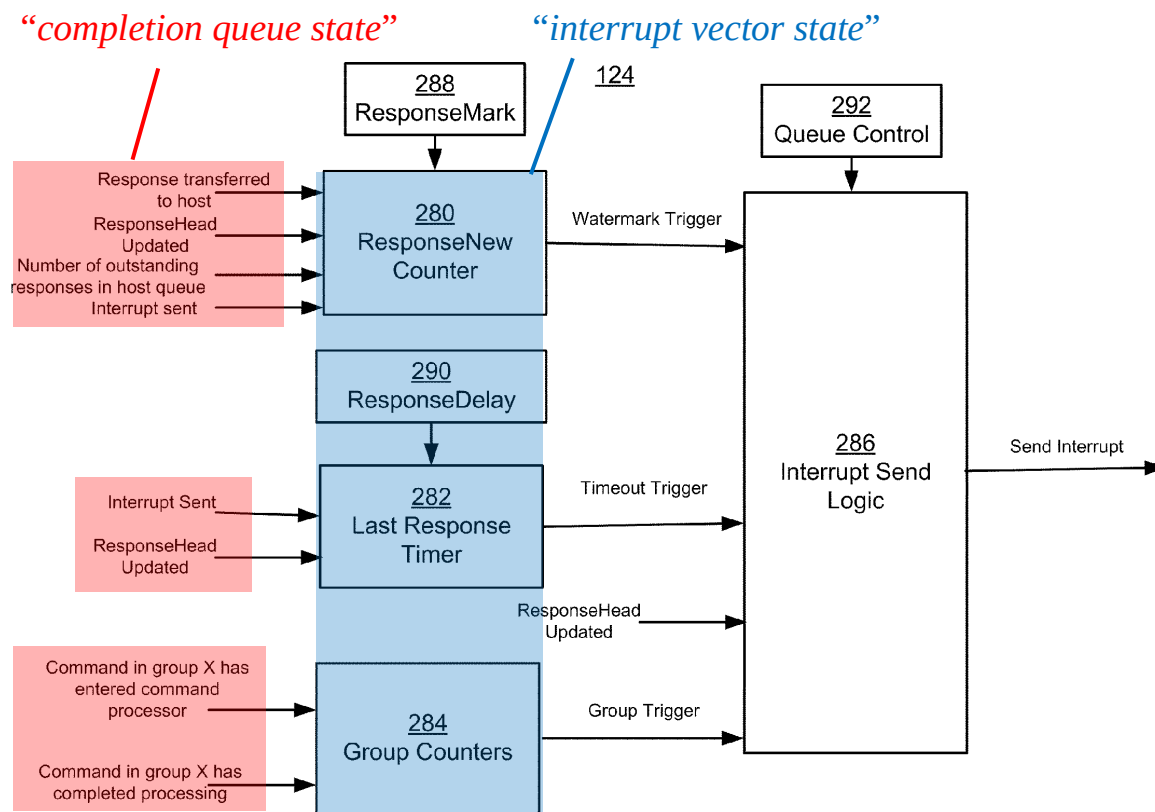
Thus, because Borchers describes an interrupt processor that utilizes response queue status information and interrupt mechanism information stored in a type of data storage, Borchers renders this limitation obvious. Ex.1003, ¶¶162-64.

[8.4] *the interrupt manager controller configured to map at least one completion queue state of the plurality of completion queue states to an interrupt vector state of the plurality of interrupt vector states,*

Borchers explains that when there are multiple command/response queue pairs as shown in Fig. 1B, each buffer pair is processed and handled separately. “The command buffers 219a-219n and the response buffers 223a-223n may be configured to operate and function as described above with respect to the command buffer 119 and the response buffer 123 of FIG. 1A.” Ex.1005, [0049]. “The multiple different head and tail pointers, each of which corresponds to a buffer pair, may be stored on the host 106, the data storage device 100 or a combination of the host 106 and the data storage device 100.” Ex.1005, [0049]. “In some instances, an interrupt may be received by an interrupt handler 225a-225n when a related group of commands has been processed by the data storage device, as discussed in more detail below with respect to FIG. 2.” Ex.1005, [0050]. “Each of the buffer pairs may be granted access to any address mapping, which may be stored on the host 106 and/or on the data storage device 100.” Ex.1005, [0051].

Accordingly, each buffer pair is handled separately in the manner described with Fig. 2. Fig. 2 describes the response queue status information (“*completion*

queue state”) and interrupt mechanisms (*“interrupt vector state”*) as shown below. Thus, for each separate command/response buffer pair, the corresponding response queue status information is associated with the corresponding interrupt mechanisms for that pair (*“map at least one completion queue state of the plurality of completion queue states to an interrupt vector state of the plurality of interrupt vector states”*).

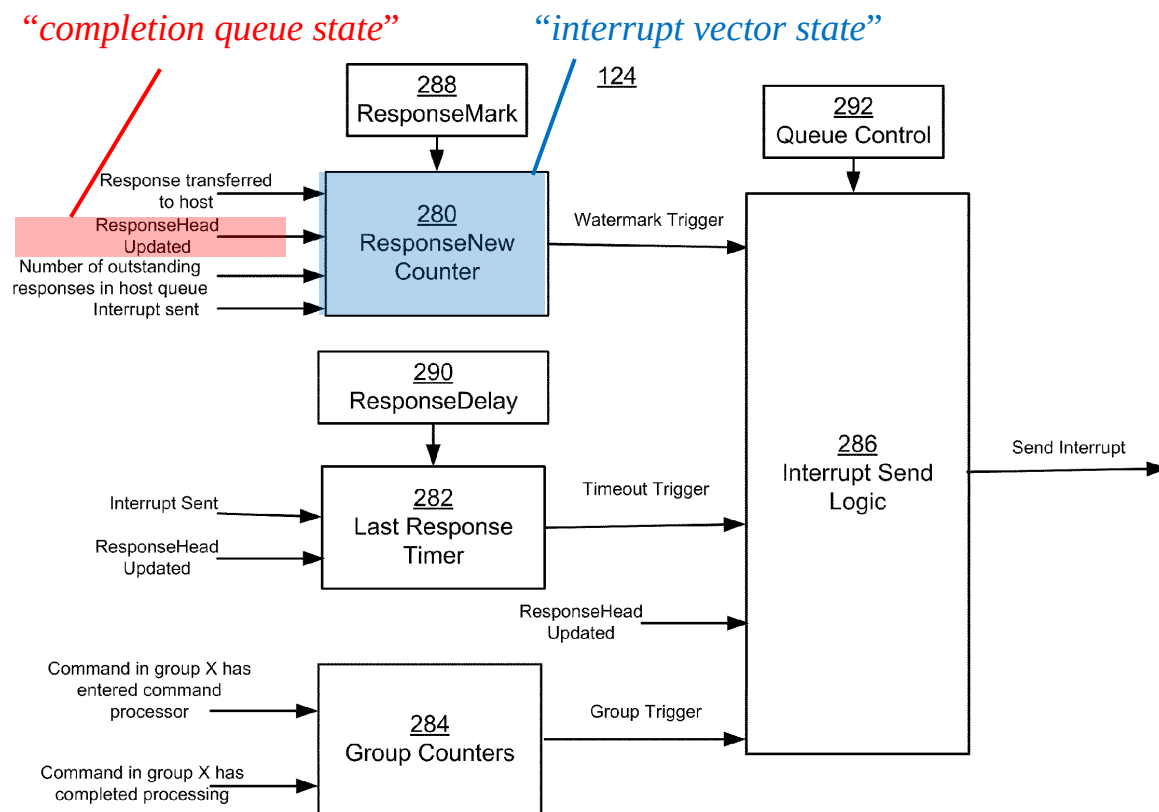


Ex.1005, Fig. 2 (annotated); Ex.1003, ¶166.

Thus, because Borchers’ interrupt controller includes interrupt mechanisms for each separate command/response buffer pair, Borchers renders this limitation

obvious. Ex.1003, ¶¶165-67.

Additionally, Borchers teaches a “*plurality of completion queue states*” in that there are several pieces of status information, including that a Response has been transferred to the host, the response queue head pointer has been updated, and the number of outstanding responses in the host queue. At least one of these pieces of information is mapped to one of the interrupt mechanisms. For example, the ResponseHead updated piece of information is mapped to the ResponseNew Counter 280 as shown below.



Borchers, Fig. 2 (annotated); Ex.1003, ¶168.

Thus, because Borchers maps at least one of the response queue status items (ResponseHead Updated) to one of the interrupt mechanisms (ResponseNew Counter 280), Borchers renders this limitation obvious. Ex.1003, ¶¶168-69.

[8.5] *generate the interrupt vector state based on each completion queue state mapped to the interrupt vector state,*

First, for the reasons explained above at [1.2], Borchers generates interrupt mechanism information (“*interrupt vector state*”) based on the status information of the response queue (“*each completion queue state mapped to the interrupt vector state*”).

Second, in the case where there are multiple command/response buffer pairs as described in Fig. 1B (and described above at [8.1]), Borchers’ system would include counters and timers (“*interrupt vector state[s]*”) for each command/response queue. Accordingly, each of the counters/timers are “*based on*” their respective response queue status information (“*completion queue state*”). Ex.1003, ¶¶170-71.

[8.6] *determine a completion queue corresponding to a completion queue state mapped to the interrupt vector state contains an unprocessed completion status based on the interrupt vector state, and*

For the reasons explained above at [1.3], Borchers renders this limitation obvious. Ex.1003, ¶172.

[8.7] *to generate an interrupt message packet based on the interrupt vector state for triggering an interrupt in the host processing unit to alert the host processing*

unit of the unprocessed completion status in the completion queue.

For the reasons explained above at [1.4], Borchers renders this limitation obvious. Ex.1003, ¶173.

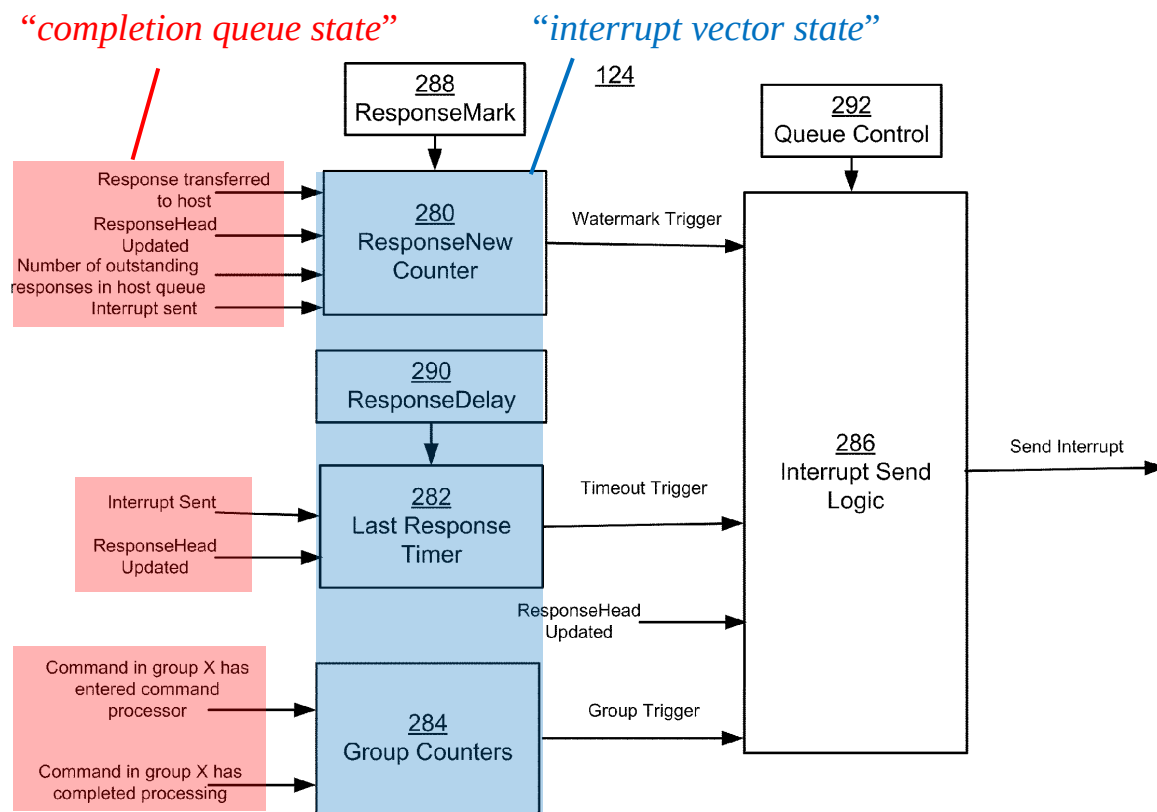
11. Claim 9

[9.1] The nonvolatile memory controller of claim 8, wherein the interrupt manager controller is configured to map at least two completion queue states of the plurality of completion queue states to the interrupt vector state.

Borchers explains that when there are multiple command/response queue pairs as shown in Fig. 1B, each buffer pair is processed and handled separately. “The command buffers 219a-219n and the response buffers 223a-223n may be configured to operate and function as described above with respect to the command buffer 119 and the response buffer 123 of FIG. 1A.” Ex.1005, [0049]. “The multiple different head and tail pointers, each of which corresponds to a buffer pair, may be stored on the host 106, the data storage device 100 or a combination of the host 106 and the data storage device 100.” Ex.1005, [0049]. “In some instances, an interrupt may be received by an interrupt handler 225a-225n when a related group of commands has been processed by the data storage device, as discussed in more detail below with respect to FIG. 2.” Ex.1005, [0050]. “Each of the buffer pairs may be granted access to any address mapping, which may be stored on the host 106 and/or on the data storage device 100.” Ex.1005, [0051].

Accordingly, each buffer pair is handled separately in the manner described

with Fig. 2. Fig. 2 describes the response queue status information (“*completion queue state*”) and interrupt mechanisms (“*interrupt vector state*”) as shown below. Thus, for each separate command/response buffer pair, the corresponding response queue status information is associated with the corresponding interrupt mechanisms for that pair (“*map at least two completion queue states of the plurality of completion queue states to the interrupt vector state*”).

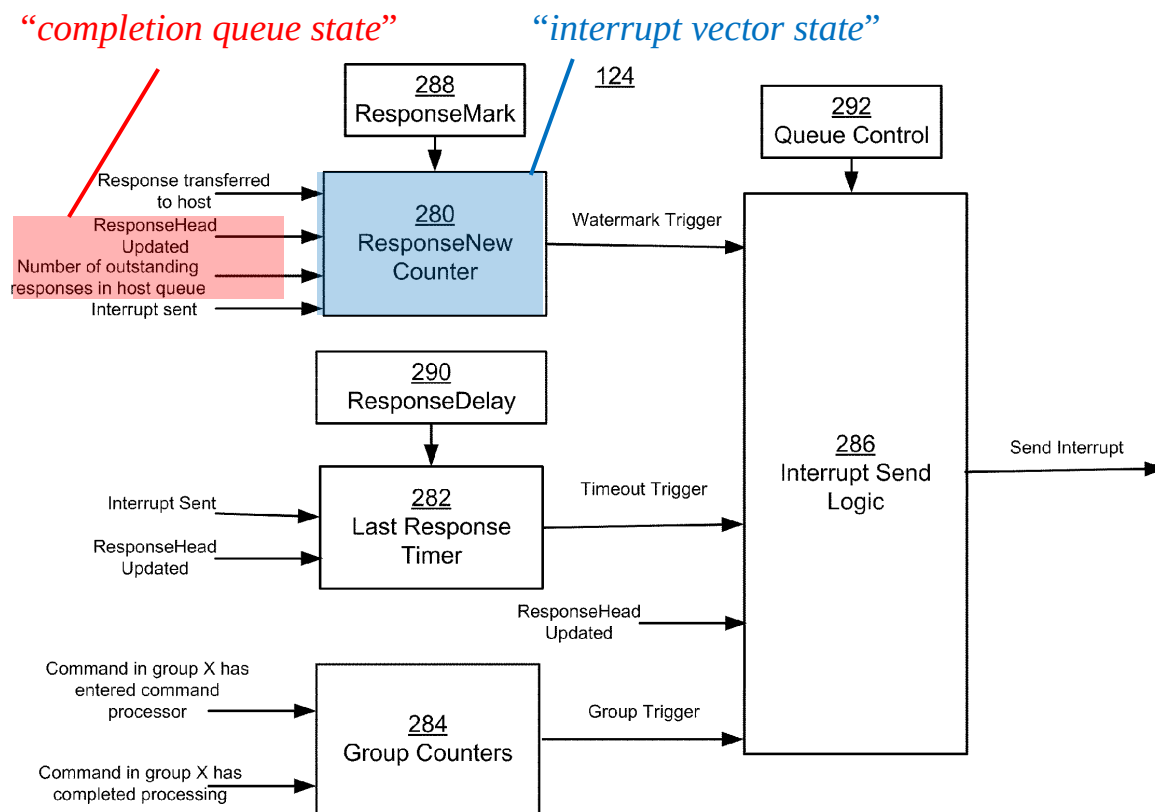


Ex.1005, Fig. 2 (annotated); Ex.1003, ¶175.

Thus, because Borchers’ interrupt controller includes interrupt mechanisms for each separate command/response buffer pair, Borchers renders this limitation

obvious. Ex.1003, ¶¶174-76.

Additionally, Borchers teaches a “*plurality of completion queue states*” in that there are several pieces of status information, including that a Response has been transferred to the host, the response queue head pointer has been updated, and the number of outstanding responses in the host queue. At least two of these pieces of information is mapped to one of the interrupt mechanisms. For example, the ResponseHead updated piece of information and number of outstanding response are mapped to the ResponseNew Counter 280 as shown below.



Ex.1005, Fig. 2 (annotated); Ex.1003, ¶177.

Thus, because Borchers maps at least one of the response queue status items (ResponseHead Updated) to one of the interrupt mechanisms (ResponseNew Counter 280), Borchers renders this limitation obvious. Ex.1003, ¶¶177-78.

12. Claim 10

[10.1] *The nonvolatile memory controller of claim 8, wherein the interrupt manager controller is a sequential logic circuit.*

The specification of the '968 patent describes a sequential logic circuit as a state machine: “In various embodiments, the interrupt manager 1040 is a hardware mechanism for generating interrupt message packets. For example, the interrupt manager controller 1100 in the interrupt manager 1040 may be a sequential logic circuit (e.g., a state machine).” ’968 patent, 17:55-59. A POSITA would have understood a state machine to be any discrete computing system such as a digital computer. *See e.g.*, Ex.1010, 1102 (“**state machine** A model of a system in which all values are discrete, as in a digital computer.”). Borchers explains that the memory controller, of which the interrupt processor is a part, may be implemented in a variety of manners, all of which are some form of a state machine or “*sequential logic circuit.*” “The controller 110 may include a microcontroller, a FPGA controller, other types of controllers, or combinations of these controllers.” Ex.1005, [0113]. “In another exemplary implementation, the controller 110 is a FPGA controller. The FPGA controller may be implemented in hardware,

software, or a combination of hardware and software.” Ex.1005, [0114]. “Method steps also may be performed by, and an apparatus may be implemented as, special purpose logic circuitry, e.g., a FPGA (field programmable gate array) or an ASIC (application-specific integrated circuit).” Ex.1005, [0127].

Thus, because Borchers’ memory controller, and its associated interrupt processor may be implemented in a variety of manners, including FPGAs or special logic circuitry, Borchers renders this limitation obvious. Ex.1003, ¶¶179-80.

13. Claim 11

[11.1] The nonvolatile memory controller of claim 8, wherein a completion queue state of the plurality of completion queue states includes a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue.

For the reasons explained above at [1.5] and [8.1], Borchers renders this limitation obvious. Ex.1003, ¶181.

14. Claim 12

[12.1] The nonvolatile memory controller of claim 8, wherein a completion queue state of the plurality of completion queue states includes an event count indicating a number of completion message packets received by a host controller interface and including a completion status for the completion queue associated with the completion queue state.

For the reasons explained above at [4.1], Borchers renders obvious “*wherein a completion queue state of the plurality of completion queue states includes an*

event count indicating a number of completion message packets received by a host controller interface.” Ex.1003, ¶182.

In addition, for the reasons explained above at [1.1] and [1.3], Borchers teaches “*a completion queue state of the plurality of completion queue states ... including a completion status for the completion queue associated with the completion queue state.*” Ex.1003, ¶183.

15. Claim 13

[13.1] *The nonvolatile memory controller of claim 12, wherein the interrupt vector state includes an aggregate event count for aggregating event counts of the completion queue state over a plurality of update operations, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the aggregate event count is below an aggregate event count threshold.*

See [5.1]. Ex.1003, ¶184.

16. Claim 14

[14.1] *The nonvolatile memory controller of claim 8, wherein the interrupt vector state includes an aggregate time indicator for indicating a time period between the last time the interrupt manager generated an interrupt message packet for the completion queues associated with the interrupt vector state, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the aggregate time indicator is below an aggregate time threshold.*

First, for the reasons explained above at [6.1], Borchers renders obvious “*wherein the interrupt vector state ... associated with the interrupt vector state*” as claimed.

Second, Borchers’ interrupt processor 124 does not send an interrupt signal

until the last response timer (“*aggregate time indicator*”) reaches a time threshold (“*wherein the interrupt manager is inhibited from generating an interrupt message packet if the aggregate time indicator is below an aggregate time threshold*”). “In one exemplary implementation, the host 106, through its driver 107, may control when the interrupt processor 124 should generate interrupts.” Ex.1005, [0036]. “For instance, the host 106 through the driver 107 may configure the interrupt processor 124 to use a water mark interrupt mechanism, a timeout interrupt mechanism, a group interrupt mechanism, or a combination of these interrupt mechanisms.” Ex.1005, [0036]. “If the time (e.g., time in microseconds) since the last interrupt is equal to or greater than the ResponseDelay and there are new responses in the response buffer 123, then the interrupt processor 124 generates an interrupt and the timeout is zeroed.” Ex.1005, [0037].

Thus, because Borchers uses a last response timer and does not send an interrupt signal until the timer reaches a Response Delay value, Borchers renders this limitation obvious. Ex.1003, ¶¶185-87.

17. Claim 15

[15.1] *The nonvolatile memory controller of claim 8, wherein a completion queue state of the plurality of completion queue states includes an empty queue indicator for indicating whether the completion queue is empty, and wherein the interrupt manager is inhibited from generating an interrupt message packet if the empty queue indicator indicates the completion queue is empty.*

See [7.1]. Ex.1003, ¶188.

18. Claim 16**[16.0] A method comprising:**

Borchers describes a method for using circular command queues for communication between a host and memory controller. “In another general aspect, a method for communicating commands between a host and a flash memory data storage device includes populating a circular command queue of a driver on the host with commands for retrieval by the data storage device.” Ex.1005, [0006].

Accordingly, Borchers teaches “a method” as claimed. Ex.1003, ¶¶189-90.

[16.1] generating a completion queue state by a nonvolatile memory controller for indicating the occurrence of a completion queue event associated with a completion queue in a host processing unit,

See [1.1]. Ex.1003, ¶191.

[16.2] the completion queue state including a doorbell update status indicating whether the host processing unit has performed a doorbell update event in which the host processing unit updates a head pointer stored in the nonvolatile memory controller for the completion queue;

See [1.5]. Ex.1003, ¶192.

[16.3] generating an interrupt vector state by the nonvolatile memory controller based on the completion queue state, the interrupt vector state associated with an interrupt vector in the host processing unit;

First, for the reasons explained above at [1.2], Borchers renders obvious “generating ... queue state.”

Second, as explained above at [1.2], it would have been obvious for Borchers’ interrupt signals to include interrupt vectors (i.e., a message address and

message data). Accordingly, Borchers renders obvious “*the interrupt vector state associated with an interrupt vector in the host processing unit*” as claimed.

Ex.1003, ¶¶193-94.

[16.4] *determining by the nonvolatile memory controller based on the interrupt vector state that the completion queue contains an unprocessed completion status; and*

See [1.3]. Ex.1003, ¶195.

[16.5] *generating an interrupt message packet by a nonvolatile memory interface for triggering an interrupt in the host processing unit to alert the host processing unit of the unprocessed completion status in the completion queue.*

See [1.4]. Ex.1003, ¶196.

19. Claim 17

[17.1] *The method of claim 16, further comprising sending the interrupt message packet to the host processing unit.*

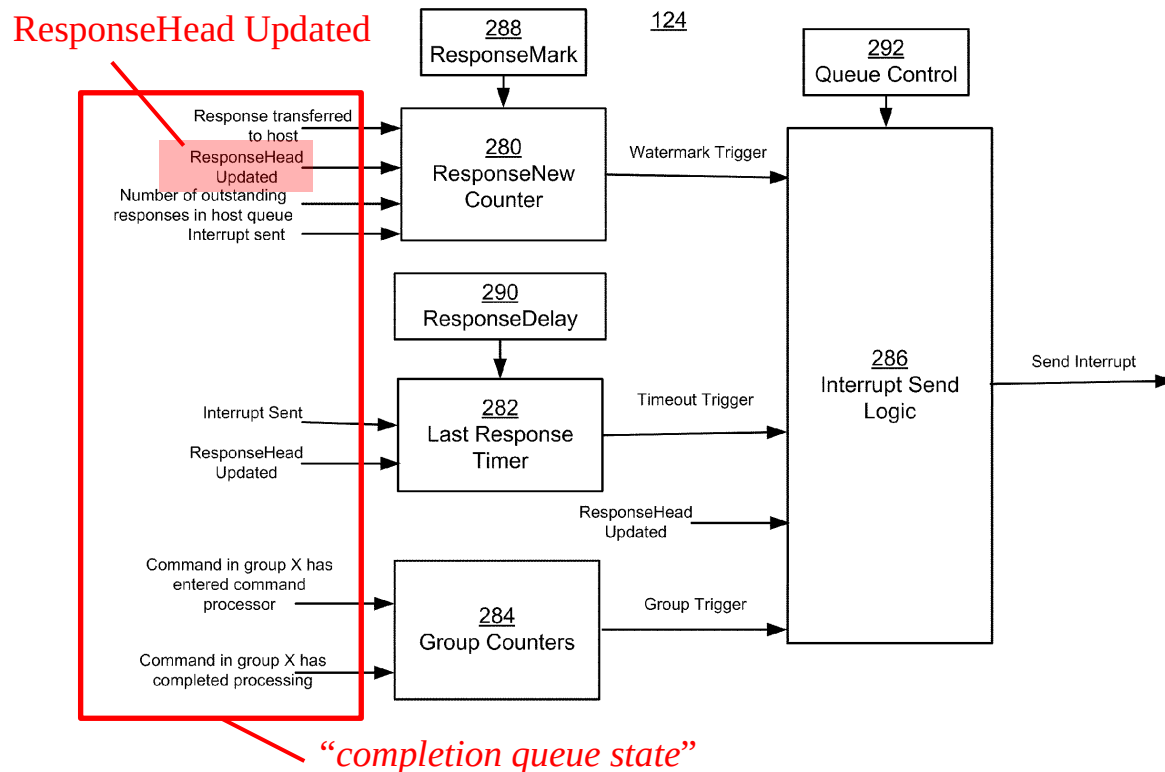
See [1.4]. Ex.1003, ¶197.

20. Claim 18

[18.1] *The method of claim 16, wherein the completion queue event is the host processing unit updating a head pointer stored in the nonvolatile memory controller for the completion queue.*

As explained above at [1.1], Borchers receives status information for the response queue (“*completion queue*”). This status information includes that the host has updated the head pointer of the response queue. During operation, “[t]he host 106 is configured to read the responses from the response buffer 123 and update the head pointer in the MMIO space of the data storage device to indicate

that the host has received the response.” Ex.1005, [0035].



Borchers, Fig. 2 (annotated); Ex.1003, ¶198.

Accordingly, because the response queue status information (“*completion queue state*”) includes an indication that the head pointer of the response queue has been updated, Borchers renders this limitation obvious. Ex.1003, ¶198-99.

D. Ground 2: Claims 1-18 are obvious in view of Borchers and the PCI standards.

Ground 1 shows how Borchers renders obvious each of the challenged claim limitations. Ground 1 further relies on the PCIe/PCI standards as evidence of the background knowledge of a POSITA. To the extent Patent Owner argues that the

PCIe/PCI standards would not have been within the background knowledge of a POSITA, Ground 2 is presented to show that combining the teachings of the PCIe/PCI standards with Borchers would have been obvious to a POSITA. Ex.1003, ¶200.

1. Summary of the PCI Standards

The PCI Express 2.0 Base Specification document “describes the PCI Express architecture, interconnect attributes, fabric management, and the programming interface required to design and build systems and peripherals that are compliant with the PCI Express specification.” Ex.1007, 21. “The PCIe Standard states that “[t]he goal is to enable such devices from different vendors to inter-operate in an open architecture.” Ex.1007, 21.

As an example, the PCIe Standard describes the structure of interrupt signals. PCIe describes a “Message Signaled Interrupt (MSI/MSI-X)” which are “Two similar but separate mechanisms that enable a device to request service by writing a system-specified DWORD of data to a system-specified address using a Memory Write Request. Compared to MSI, MSI-X supports a larger maximum number of vectors and independent message address and data for each vector.” Ex.1007, 26. *See also* Ex.1007, 458; Ex.1003, ¶¶201-06.

2. Reasons to combine the PCI standard with Borchers

A POSITA would have found it obvious to implement Borchers’ techniques

according to standardized practices such as those defined in the PCIe/PCI standards. Ex.1003, ¶207.

Borchers describes a known interface device for communication between a host and memory controller. *See generally*, Ex.1005. Borchers explains that “the high speed interface may include a PCIe interface.” Ex.1005, [0110]. “The PCIe interface 108 may include a connector to the host 106 such as, for example, a PCIe connector cable assembly. Other high speed interfaces, connectors and connector assemblies also may be used.” Ex.1005, [0110].

Accordingly, a POSITA would have looked to known techniques for implementing a PCI Express interface. It would have been obvious to look to the known standards documentation such as the PCI Express Base Standard and the PCI standard. Indeed, the PCI Express standard states that “describes the PCI Express architecture, interconnect attributes, fabric management, and the programming interface required to design and build systems and peripherals that are compliant with the PCI Express specification.” Ex.1007, 21. Accordingly, it would have been natural for a POSITA to implement Borchers’ memory interface 108 in accordance with industry standards. Ex.1003, ¶209.

For example, one aspect of the memory interface is how it implements interrupt signals. Borchers explains that “The interrupt processor 124 is configured to signal the host 106 with an interrupt when new responses are available in the

response buffer 123.” Ex.1005, [0035]. A POSITA would have found it obvious to thus implement the interrupt signals according to the PCI Express standard. As stated in the PCI Express standard, “[a]ll PCI Express device functions that are capable of generating interrupts must implement MSI or MSI-X or both.” Ex.1007, 453. “MSI and the MSI Capability structures are defined in the PCI Local Bus Specification, Revision 3.0.” Ex.1007, 453. PCIe describes a “Message Signaled Interrupt (MSI/MSI-X)” which are “Two similar but separate mechanisms that enable a device to request service by writing a system-specified DWORD of data to a system-specified address using a Memory Write Request. Compared to MSI, MSI-X supports a larger maximum number of vectors and independent message address and data for each vector.” Ex.1007, 26. *See also* Ex.1007, 458. Ex.1003, ¶210.

The PCI Local Bus Specification also explains that MSI and MSI-x interrupts use vectors. “System software initializes the message address and message data (from here on referred to as the ‘vector’) during device configuration, allocating one or more vectors to each MSI capable function.” Ex.1006, 231. Accordingly, it would have been obvious that Borchers’ interrupt signals, implemented according to the PCI Express standard, would have used interrupt vectors. Ex.1003, ¶211. Indeed, the combination is nothing more than “the predictable use of prior art elements according to their established functions.”

KSR Int'l v. Teleflex Inc., 550 U.S. 398, 417 (2007).

Accordingly, the combination of Borchers and the PCIe/PCI standards would have predictably resulted in interrupt signals implemented using interrupt vectors. A POSITA would have had a reasonable expectation of success because the PCIe/PCI standards are tried-and-true, industry vetted implementations. The PCIe standard is “an enhancement to the PCI architecture” which was “the most widely accepted and implemented expansion standard in the world.” Ex.1007, 21; Ex.1006, 15. Ex.1003, ¶212.

Thus, the combination of Borchers and the PCIe/PCI standards are merely applying a known technique (interrupt signals according to PCIe/PCI standards) to a known device (Borchers’ memory interface) ready for improvement to yield predictable results (interrupt signals with interrupt vectors). Ex.1003, ¶¶207-13.

3. Claim Analysis for claims 1-18

The claim analysis for Ground 2 is substantially the same as that of Ground 1. *See supra* X.C; Ex.1003, ¶214.

E. Ground 3: Claims 1-18 are obvious in view of Borchers, the PCIe/PCI standards, and Serebrin.

Grounds 1 and 2 rely on the background knowledge of a POSITA that the timer values, counter values, and other data that represent response queue status information (“*completion queue state*”) and interrupt mechanism information

(“*interrupt vector state*”) would be stored in some type of storage. It would have been obvious for this storage to be a register, flag, or other form of memory. To the extent Patent Owner argues that such is not background knowledge of a POSITA, Ground 3 shows that it would be obvious for an interrupt processor to include storage such as registers to temporarily store such status information, as evidenced by Serebrin. Ex.1003, ¶215.

1. Summary of Serebrin

Like Borchers and the ’968 patent, Serebrin relates to “a device interrupt manager for a “memory management unit.” Ex.1008, [0008]. Serebrin provides evidence that it was known for interrupt managers to use cache or registers to store state information. Ex.1003, ¶¶215-19

2. Serebrin is Entitled to its Provisional Filing Date.

Serebrin’s provisional application (Ex.1009) is nearly identical to its specification and thus provides written description support for at least one claim as demonstrated in the chart below.

Serebrin Publication, Claim 1	Serebrin Provisional.
A device interrupt manager configured to receive an interrupt from a device that is assigned to a guest,	“A device interrupt manager configured to receive an interrupt from a device that is assigned to a guest.” Ex.1009, 48.

wherein the device interrupt manager is configured to transmit an operation for recordal of the interrupt in a memory location,	“The device manager may be configured to record the interrupt in a guest interrupt controller data structure.” Ex.1009, [0023], 10.
wherein the memory location is associated with a virtual processor within the guest,	More particularly, the device interrupt manager may be configured to detect which vCPU within the guest is targeted by the interrupt. The device manager may be configured to record the interrupt in a guest interrupt controller data structure. Ex.1009, [0023], 10.
wherein the virtual processor is targeted by the interrupt.	A processor or vCPU may be targeted by an interrupt if the interrupt is to be received by the interrupt controller associated with the processor/vCPU. Ex.1009, [0027], 12.

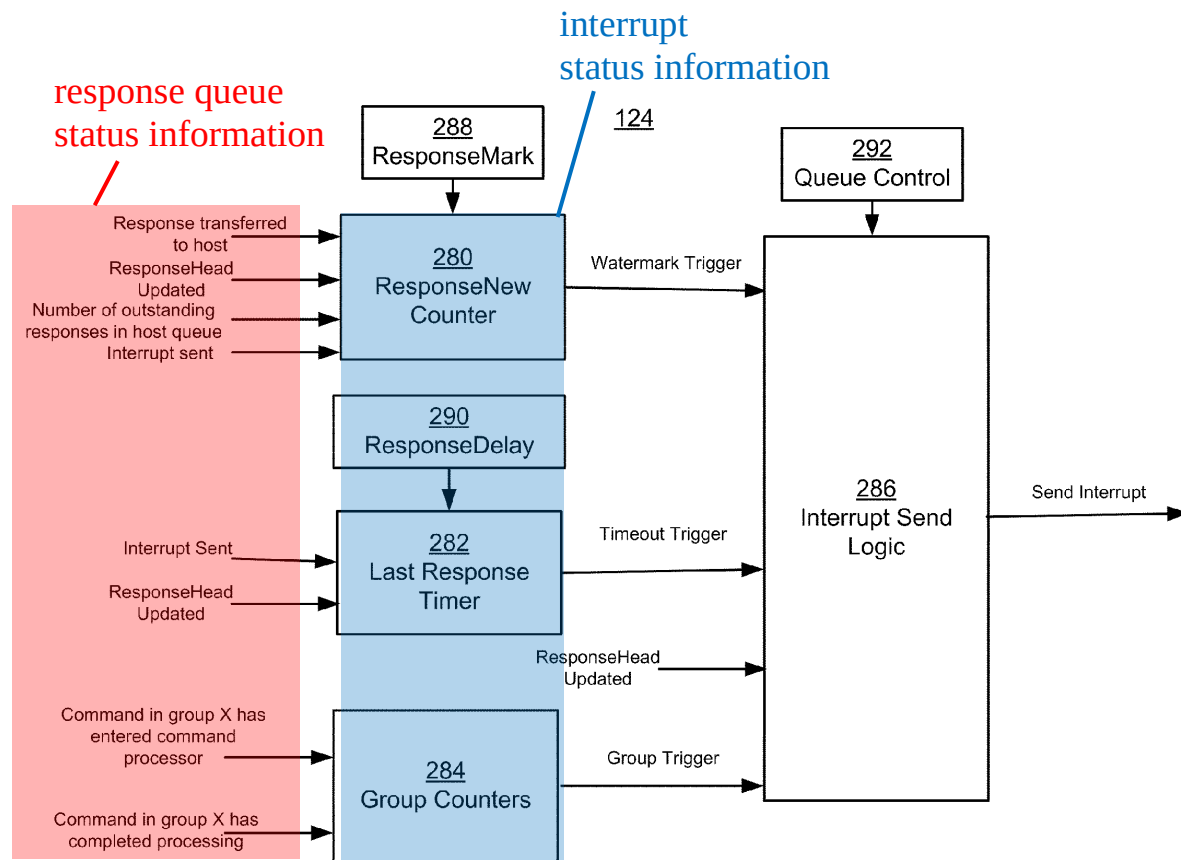
Accordingly, because the Serebrin Provisional provides written description support for each element of the claims, it is entitled to the filing date of its provisional application. The following analysis cites to both Serebrin and the corresponding teaching in the Serebrin provisional. Ex.1003, ¶¶220-22.

3. Reasons to combine Serebrin with Borchers and the PCIe/PCI standards

A POSITA would have found it obvious for Borchers' interrupt processor to utilize cache or registers to store state information, as evidenced by Serebrin.

Ex.1003, ¶223.

As described above at X.C.1, Borchers' memory controller includes an interrupt processor 124. The interrupt processor 124 relies on status information from the host's response queue. The status information is then used by the interrupt processor 124 to maintain interrupt status information (e.g., timers and counters) for determining when to send an interrupt signal to the host. *See* Ex.1005, [0060].

**Ex.1005, Fig. 2 (annotated); Ex.1003, ¶224.**

A POSITA would have understood that both the response queue status information and the interrupt status information would be stored or buffered in some type of storage location, such as a cache or register. Ex.1003, ¶225. Indeed, it was known for interrupt managers to use caches or registers to store state information. Serebrin provides an example of using caches or registers to store state information. Indeed, the combination is nothing more than “the predictable use of prior art elements according to their established functions.” *KSR* 550 U.S. at 417 (2007).

Serebrin describes “a memory controller 42 and an input/output (I/O) memory management unit (IOMMU) 40 that further includes a device interrupt manager 38.” Ex.1008, [0051]; Ex.1009, 19. The interrupt manager is connected to memory 56 as shown in Fig. 2 below. The memory 56 stores gAPIC (guest Advanced Programmable Interrupt Controller) states. The “device interrupt manager 38 may be configured to record each guest interrupt received in the bridge 36 in the gAPIC state data structure 58 [and] update the gAPIC state in the gAPIC state data structure 58.” Ex.1008, [0055]; Ex.1009, 21. Serebrin explains that a variety of forms of memory such as cache or registers may be used to store the interrupt state information. *See e.g.*, Ex.1008, [0057]; Ex.1009, 22.

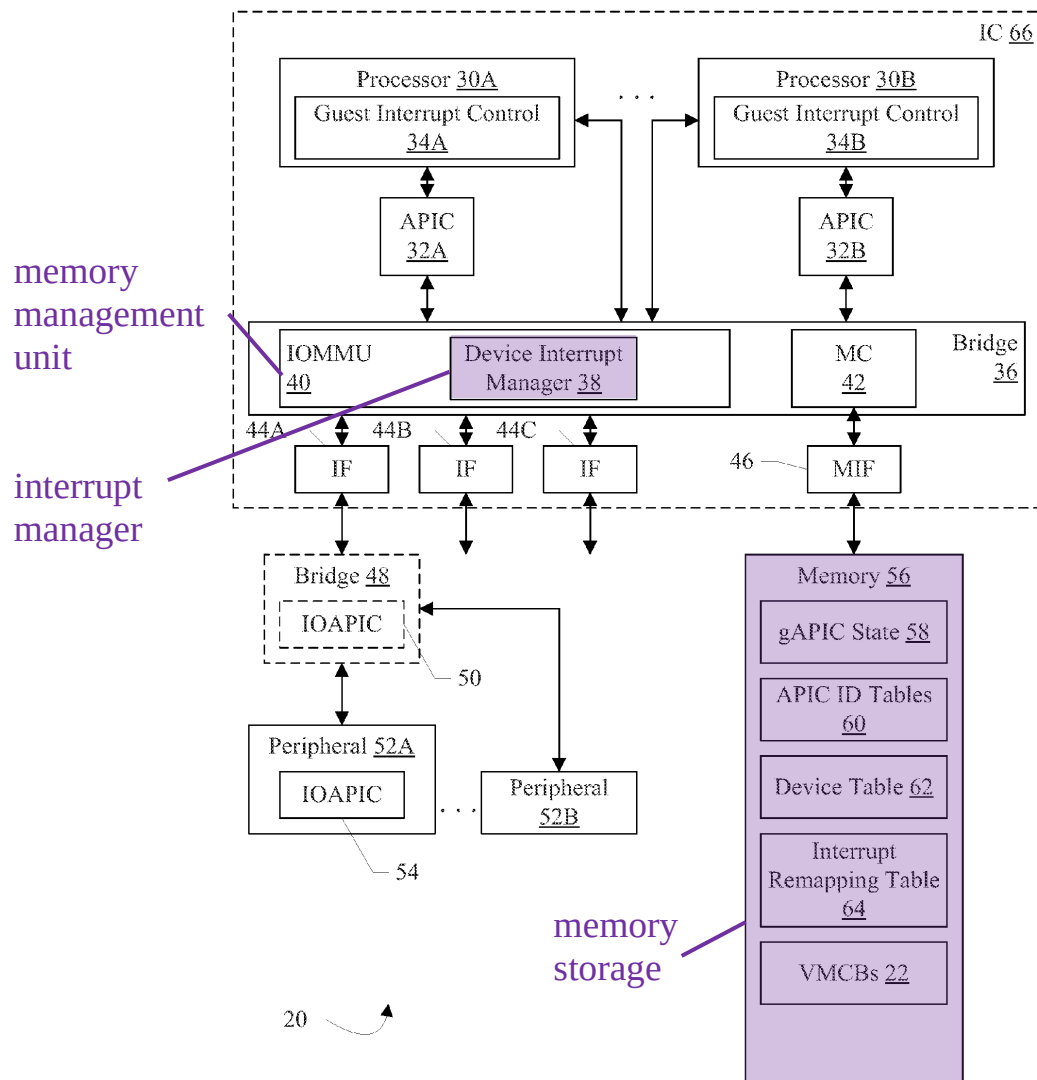


Fig. 2

Ex.1008, Fig. 2 (annotated); Ex.1003, ¶226.

Accordingly, a POSITA would have found it obvious for Borchers' interrupt manager to similarly include cache/registers for storing state data. Ex.1003, ¶227. The combination of Serebrin and Borchers thus predictably results in Borchers' response queue status information and interrupt mechanism information being placed in storage such as cache or registers.

A POSITA would have had a reasonable expectation of success given that Serebrin stores similar types of state information as Borchers. Ex.1003, ¶228. In particular, Serebrin’s interrupt manager stores state information such as “the interrupt requests that have been transmitted to the gAPIC” and “internally-generated interrupts, timers, the local vector table, etc.” Ex.1008, [0090]-[0094]; Ex.1009, 34-35.

Accordingly the combination of Serebrin with the teachings of Borchers is merely applying a known technique (Serebrin’s cache/registers) to a known device (Borchers’ interrupt manager) ready for improvement to yield predictable results (storing state information in cache/registers). Ex.1003, ¶¶223-29.

4. Claim Analysis for claims 1-18

The claim analysis for Ground 3 is substantially the same as that of Ground

1. *See supra* X.C. Ex.1003, ¶230.

XI. DISCRETIONARY DENIAL IS NOT WARRANTED

Petitioner respectfully submits that the Board should not exercise its discretion under 35 U.S.C. §§314(a) or 325(d) to deny this Petition.

A. The Fintiv factors favor institution.

Denial would be improper based on factors in *Apple v. Fintiv*, IPR2020-00019, Paper 11 (P.T.A.B. Mar. 20, 2020) (precedential).

1. No evidence regarding a stay

No motion to stay has been filed, so the Board should not infer the outcome of such a motion. Thus, this factor is neutral on discretionary denial.

2. Parallel proceeding trial date

This factor weighs against discretionary denial because no trial date has currently been scheduled. Moreover, the projected trial date—based on median time-to-trial statistics—is in January of 2027³, which is well after the projected date for the Board to issue a Final Written Decision in July 2026. Because the projected trial date is approximately six months *after* the Board’s expected date for issuing a Final Written Decision, this factor weighs against discretionary denial.

3. Investment in the parallel proceeding

The investment in the co-pending litigation has been minimal. No schedule has been set. Thus, the Markman hearing is unlikely to occur before the Board issues an institution decision. This lack of investment favors institution.

4. Overlapping issues with the parallel proceeding

The co-pending litigation is in its early stages. Petitioner served its preliminary invalidity contentions on December 16, 2024. However, Petitioner has

³ The current average time-to-trial for the district court hearing the co-pending litigation is 30.4 months. *See* Ex.1011, Ex.1012.

not served its final invalidity contentions, nor has the deadline for doing so been set. The extent of overlap is thus speculative at this point in time.

5. Petitioner is a defendant

Petitioner is a defendant in the co-pending litigation. That is true of most Petitioners in IPR proceedings, making this factor neutral.

6. Other circumstances

“[T]he PTAB will not deny institution of an IPR or PGR under *Fintiv* (i) when a petition presents compelling evidence of unpatentability.” Ex.1013, 9. Here, the petition—along with Dr. Min’s expert testimony—plainly shows that the ’968 patent claims no more than known concepts related to interrupt coalescing.

B. Advanced Bionics Test Favors Institution.

Denial under 35 U.S.C. § 325(d) is not warranted because the challenges presented in this petition are neither cumulative nor redundant to the prosecution of the ’968 patent.

Under the first prong of the *Advanced Bionics* framework, Petitioner acknowledges that Borchers was cited in an IDS provided by the Applicant. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 7-8 (Feb. 13, 2020) (precedential).

Under the second prong, however, the evidence shows that the Examiner “erred in a manner material to the patentability of challenged claims.” *Id.* The

second prong is guided by *Becton, Dickinson* factors (c), (e), and (f). *Id.* at 9-10, n. 10 (citing *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (Dec. 15, 2017)). These factors weigh against exercising discretion.

With respect to factor (c), Borchers was never used in a rejection nor discussed at all by the Examiner. Borchers' inclusion in an IDS does not show that Borchers was given serious evaluation by the Examiner. *See Navistar, Inc. v. Fatigue Fracture Tech., LLC*, IPR2018-00853, Paper 13 at 17 (Sept. 12, 2018) ("...the fact that [references] were of record... provides little impetus... to deny institution under § 325(d)").

With respect to factors (e) and (f), the Examiner erred by overlooking Borchers' teaching with respect to interrupt coalescing. While Borchers does not refer to certain items as a "doorbell update status," a POSITA would have recognized that Borchers' response head update is a "doorbell update" status as evidenced by at least the background knowledge of a POSITA evidenced in the PCI standards. This Petition presents the PCI standards as additional evidence, along with Dr. Min's testimony, to show that Borchers teaches what is claimed. *See, e.g., Puma N. Am., Inc. v. Nike, Inc.*, IPR2019-01058, Paper 10, 19 (PTAB Oct. 31, 2019) (instituting where petition presented "new non-cumulative evidence.... helpful to our consideration of a prior art combination that was not

before the Examiner”). Accordingly, discretionary denial under 325(d) is not warranted.

XII. CONCLUSION

Petitioner has established a reasonable likelihood that the Challenged Claims are unpatentable.

Respectfully submitted,

Dated: January 24, 2025
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XIII. MANDATORY NOTICES**A. Real Party-in-Interest**

The real parties-in-interest (“RPI”) are Sandisk Technologies, Inc. and Western Digital Technologies, Inc. (“Petitioner”).

B. Related Matters

Pursuant to 37 C.F.R. § 42.8(b)(2), to the best knowledge of the Petitioner, the ’968 patent is or was involved in the following cases:

Case Heading	Number	Court	Filed	Status
<i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i>	2-24-cv-02864	CDCA	April 9, 2024	Pending
<i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i>	1-24-cv-00101	WDTX	January 30, 2024	Pending

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Please address all correspondence in this proceeding to lead and back-up counsel. Petitioner consents to service in this proceeding by email at the addresses above

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), Petitioner hereby certifies, in accordance with and reliance on the word count provided by the word-processing system used to prepare this Petition, that the number of words in this paper is 13,987. Pursuant to 37 C.F.R. § 42.24(d), this word count excludes the table of contents, table of authorities, mandatory notices under § 42.8, certificate of service, certificate of word count, appendix of exhibits, and any claim listing.

Dated: January 24, 2025

/David M. O'Dell/

David M. O'Dell
Lead Counsel for Petitioner
Registration No. 42,044

CERTIFICATE OF SERVICE

The undersigned certifies that, in accordance with 37 C.F.R. § 42.6(e) and 37 C.F.R. § 42.105, service was made on Patent Owner as detailed below.

Date of service January 24, 2025

Manner of service FEDERAL EXPRESS

Documents served Petition for *Inter Partes* Review Under 35 U.S.C. § 312 and 37 C.F.R. § 42.104 of U.S. 8,554,968; Petitioner's Power of Attorney; Petitioner's Exhibit List; All Exhibits.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND
WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioners

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner

Case IPR2025-00517
U.S. Patent No. 8,554,968

**PATENT OWNER POLARIS POWERLED TECHNOLOGIES, LLC'S
BRIEF ON DISCRETIONARY DENIAL**

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PATENT OWNER'S EXHIBIT LIST

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2001	List of Docket Entries, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 1-24-cv-00101 (W.D. Tex.)
2002	List of Docket Entries, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal)
2003	List of Docket Entries, <i>Micron Technology Inc. et al. v. Polaris PowerLED Techs., LLC</i> , 1-25-cv-00073 (D. Idaho)
2004	Scheduling and Case Management Order, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Jan. 27, 2025), ECF No. 54
2005	Western Digital's Notice of Motion and Motion to Stay Action Pending <i>Inter Partes</i> Review, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Feb. 3, 2025), ECF No. 58
2006	Minute Order, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Feb 3, 2025), ECF No. 59
2007	Plaintiff's Opposition to Motion to Stay, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Feb. 10, 2025), ECF No. 60
2008	Patent L.R. 3-3 and 3-4 Invalidity Disclosures of Western Digital Defendants, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal), ECF No. 60-3 and Appendices A-C of the Invalidity Disclosures
2009	Defendants' Identification of Claim Terms for Construction, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal), ECF No. 60-4
2010	Stipulated Protective Order, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal), ECF No. 61

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Exhibit No.	Description
2011	Western Digital's Reply in Support of Motion to Stay Action Pending <i>Inter Partes</i> Review, <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal Feb. 14, 2025), ECF No. 62
2012	USPTO Appeal Statistics (Mar. 31, 2025), <i>available at</i> https://www.uspto.gov/patents/ptab/statistics
2013	Patent Trial & Appeal Board (PTAB) Dashboard, <i>available at</i> https://www.uspto.gov/dashboard/ptab/
2014	Press Release: Sandisk Celebrates Nasdaq Listing After Completing Separation from Western Digital (Feb. 24, 2025), <i>available at</i> https://shop.sandisk.com/company/newsroom/press-releases/2025/sandisk-celebrates-nasdaq-listing-after-completing-separation
2015	U.S. Provisional Patent Application No. 61/374,242
2016	Redline Comparison Between U.S. Patent Application No. 12/756,477 and U.S. Patent Application No. 12/537,733
2017	U.S. Patent No. 10,296,249 to Benisty
2018	IDS Submitted in U.S. Application No. 15/585,808
2019	NVM Express, Revision 1.0 (Mar. 1, 2011), <i>available at</i> https://web.archive.org/web/20110305032748/www.intel.com/standards/nvmhci
2020	U.S. Patent No. 7,620,784 to Panabaker
2021	U.S. Patent No. 8,244,946 to Gupta <i>et al.</i>
2022	U.S. Patent Application Publication No. 2008/0320214 to Ma <i>et al.</i>
2023	U.S. Patent Application Publication No. 2010/0185808 to Yu <i>et al.</i>
2024	Defendants' Identification of Claim Terms for Construction (Apr. 18, 2025), <i>Polaris PowerLED Techs., LLC v. Western Digital Corp. et al.</i> , 2-24-cv-02864 (C.D. Cal. Feb. 10, 2025)

I. INTRODUCTION

The Board should exercise its discretion under 35 U.S.C. § 314(a) and *Fintiv* to deny institution of this *inter partes* review (IPR) because the same parties are in advanced stages of litigating the validity of this patent in district court. The district court jury trial is scheduled for June 16, 2026—more than two months *before* the Board’s projected deadline for issuing a final written decision. Litigating the same issues at the Board would therefore be duplicative and contrary to the intent of IPRs for “providing a more efficient system for challenging patents” and “reducing unwarranted litigation costs.” H.R. Rep. No. 112-98 at 39-40 (2011); *see also NHK Spring Co. Ltd. v. Intrix-Plex Techs., Inc.*, IPR2018-00752, Paper 8 at 19-20 (P.T.A.B. Sept. 12, 2018) (precedential).

Other considerations also strongly favor discretionary denial. For example, the record strongly indicates that Petitioners’ primary reference for all three grounds in this IPR, Borchers, is likely later in time than the priority date of the ’968 patent. Borchers has a date of April 8, 2010. But the provisional patent application of the ’968 patent (EX2015), filed August 16, 2010, attaches extensive data sheets and technical product documentation, including materials from earlier than April 8, 2010. This demonstrates that the inventors had already fully developed their R&D program and were working toward semiconductors that practiced the ’968 patent’s claimed inventions. The dispute surrounding whether

Borchers is eligible as prior art or is antedated will require substantial discovery—including third-party discovery. The district court case is better positioned to handle this fact-intensive discovery.

Additionally, Petitioners have not agreed to a *Sotera* stipulation or identified any reason why instituting an IPR would reduce the number of issues litigated in district court. Since the district court trial is already scheduled and instituting an IPR would not improve judicial efficiencies, the Board should deny institution and focus its limited resources on other pending cases at the Board.

Compounding the case for denial, the Board is also on firm ground to deny institution under 35 U.S.C. § 325(d). The Petition's Grounds of Unpatentability rely on the same primary reference (Borchers), substantially the same art (the PCI standards), and art that is cumulative and insignificant (Serebrin) to the art considered during prosecution. And Petitioners have not established that the Office erred in a manner material to the patentability of the challenged claims. For this additional reason, the Board should exercise its discretion and *deny* institution.

II. THE BOARD SHOULD DENY INSTITUTION UNDER § 314(A).

A. The *Fintiv* factors favor discretionary denial.

When the patent owner raises an argument for discretionary denial due to an earlier trial date in a co-pending litigation, the Board weighs the following factors:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;

2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board's exercise of discretion, including the merits.

Apple Inc. v. Fintiv, Inc., IPR2020-00019, Paper 11 at 5-6 (P.T.A.B. Mar. 20, 2020) (precedential) ("*Fintiv*"). These factors, when considered as a whole, support *denying* institution. Factor 1 is neutral, factors 2-6 all weigh in favor of denial, and no factor weighs against exercising the Board's discretion to deny institution.

1. Factor 1 is, at worst, neutral because there is no evidence a stay order will be granted in the district court.

Under the first factor, if the district court stays the case or provides guidance that it will stay the case and await the Board's final resolution of the patentability issues, this fact usually weighs against exercising authority to deny institution. *Fintiv*, 7. However, here, the district court has not provided such guidance and issued a scheduling order to continue through trial. EX2004.

Actions in the district court indicate that a stay is *not* imminent because the case is moving faster than initially scheduled. On January 27, 2025, the district court issued its scheduling and case management order, which set the deadlines to

file infringement contentions and invalidity contentions as February 18, 2025, and April 4, 2025, respectively. EX2004, 26. After Western Digital filed a motion to stay the case (EX2005), the parties decided to advance the case by jointly stipulating to serve, before they were due, amended infringement and invalidity contentions. EX2006.

The amended infringement and invalidity contentions were served early to resolve a discovery dispute over the scope of accused products. Polaris's initial infringement contentions, served in October 2024, accused all Western Digital and SanDisk solid-state drive products from 2018 onward supporting NVMe, among other features, and included a list of exemplar product lines. Western Digital challenged the sufficiency of these contentions, arguing they lacked adequate detail for products beyond WD Black-branded SSDs, and consequently limited its discovery production to only those SSDs. To break this impasse and advance discovery on the full scope of accused products, Polaris prepared and sent proposed amended infringement contentions to Western Digital. These amended contentions included significantly expanded claim charts, reflecting a substantial increase in detail about exemplary SSD product lines. Polaris maintained that its initial contentions were sufficient and compliant with applicable rules, and the amended contentions were offered to address Western Digital's concerns and resolve the dispute amicably. Western Digital acknowledged that the proposed

amended contentions addressed its concerns about detail but conditioned its agreement to Polaris' service of these contentions on Polaris allowing Western Digital to serve amended invalidity contentions. Western Digital claimed its December 2024 invalidity contentions inadvertently omitted certain details and sought to amend them. After negotiations, the parties reached an agreement and submitted a stipulation to the Court on February 3, 2025. That same day, the Court approved the stipulation, permitting both Polaris' amended infringement contentions and Western Digital's amended invalidity contentions. As ordered, the parties exchanged the amended infringement and invalidity contentions early.

The parties also exchanged proposed terms for construction earlier than required. EX2002 (deadline for exchange April 18, 2025); EX2009 (identification of claim terms served on January 24, 2025). Such proactive measures show that the district court case is advancing according to schedule (if not faster).

Western Digital's motion to stay the district court case (EX2005) is still pending, but there is no indication that the court will grant the motion. In fact, the district court canceled the hearing on the motion. EX2002, ECF No. 63. And the court has denied motions to stay in cases—like this one—where the defendant waited almost a year after it was served with a complaint to file an IPR petition. Order Denying Defendant Skechers U.S.A., Inc.'s Motion to Stay Pending *Inter Partes* Review at 2, *Nike, Inc. v. Skechers U.S.A., Inc.*, 2-19-cv-9230 (C.D. Cal

Dec. 30, 2020), ECF No. 82 (“Defendant waited almost a year after it was served with the Complaint to file its IPR petitions. Defendants’ delay in filing its IPR petitions also weighs against granting a stay.”) (citation omitted); Order Denying Defendant’s Motion to Stay at 5, *Jiaying Super Lighting Elec. Appliance Co., Ltd. et al. v. MaxLite, Inc.*, 2-19-cv-4047 (C.D. Cal June 17, 2020), ECF No. 73 (“Such a delay cuts against granting a stay because ‘courts expect accused infringers to evaluate whether to file, and then to file, IPR petitions as soon as possible after learning that a patent may be asserted against them.’”) (citation omitted).

Regardless of Western Digital’s arguments in favor of a stay (EX2005, EX2011), there is no specific evidence that the district court will stay the case. “In the absence of specific evidence, [the Board] will not attempt to predict how the district court in the related district court litigation will proceed because the court may determine whether or not to stay any individual case . . . based on a variety of circumstances and facts beyond [the Board’s] control and to which the Board is not privy.” *Sand Revolution II, LLC v. Continental Intermodal Group – Trucking LLC*, IPR2019-01393, Paper 24 at 7 (P.T.A.B. June 16, 2020) (informative). The first *Fintiv* factor is therefore, at worst, neutral. *Id.*; *Fintiv*, 6-9.

2. Factor 2 favors discretionary denial because the district court’s trial date is scheduled to occur before the projected final written decision.

The second factor weighs in favor of denying institution because the district

court's scheduled trial date is before the Board's projected statutory deadline. See *Fintiv*, 9. The district court scheduled trial for June 16, 2026. EX2004, 25. This trial date is *before* the Board's projected final written decision. Polaris's POPR is due May 27, 2025.¹ An institution decision is then due August 27, 2025. 35 U.S.C. § 314(b). If instituted, that timeline would make the final written decision due August 27, 2026—more than two months *after* the district court's trial date. 35 U.S.C. § 316(a)(11). "If the court's trial date is earlier than the projected statutory deadline, the Board generally has weighed this fact in favor of exercising authority to deny institution" *Fintiv*, 9. In *Fintiv*, a scheduled district court trial date two months before the projected final written decision—a similar timeframe—weighed in favor of discretionary denial. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 15 at 13 (P.T.A.B. May 13, 2020) (informative) ("*Fintiv II*").

Petitioners' statistical-based argument for a 2027 trial date is no longer relevant. In the petition, Petitioners projected a trial date in January 2027 based on the median time-to-trial for civil cases in the Central District of California. Pet., 88 n.3 (citing EX1012). But after Petitioners filed the petition, the court scheduled

¹ The POPR is due three months after the February 26th Notice of Filing Date. 37 C.F.R. § 42.107(b). May 26th is a Federal holiday, which makes the POPR due the next business day. 37 C.F.R. § 1.7(a).

trial for June 16, 2026. EX2004, 25. Nothing in the district court record indicates that the court intends to deviate from this schedule. To the contrary, the court stated that this date was “firm.” EX2004, 1.

The second *Fintiv* factor therefore weighs in favor of discretionary denial as it did in *Fintiv*. *Fintiv*, 9; *Fintiv II*, 13.

3. Factor 3 favors denial because the parties have already invested substantial resources in the parallel proceedings.

Under the third *Fintiv* factor, “[t]he Board also has considered the amount and type of work already completed in the parallel litigation by the court and the parties *at the time of the institution decision*.” *Fintiv*, 9 (emphasis added). The deadline for issuing an institution decision is August 27, 2025. *Supra* Section II.A.2. By this date, substantial work will have already been done, including final invalidity contentions, all discovery and briefing for claim construction, and the Markman hearing. This heavy investment by the parties and the district court favors denial of institution. *Fintiv*, 9-12.

Work Performed to Date:

- January 30, 2024: Polaris filed a complaint for patent infringement in the Western District of Texas. EX2001, ECF No. 1.
- April 9, 2024: Polaris re-filed the case in the Central District of California to resolve a threatened motion to transfer. EX2002, ECF No. 1. Polaris dismissed its Western District of Texas (W.D. Tex.) case on April 5, 2024, and refiled in the Central District of California (C.D. Cal.) on April 9, 2024, at Western Digital’s suggestion, to resolve a venue dispute and avoid related motion practice costs. Western Digital proposed a stipulated dismissal

without prejudice for transfer to C.D. Cal. because Western Digital argued that W.D. Tex. was an improper venue.

- June 21, 2024: Polaris filed an amended complaint. EX2002 at ECF No. 40. The complaint included claim charts detailing alleged infringement of claims 1-3, 6-11, and 14-18 of the '968 patent. *See* EX2002, ECF No. 40-4.
- October 2, 2024: Polaris served its first sets of requests for production and interrogatories. *See* EX2007, *22.
- October 2, 2024: Polaris served its initial infringement contentions and accompanying document production. *See* EX2007, *22. The initial infringement contentions again identified the asserted claims. EX2008, *3.
- June 5, 2024: Western Digital filed answers to the amended complaint. EX2002, ECF Nos. 43-45.
- November 1, 2024: Western Digital responded to requests for production. *See* EX2007, *22.
- November 22, 2024: Western Digital responded to interrogatories. *See* EX2007, *22.
- December 16, 2024: Western Digital served invalidity contentions and accompanying document production. EX2008. The contentions charted 16 references for the '968 patent, cited numerous other references, and cited product art from different companies. *Id.*, *53-59. The contentions also analyze the motivation to combine for different combinations. *Id.*, *57-64. They also provide contentions under §§ 101 and 112. *Id.*, *64-71. In total, the invalidity contentions comprise over 3,000 pages. *See* EX2007, *22.
- January 24, 2025: Western Digital identified terms for construction, including six terms for the '968 patent. EX2009.
- February 4, 2025: Polaris had served amended infringement contentions that identified the asserted claims again. *See* EX2007, *22.
- February 6, 2025: Western Digital served amended invalidity contentions. *See* EX2007, *22.
- February 11, 2025: The court ordered entry of the protective order. EX2010.

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- April 18, 2025: Western Digital served Defendants’ Identification of Claim Terms for Construction, which this time included seven terms for the ’968 patent. EX2024, *2-3.

Additional Work To Be Completed Before the Institution Decision (EX2004, 26):

- May 9, 2025: Preliminary Claim Constructions and Extrinsic Evidence Due
- May 24, 2025: Damages Contentions Due
- June 3, 2025: Joint Claim Construction, Prehearing Statement, and Expert Reports on Claim Construction Due
- June 23, 2025: Responsive Damages Contentions Due
- July 3, 2025: Claim Construction Discovery Cutoff
- July 18, 2025: Claim Construction Opening Briefs Due
- July 23, 2025: Damages Contentions Meeting Deadline
- July 28, 2025: Deadline to Amend Pleadings or Add Parties
- August 1, 2025: Claim Construction Responsive Briefs Due
- August 8, 2025: Claim Construction Reply Briefs Due
- August 22, 2025: Markman Hearing

For the work scheduled between filing this brief and the deadline of the institution decision, the district court has stated that “[t]hese dates and requirements are firm.” EX2004, 1. Based on the level of investment and effort already expended on claim construction and invalidity contentions in the district court, this factor weighs in favor of discretionary denial. *Fintiv II*, 14.

Under *Fintiv* factor 3, the Board also considers whether the petitioner could

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have filed the petition more expeditiously to avoid unnecessary investment by the parties and the court. *Fintiv*, 11. “[I]f the petitioner cannot explain the delay in filing its petition, these facts have favored denial.” *Fintiv*, 12; *Next Caller Inc. v. TRUSTID, Inc.*, IPR2019-00961, Paper 10 at 16 (P.T.A.B. Oct. 16, 2019) (weighing the petitioner’s unexplained delay in filing the petition in favor of denial and noting that had the petitioner filed the petition earlier, the PTAB proceeding may have resolved the issues before the district court).

Here, Petitioners could have filed the IPR petition well before substantial work started in the district court case. Western Digital Technologies, Inc. was first served with a complaint alleging infringement of the ’968 patent on January 30, 2024. EX2001 at ECF No. 1.² Polaris first identified the asserted claims on June 21, 2024, in its amended complaint, and then again on October 2, 2024, in its initial infringement contentions. *See* EX2002, ECF No. 40-4; EX2008, *3. So

² The litigation was originally filed in the Western District of Texas on January 30, 2024, as Case No. 1:24-cv-00101, but refiled in the Central District of California on April 9, 2024. The one-year time bar for filing an IPR petition is tied to the filing of the first case. *Click-To-Call Techs., LP v. Ingenio, Inc.*, *Yellowpages.Com, LLC*, 899 F.3d 1321, 1328 n.3 (Fed. Cir. 2018) (*en banc*), *vacated on other grounds*.

Western Digital first had notice of the asserted claims in June 2024. Rather than filing a petition in the early stages of the case after knowing the asserted claims, Petitioners waited *for about seven months* and filed the petition in the last possible week after substantial work ensued. Petitioners did not explain this lengthy delay in the Petition. This inexcusable delay makes factor 3 weigh even more in favor of denying institution. *Next Caller*, IPR2019-00961, Paper 10 at 16. It also makes a stay less likely. *Supra* Section II.A.1.

4. Factor 4 favors denial because there is substantial overlap between the IPR grounds and the invalidity contentions in the district court case.

The fourth *Fintiv* factor—overlap between issues raised in the petition and in the parallel proceeding—favors denying institution. “[I]f the petition includes the same or substantially the same claims, grounds, arguments, and evidence as presented in the parallel proceeding, this fact has favored denial.” *Fintiv*, 12. “Conversely, if the petition includes materially different grounds, arguments, and/or evidence than those presented in the district court, this fact has tended to weigh against exercising discretion to deny institution” *Id.*, 12-13.

Petitioners have relied on the same references in this IPR as the lead references in its invalidity contentions, showing that parallel proceedings would result in substantial overlap and duplicative work. The IPR grounds include four references: (1) U.S. Patent Application Pub. No. 2010/0262979 to Borchers *et al.*;

(2) PCI Local Bus Specification Revision 3.0; (3) PCI Express® 2.0 Base Specification Revision 0.9; and (4) U.S. Patent Application Pub. No. 2011/0197003 to Serebrin *et al.* Pet., 18-19. The first three claim charts in the invalidity contentions (C1-C3) rely on the same four references, as shown below.

Claim Charts in the Invalidity Contentions

Claim Chart	Reference
Chart C1	U.S. Pat. App. Pub. 2010/0262979 to Borchers <i>et al.</i>
Chart C2	PCI Local Bus Specification Revision 3.0
	PCI Express® 2.0 Base Specification Revision 0.9
Chart C3	U.S. Pat. App. Pub. 2011/0197003 to Serebrin <i>et al.</i>

Western Digital’s invalidity contentions rely on additional references (EX2008, *53-54), but “Petitioner’s assertion of additional invalidity contentions in the District Court is not relevant to the question of the degree of overlap for this factor.” *Fintiv II*, 15. “[B]ecause the identical claims are challenged based on the same prior art in both the Petition and in the District Court, this factor weighs in favor of discretionary denial in this case.” *Id.*

Western Digital has also not submitted any stipulation limiting the art that it can present at trial, which indicates that it intends to raise the same invalidity

positions in district court. *See Sand Revolution II*, IPR2019-01393, Paper 24 at 12 (“Petitioner’s stipulation, however, mitigates to some degree the concerns of duplicative efforts between the district court and the Board, as well as concerns of potentially conflicting decisions.”); *Sotera Wireless, Inc. v. Masimo Corp.*, IPR2020-01019, Paper 12 (P.T.A.B. Dec. 1, 2020) (precedential as to II.A) (“such a broad stipulation better addresses concerns of duplicative efforts and potentially conflicting decisions in a much more substantial way.”). Even if Western Digital were to submit a stipulation, it is too late—the Board’s discretionary panels should consider stipulations only if they are filed with sufficient time for a patent owner to address the impact of the stipulation in its discretionary denial brief. *See* FAQs for Interim Process for PTAB Workload Management, FAQ14; PTAB Boardside Chat on Interim Process for PTAB Workload Management (Apr. 17, 2025) (petitioners “*must*” file a stipulation within one month of the notice of filing date for consideration). Petitioners have had ample time to file a stipulation and have chosen not to. Factor 4 weighs in favor of denial on this basis alone.

Factor 4 also weighs in favor of denial because Western Digital relies on system prior art in its invalidity contentions, which prevents this case from being a “true alternative” to the district court proceeding. *Cf. Motorola Solutions, Inc. v. Stellar, LLC*, IPR2024-01205, Paper 19 at 3-4 (P.T.A.B. Mar. 28, 2025). In *Motorola*, the Director denied institution under 35 U.S.C. § 314(a) because

“Petitioner’s invalidity arguments in the district court are more expansive and include combinations of the prior art asserted in these proceedings with unpublished system prior art” *Id.*, 4.³ Similar here, Western Digital’s invalidity contentions include combinations of the asserted art with system prior art. *See* EX2008, *54-56 (relying on system prior art from numerous companies). For example, Western Digital has alleged invalidity based on Borchers and “Products that practice PCI Local Bus Specification Revision 3.0 or PCI Express® 2.0 Base Specification revision 0.9.” *Id.*, *56. Accordingly, this IPR would not be a “true alternative” to the district court case but instead litigate the same or (at best) substantially similar invalidity grounds.

The risk of duplicative litigation is even higher here because Western Digital Corporation is not a named petitioner, RPI, or privy, and may still try to raise the identical invalidity positions in the district court case. Petitioners appear to have strategically omitted the defendant Western Digital Corporation—the parent

³ In *Motorola*, the Director suggested that the petitioner’s stipulation “is not likely to moot” a combination of prior art asserted in the IPR proceeding and system prior art. *Motorola*, IPR2024-01205, Paper 19 at 4. Patent Owner takes no position whether a *Sotera* stipulation is not likely to moot such a combination of prior art. Regardless, Petitioners have not offered such stipulations here.

corporation of Western Digital Technologies, Inc.⁴—from the petition to evade estoppels.⁵ When Polaris raised this issue in briefing in the district court case (EX2007, *16), Western Digital Corporation tried to cure the issue by agreeing to estoppels. EX2011, *5. But it did so conditionally, stating: “[S]hould a stay be granted, Western Digital Corporation agrees to be bound under 35 U.S.C. § 315(e)(2).” *Id.* (emphasis added). If the court does not grant a stay, Western Digital Corporation could try to litigate the same grounds in district court.

For these reasons, the fourth *Fintiv* factor weighs strongly in favor of denying institution. *Fintiv*, 12. This inefficiency and duplication of efforts is

⁴ If the Board determines that Western Digital Corporation is an unnamed real party in interest or privy of Petitioners, Petitioners’ gamesmanship favors denying institution. *See* 35 U.S.C. §§ 312(a)(2).

⁵ Estoppels under 35 U.S.C. § 315(e)(2) apply only to a petitioner, real party in interest, or privy of the petitioner. Western Digital Corporation is not a petitioner, and is not listed as an RPI or privy of the petitioner. So Western Digital Corporation appears to be reserving an argument that it is not estopped in district court from raising the same grounds presented in the IPR, which further demonstrates that this IPR is not a “true alternative” to litigating validity before the district court.

precisely what the Board’s discretionary authority is intended to prevent. *NHK Spring*, IPR2018-00752, Paper 8 at 19-20; H.R. Rep. No. 112-98 at 39-40 (2011). And the Board should not permit Western Digital Corporation’s gamesmanship.

5. Factor 5 favors denial because the parties in the IPR overlap with the parties in the district court litigation.

Under the fifth *Fintiv* factor, “[i]f a petitioner is unrelated to a defendant in an earlier court proceeding, the Board has weighed this fact against exercising discretion to deny institution” *Fintiv*, 13-14. But here, both of the Petitioners are defendants or are related to a defendant in the co-pending litigation. Western Digital Technologies, Inc. is a defendant in the litigation. SanDisk Technologies, Inc. is a related party and real party in interest because it was owned by Western Digital as of the filing date of the petition. *See* EX2014 (announcing on February 24, 2025 its separation from Western Digital); Pet., 92 (“The real parties-in-interest (‘RPI’) are SanDisk Technologies, Inc. and Western Digital Technologies, Inc. (‘Petitioner’).”). Even if SanDisk were unrelated to a defendant, “if the issues are the same as, or substantially similar to, those already or about to be litigated, or other circumstances weigh against redoing the work of another tribunal, the Board may, nonetheless, exercise the authority to deny institution.” *Fintiv*, 14.

This factor therefore weighs in favor of denial. *Fintiv*, 13-14. And, if the Board deems SanDisk unrelated, it should still deny institution. *Id.*

6. Factor 6 favors denial, but Polaris will raise its merits arguments in the POPR.

Under the sixth *Fintiv* factor, the Board may consider other circumstances that impact the Board’s exercise of discretion, including the merits. *Fintiv*, 14-15. Polaris’s merits arguments will be in its Patent Owner Preliminary Response (POPR), which will explain why the grounds fundamentally misinterpret the invention and, as a result, fail to disclose numerous claim elements. The Director should consider these arguments when determining whether to exercise its discretion to deny institution under 35 U.S.C. § 314(a). See FAQs for Interim Process for PTAB Workload Management, FAQ8 (“The Director will receive each . . . POPR”), FAQ12 (“the Director will consider the merits in the merits briefing if the parties ask the Director to do so.”).

B. Other considerations also favor discretionary denial.

The Board’s Memorandum on the Interim Process for PTAB Workload Management presents additional considerations for discretionary denial, including:

Whether the PTAB or another forum has already adjudicated the validity or patentability of the challenged patent claims;

Whether there have been changes in the law or new judicial precedent issued since issuance of the claims that may affect patentability;

The strength of the unpatentability challenge;

The extent of the petition’s reliance on expert testimony;

Settled expectations of the parties, such as the length of time the claims have been in force;

Compelling economic, public health, or national security interests; and
Any other considerations bearing on the Director's discretion.

Interim Processes for PTAB Workload Management at 2 (Mar. 26, 2025). There are several considerations that weigh in favor of discretionary denial here.

1. The district court is better positioned for the discovery needed to antedate Borchers.

The record evidence strongly indicates that Borchers, the primary reference in all three grounds of unpatentability, was published later than the priority date of the '968 patent and would not be eligible as prior art.⁶ And establishing that the inventors conceived of the invention before Borchers' priority date and were diligent to a reduction to practice will be litigated fully in district court entailing fact-intensive discovery that is better suited for the district court, which has broader subpoena powers and broader protections for confidential information.

Petitioners allege that Borchers is prior art under (pre-AIA) 35 U.S.C. § 102(e) because it was filed on April 8, 2010, and published on October 14, 2010. Pet., 18. Petitioners do *not* allege that Borchers, as a continuation-in-part of an

⁶ Serebrin is also susceptible to antedating but appears only in Ground 3, so Polaris has focused on Borchers for the purposes of this discretionary denial brief.

earlier application, is entitled to an earlier filing date. *Id.*⁷ The earliest possible priority date of Borchers is therefore April 8, 2010.

The '968 patent's provisional application (U.S. Provisional Application No. 61/374,242) was filed on August 16, 2010. It contains 350 pages of specifications showing that the inventors had been developing a memory unit called the Delaware Non-Volatile Memory Host Controller Interface (NVMHCI) *before* Borchers' April 8, 2010 priority date. *See* EX2015.⁸ For example, the provisional application,

⁷ Borchers is not entitled to the August 7, 2009 filing date of U.S. Patent Application No. 12/537,733 (or its provisional applications) because substantial new matter was added when Borchers was filed as a CIP, including disclosure that Petitioners rely on (such as disclosure related to Figure 1C). *See* EX2016 (redline comparison between Borchers and U.S. Patent Application No. 12/537,733 to show new matter). Additionally, "[w]hen neither the PTO nor the Board has previously considered priority, there is simply no reason to presume that claims in a CIP application are entitled to the effective filing date of an earlier filed application." *PowerOasis, Inc. v. T-Mobile USA, Inc.*, 522 F.3d 1299, 1305 (Fed. Cir. 2008).

⁸ Despite the provisional application including evidence showing that the inventors were working on the NVMHCI before Borchers' April 8, 2010 filing date, Petitioners did not file the provisional application with the Petition.

although filed on August 16, 2010, includes specifications dated March 5, 2010 describing, among other things, a queue structure, queue requests, and queue arbitration. EX2015, 5-10. It shows different aspects of source code and various algorithms, dated March 15, 2010. *See* EX2015, 71-83. And, dated as early as February 1, 2010, it includes details about interrupts and doorbell registers used with the eNVMHCI Flash Drive Controller. *See* EX2015, 317-350. In addition to this evidence that indicates a possible earlier invention date, Polaris has reason to believe that the inventors and other third parties have more documentation, including product specifications, source code, commit logs, emails, and other product-development documentation that supports an earlier invention date and diligence towards a reduction to practice.

Antedating a reference requires substantial discovery that is ill suited for PTAB proceedings, and is not the best use of PTAB resources. In prior cases, patent owners have submitted various types of extrinsic evidence. They have submitted inventor declarations. *E.g.*, *ATI Techs. ULC v. Iancu*, 920 F.3d 1362, 1370 (Fed. Cir. 2019); *Nintendo America Inc. v. iLife Techs., Inc.*, 717 F. App'x 996, 1000-03 (Fed. Cir. 2017) (non-precedential); *Medtronic, Inc. v. Teleflex Innovations S.A.R.L.*, IPR2020-00135, Paper 128 at 17-71 (P.T.A.B. June 17, 2021); *CallMiner, Inc. v. Mattersight Corp.*, IPR2020-00220, Paper 59 at 60-84 (P.T.A.B. June 16, 2021); *Arkema France v. Honeywell Int'l, Inc.*, IPR2015-

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00915, Paper 56 at 12, 21, 30 (P.T.A.B. Oct. 20, 2016); *Sequenom, Inc. v. Board of Trustees of the Leland Stanford Junior University*, IPR2013-00390, Paper 45 at 5-15 (P.T.A.B. Nov. 25, 2014). They have produced source code and thousands of pages of commit logs. *E.g.*, *ATI Techs.*, 920 F.3d at 1370-71; *CallMiner*, IPR2020-00220, Paper 59 at 60-84. Expert witnesses were used to map technical documents, products, and/or source code to the patent claims. *E.g.*, *ATI Techs.*, 920 F.3d at 1371-72; *Medtronic*, IPR2020-00135, Paper 128 at 17-71; *CallMiner*, IPR2020-00220, Paper 59 at 60-84; *Arkema*, IPR2015-00915, Paper 56 at 13, 21, 30. Patent owners have also used declarations from additional fact witnesses to corroborate inventor testimony and authenticate documents. *E.g.*, *ATI Techs.*, 920 F.3d at 1371; *Nintendo*, 717 F. App'x at 1000-03; *Medtronic*, IPR2020-00135, Paper 128 at 17-71; *CallMiner*, IPR2020-00220, Paper 59 at 60-84; *Arkema*, IPR2015-00915, Paper 56 at 12, 21, 30; *Dynamic Drinkware LLC v. Nat'l Graphics, Inc.*, IPR2013-00131, Paper 42 at 8-9 (P.T.A.B. Sept. 12, 2014). Although the Board has procedures for parties to produce evidence, “discovery is limited” and “significantly different from the scope of discovery generally available under the Federal Rules of Civil Procedure.” *Garmin Int'l, Inc. v. Cuozzo Speed Techs. LLC*, IPR2012-00001, Paper 26 at 5 (P.T.A.B. Mar. 5, 2013) (precedential).

Given the scope of discovery likely needed to antedate Borchers, the district court would be better positioned to adjudicate this dispute. Federal district courts

have broad third-party subpoena powers to require third parties to “attend and testify; produce designated documents, electronically stored information, or tangible things in that person’s possession, custody, or control; or permit the inspection of premises.” FRCP, Rule 45. In contrast, the Board does not have the power to issue third-party subpoenas. Instead, the Board needs a district court to issue a subpoena. *See* 35 U.S.C. § 24. And even that power appears limited to testimony. *See id.* Here, the named inventors of the ’968 patent are not employees of Polaris, and other third parties likely have information needed to show conception, diligence, and/or reduction to practice. To ensure that all the evidence is in the record for the fact finder, the district court is better suited to adjudicate the discovery issues that will be associated with determining whether Borchers even qualifies as prior art.

Instituting trial in an IPR could also cause duplicative and/or unnecessary work related to discovery of confidential information required to antedate Borchers—especially third-party confidential information and source code. For example, the parties already negotiated terms for, and the district court has entered, a protective order. EX2010. That protective order is limited to the district court case and includes specific terms for source code, engineering and development documents, and other confidential business information. *Id.* In contrast, the default protective order in an IPR is far more limited and does not address additional

protections for the type of evidence that would need to get produced for antedating Borchers. *See* PTAB Consolidated Trial Practice Guide at 117-21 (Nov. 2019).

The parties would therefore need to re-negotiate terms for disclosure of confidential information in the IPR. If any required confidential information produced in the district court case is needed in the IPR (or vice versa), additional, non-substantive discovery-related efforts would be necessary to use the information in the other forum. *See* EX2010 at ¶7 (not permitting disclosure of confidential information to the PTAB); PTAB Consolidated Trial Practice Guide at 117-18 (Nov. 2019) (not permitting disclosure of confidential information to the district court).

The Board may also have to weigh in on disputes, which would expend Board resources that could otherwise be dedicated to other matters, such as *ex parte* appeals. This work can and should be avoided by denying institution and leaving the case to the district court, which already entered a protective order and a discovery schedule.

2. Instituting an IPR would not reduce the number of issues for the judge and jury to decide in the district court case.

The Board should also deny institution because the Petitioners have not explained how instituting an IPR would reduce the number of issues adjudicated by the district court judge and decided by a jury. For example, Petitioners have not represented or indicated that they would present fewer references or grounds to the

jury if an IPR is instituted. Instead, Western Digital's extensive 3,000-page invalidity contentions show the opposite—that it will present as many grounds and references to the jury as the court allows. In the invalidity contentions, Western Digital charted sixteen references for the '968 patent. EX2008, *53-54. It also served a list of approximately **300** different “References and Exemplary Combinations of References” for the '968 patent that it reserves the right to present to the jury. EX2008 (Appendix C).

Western Digital also cited product art from numerous companies. EX2008, *54-56. Even if the four references in the petition were removed from the candidate pool (EX1005, EX1006, EX1007, EX1008), Western Digital would still have many references to combine with product art. *See* 35 U.S.C. § 315(e) (estoppels do not apply to product prior art). Instituting an IPR would therefore not reduce the number of references or grounds but instead merely shift which references and grounds the defendants decide to present to the jury.

Instituting an IPR would also not resolve other invalidity theories such as Western Digital's arguments under 35 U.S.C. §§ 101 and 112. “Where the petitioner is relying on corresponding system art in a co-pending proceeding *and/or several other invalidity theories*, a stipulation may not be particularly meaningful because the efficiency gained by any AIA proceeding will be limited.” FAQs for Interim Process for PTAB Workload Management, FAQ14 (emphasis

added). Western Digital has raised, and is continuing to pursue, other invalidity theories under § 101 and § 112. EX2008, *64-71. Since these invalidity theories cannot be resolved in an IPR (35 U.S.C. § 311(b)), instituting an IPR would not resolve all the invalidity defenses at issue in the district court case and therefore not serve as a “true alternative” to the district court proceeding. *Motorola*, IPR2024-01205, Paper 19 at 3-4.

Instituting an IPR would also not reduce issues for claim construction. “Petitioner submits that, for the purposes of this [IPR] proceeding and the Grounds presented herein, *no claim term requires express construction*.” Pet., 17 (emphasis added). In contrast, the defendants in the district court have identified seven terms of the ’968 patent for construction. EX2024, *2-3. Since the grounds do not address any of the constructions the defendants intend to present in the district court, it is unclear how instituting an IPR would help the district court resolve these disputes. To the contrary, instituting an IPR may complicate claim construction issues because Petitioners appear to be taking inconsistent positions—plain and ordinary meaning for all terms in the IPR but more narrow constructions in the district court, including indefiniteness.

3. The expert declaration does not provide adequate, independent analysis that should accompany a petition.

When deciding whether to deny institution under § 314(a), the Board should also consider the substantial overlap between the petition and the expert

declaration. When the declaration “merely repeats, *verbatim*, the conclusory assertion for which it is offered to support” and “does not cite to any additional supporting evidence or provide any technical reasoning to support [the] statement,” the testimony is entitled to little weight. *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15 (P.T.A.B. Aug. 24, 2022) (precedential); *see also* 37 C.F.R. § 42.65(a) (“Expert testimony that does not disclose the underlying facts or data on which the opinion is based is entitled to little or no weight.”).

Petitioners submitted a declaration by Dr. Paul Min to support the arguments in the petition. But like the expert declaration in *Xerox*, Dr. Min’s declaration merely repeats, *verbatim*, conclusory assertions in the petition. He does not provide additional technical reasoning to support many of the substantive statements.

Some examples of Dr. Min’s repeating the petition (or vice versa) are provided below. Dr. Min repeats, *verbatim*, the arguments from the petition. He even uses the same italicized, bolded, and underlined styling and repeats legal conclusions with verbiage lifted straight from the petition. When Dr. Min’s declaration varies, it merely provides longer or additional block quotations that are cited in the petition.

Petition	Dr. Min Declaration
The PCI Standards represent the background knowledge of a POSITA	The PCIe Standard represents the background knowledge of a POSITA

because their subject matter is critical for designing memory systems that are compliant with industry standards. Given that the PCIe standard is “an enhancement to the PCI architecture” which was “the most widely accepted and implemented expansion standard in the world” as of 2004 (Ex.1007, 21; Ex.1006, 15), POSITAs in the field of memory systems would have been familiar with their teachings and would have sought to design their memory systems in accordance with such standards. Ex.1003, ¶77. Pet., 25.	because its subject matter is critical for designing memory systems that are compliant with industry standards. Given that the PCIe standard is “an enhancement to the PCI architecture” which was “the most widely accepted and implemented expansion standard in the world” as of 2004 (PCIe, 21; PCI, 15), POSITAs in the field of memory systems would have been familiar with its teachings and would have sought to design their memory systems in accordance with such standards. Min Declaration, ¶77.
The language that comes after the phrase “<i>A nonvolatile memory controller for ...</i>” of the preamble [1.0] describes a purpose, or intended use, of the controller. To the extent that the preamble is deemed limiting, Borchers teaches the entire preamble. Pet., 26.	The language that comes after the phrase “<i>A nonvolatile memory controller for ...</i>” of the preamble [1.0] describes a purpose, or intended use, of the controller. To the extent that the preamble is deemed limiting, Borchers teaches the entire preamble Min Declaration, ¶78.
First, Borchers’s memory controller board 102 includes an interrupt processor 124 (“<i>interrupt manager</i>”). “The controller board 102 may include a controller 110.” Ex.1005, [0019]. “The controller 110 may include a command processor 122 and <u>an interrupt processor 124.</u>” Ex.1005, [0019]. Pet., 31.	First, Borchers’s memory controller board 102 includes an interrupt processor 124 (“<i>interrupt manager</i>”). <u>The controller board 102 may include a controller 110,</u> a DRAM 111, multiple channels 112, a power module 114, and a memory module 116. <u>The controller 110 may include</u> a command processor 122 and <u>an interrupt processor 124,</u> as

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	well as other components, which are not shown. The memory boards 104 a and 104 b may include multiple flash memory chips 118 a and 118 b on each of the memory boards. The memory boards 104 a and 104 b also may include a memory device 120 a and 120 b, respectively. Borchers, [0019]. Min Declaration, ¶88.
First, Borchers' interrupt processor generates an “<i>interrupt vector state</i>” by maintaining a set of conditions that determine whether to send an interrupt signal. These set of conditions are maintained by various interrupt mechanisms including “a ResponseNew counter 280, a last response timer 282, group counters 284 and interrupt send logic 286.” Ex.1005, [0059]. Pet., 34-35.	First, Borchers' interrupt processor generates an “<i>interrupt vector state</i>” by maintaining a set of conditions that determine whether to send an interrupt signal. These set of conditions are maintained by various interrupt mechanisms including a ResponseNew counter 280, a last response timer 282, and group counters 284. Referring to FIG. 2, a block diagram of an exemplary interrupt processor 124 is illustrated. <u>The interrupt processor 124 may be configured to generate and send interrupts based on the interrupts mechanism</u> or mechanisms enabled by the host 106. <u>The interrupt processor 124 may include a ResponseNew counter 280, a last response timer 282, group counters 284 and interrupt</u>

	<u>send logic 286.</u> Borchers, [0059]. Min Declaration, ¶95.
Accordingly, because the interrupt mechanisms (e.g., timers and counters) (“<i>interrupt vector state</i>”) receive information (“<i>completion queue state</i>”) as to the status of the response queue (“<i>completion queue</i>”), Borchers’ interrupt mechanisms are generated “<i>based on</i>” that information. The interrupt mechanism information is <i>generated</i> when the timers or counters are updated. In some examples, the values of the timers or counters may be stored in a register. Indeed, a POSITA would have found it obvious for Borchers’ interrupt mechanism information to be stored in some type of memory such as a buffer, register, flag, or other form of storage. Ex.1003, ¶105. In other words, a POSITA would have recognized that the timers and counters of the interrupt mechanisms (“<i>interrupt vector state</i>”) are not merely transitory signals. Indeed, it was known for memory controllers and interrupt managers to use such registers or caches for storage. See <i>e.g.</i>, Ex.1008, Figs. 2 & 5, [0057], [0090]-[0091]; Ex.1009, Figs. 2 & 5, [0051], [0083], [0084]] (describing how an interrupt manager uses various forms of memory such as cache or registers to store state information). Accordingly, because Borchers’ interrupt processor receives and uses the response queue	Accordingly, because the interrupt mechanisms (“<i>interrupt vector state</i>”) receive information (“<i>completion queue state</i>”) as to the status of the response queue (“<i>completion queue</i>”), Borchers’ interrupt mechanisms are generated “<i>based on</i>” that information. The interrupt mechanism information is <i>generated</i> when the timers or counters are updated. In some examples, the values of the timers or counters may be stored in a register. Indeed, a POSITA would have found it obvious for Borchers’ interrupt mechanism information to be stored in some type of memory such as a buffer, register, flag, or other form of storage. In other words, a POSITA would have recognized that the timers and counters of the interrupt mechanisms (“<i>interrupt vector state</i>”) are not merely transitory signals. Indeed, it was known for memory controllers and interrupt managers to use such registers or caches for storage. See <i>e.g.</i>, Serebrin, Figs. 2 & 5, [0057], [0090]-[0091]; Serebrin Provisional, Figs. 2 & 5, [0051], [0083], [0084]] (describing how an interrupt manager uses various forms of memory such as cache or registers to store state information). Accordingly, because Borchers’ interrupt processor receives and uses the response queue status information

status information to update the interrupt mechanism timers and counters, Borchers' interrupt processor " <i>generate[s]</i> " an " <i>interrupt vector state</i> " as claimed. Pet., 39-40.	to update the interrupt mechanism timers and counters, Borchers' interrupt processor " <i>generate[s]</i> " an " <i>interrupt vector state</i> " as claimed. Min Declaration, ¶105.
Ground 1 shows how Borchers renders obvious each of the challenged claim limitations. Ground 1 further relies on the PCIe/PCI standards as evidence of the background knowledge of a POSITA. To the extent Patent Owner argues that the PCIe/PCI standards would not have been within the background knowledge of a POSITA, Ground 2 is presented to show that combining the teachings of the PCIe/PCI standards with Borchers would have been obvious to a POSITA. Ex.1003, ¶200. Pet., 76-77.	Ground 1 shows how Borchers renders obvious each of the challenged claim limitations. Ground 1 further relies on the PCIe/PCI standards as evidence of the background knowledge of a POSITA. To the extent Patent Owner argues that the PCIe/PCI standards would not have been within the background knowledge of a POSITA, Ground 2 is presented to show that combining the teachings of the PCIe/PCI standards with Borchers would have been obvious to a POSITA. Min Declaration, ¶200.
The claim analysis for Ground 2 is substantially the same as that of Ground 1. <i>See supra</i> X.C; Ex.1003, ¶214. Pet., 80.	The claim analysis for Ground 2 is substantially the same as that of Ground 1. <i>See supra</i> VIII.A. Min Declaration, ¶214.

Interestingly, Dr. Min's declaration follows the same formatting and verbiage as a declaration from a different expert (Dr. Lara Dolecek), which was filed by the same law firm. *SanDisk Technologies, Inc. et al. v. Polaris PowerLED Techs., LLC*, IPR2025-00515, Exhibit 1003 (P.T.A.B. Jan. 29, 2025).

Petitioners have also not established that Dr. Min has the requisite expertise specific to the memory controller interrupt techniques and PCI standards at issue in this IPR. Dr. Min's declaration explains that he has a background in electrical engineering (§§8, 13), has developed semiconductor devices and circuits (§9), and has expertise in networks and wireless cellular communications (§§10, 12, 17, 19, 20). One paragraph of the background section of his declaration refers to memory, but even this is silent with respect to the interrupt signaling at issue in this case:

Many of the integrated circuit chips I have developed incorporates high speed memory modules interacting with the memory controllers to perform various types of operations including pointer processing, pattern matching, tree-searching, and mathematical manipulation that require extremely fast read/write/bulk-transfer from/to the memory contents. For example, the latest generations of the switching fabric that I developed incorporated what is known in the switching field as the virtual output queue based on shared memory. In the switch fabric based on the virtual output queue based on shared memory architecture, there is no space-division switching, and rather, the switching is performed from the shared memory that takes in all of the incoming packets, which are manipulated by the pointers that organized the packets in the memory.

Min Declaration, §18.

Dr. Min also fails to provide any specifics about his background with the PCI standards. Dr. Min states that "I have personal experience using and referring

to the PCI standards throughout the 2000s” and that he “designed our systems to be compatible with the commonly used PCI standards.” Min Declaration, ¶205.

However, Dr. Min does not explain that he helped develop the standards. Nor does he identify which PCI-compatible products he developed or his role on those development teams. In fact, 144 individuals were instrumental in the development of the PCIe specification. EX1007, 631-32. Dr. Min was not one of them.

The lack of supporting evidence and additional technical reasoning from an expert who does not appear to have background experience specific to the interrupt signaling and PCI standards at issue in this case is yet another reason why the Board should deny institution. The standard for what qualifies as independent expert testimony and its use within IPRs should be higher; the declaration should not merely “cop[y], word-for-word, Petitioner’s conclusory assertions.” *Xerox*, IPR2022-00624, Paper 9 at 5. When it does, the Board should deny institution.

4. The ’968 patent issued over eleven years ago.

Under the interim process, the Director can consider “[s]ettled expectations of the parties, such as the length of time the claims have been in force” when deciding whether to exercise discretion to deny institution. Interim Processes for PTAB Workload Management at 2 (Mar. 26, 2025). Here, the ’968 patent issued on October 8, 2013—over eleven years ago. Had Petitioners objected to the issuance of the ’968 patent, they could have raised challenges over a decade ago.

35 U.S.C. §§ 302 (permitting any person at any time to file a request for reexamination), 321 (permitting post-grant review challenges up to 9-months after issuance). Western Digital could have also challenged the validity of the '968 patent after becoming aware of it at least as early as November 19, 2018. EX2018, 1 (Western Digital Technology identifying the '968 patent in an IDS on November 19, 2018); EX2017, (56) (citing the '968 patent).⁹ Instead, Petitioners waited many years to challenge the '968 patent—after Polaris relied on the issued claims in its complaint for patent infringement. This extended delay in challenging the claims also favors denying institution.

5. PTAB resources are better spent on *ex parte* appeals.

The Board should also deny institution because its limited resources are better spent on the growing backlog of *ex parte* appeals. In 35 U.S.C. § 6(b)(1), the Board is tasked with “review[ing] adverse decisions of examiners upon applications for patent pursuant to section 134(a).” Congress also tasked the Board with reviewing appeals of reexaminations, derivation proceedings, IPRs, and PGRs. 35 U.S.C. § 6(b)(2)-(4). But current Office policy is to focus on *ex parte*

⁹ The '968 patent was also cited during the prosecution of other Western Digital Technology patents, including at least U.S. Patent Nos. 10,452,278; 10,466,903; 10,509,569; 10,719,267; and 10,725,835.

appeals: “To ensure that the PTAB continues to meet its statutory obligations as to *ex parte* appeals, while continuing to maintain its capacity to conduct AIA proceedings, the Director will exercise her discretion on institution of AIA proceedings” Interim Processes for PTAB Workload Management at 1 (Mar. 26, 2025). The Board should exercise that discretion here because the pendency of *ex parte* appeals has increased (EX2012, 7), nearly a quarter of *ex parte* appeals have been pending more than eleven months (EX2013), and the backlog is growing month-over-month in almost all technology centers (EX2012, 4).

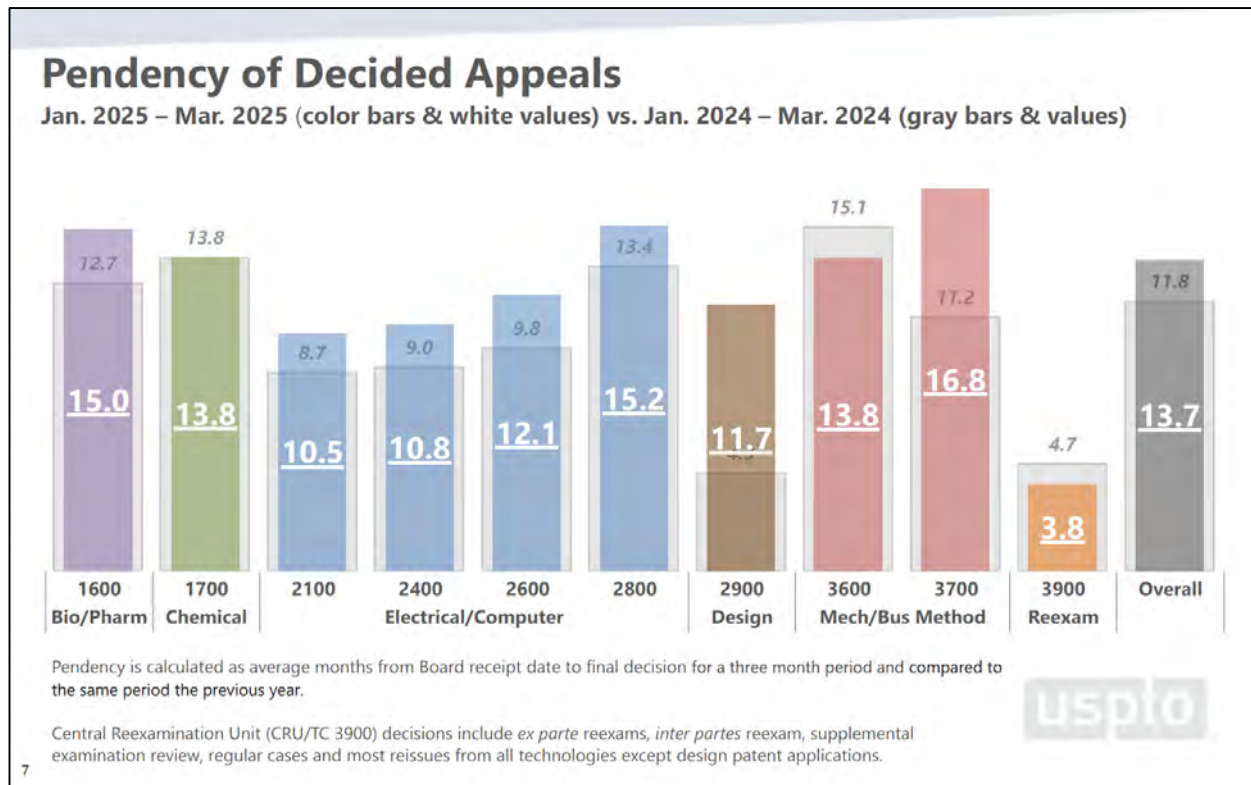
According to the latest data published by the USPTO, roughly a quarter of all *ex parte* appeals have been pending for over eleven months. EX2013.¹⁰ In 2025, the pendency has increased in almost every technical center. Shown below, the time (in months) to a final decision has increased in 2025 (shown with the color bars and white values) compared to the same data from 2024 (shown with the gray bars and gray values). For the technology center of the ’968 patent—2100¹¹—the

¹⁰ The latest data on the PTAB Dashboard is from November 2023.

However, the data from FY24 and FY25 also indicates that a substantial number of cases have been pending for over eleven months.

¹¹ The ’968 patent describes an interrupt technique for a nonvolatile memory controller. Patents for “Memory Access and Control” are under 2130, within tech

pendency has increased from 8.7 months to 10.5 months, a 20.7% increase.



EX2012, 7.

In the current fiscal year (FY25), the PTAB's backlog of *ex parte* appeals in the 2100 technology center has also increased. Shown below, in FY25, the PTAB's starting inventory of *ex parte* appeals in the technology center 2100 was 367 cases.

EX2012, 4. In FY25 (October 2024 through March 2025), 225 appeals have been filed, whereas the PTAB decided 181 appeals. *Id.* This has increased the backlog for technology center 2100 by 12% (44 cases)—the highest increase in number of

center 2100 (Computer Architecture Software and Information Security).

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cases outstanding for any technology center during FY25. *See id.*

Receipts & Dispositions (Fiscal Year through Mar. 31, 2025)												
Technology Center	Starting Inventory	Appeals Filed	Affirmed	Affirmed-in-Part	Reversed	Panel Remand	Admin Remand	Dismissed	Appeals Decided	Ending Inventory	Inventory Change	% of Inventory
1600	442	191	125	8	66	0	0	7	206	427	▼ -15	9.3%
1700	843	330	210	28	102	0	0	4	344	829	▼ -14	18.1%
2100	367	225	108	22	46	0	3	2	181	411	▲ 44	9.0%
2400	323	164	90	20	47	0	0	0	157	330	▲ 7	7.2%
2600	257	135	69	7	19	0	0	0	95	297	▲ 40	6.5%
2800	346	149	71	14	56	0	0	0	141	354	▲ 8	7.7%
2900	28	5	16	0	4	0	0	0	20	13	▼ -15	0.3%
3600	1,072	384	417	22	89	0	1	1	530	926	▼ -146	20.2%
3700	951	356	183	51	88	0	1	2	325	982	▲ 31	21.4%
3900 (Ex Parte)	12	23	13	0	4	0	1	0	18	17	▲ 5	0.4%
3900 (Sup. Exam)	0	0	0	0	0	0	0	0	0	0	▲ 0	0.0%
3900 (Reissue)	7	12	10	0	5	0	0	0	15	4	▼ -3	0.1%
3900 (Regular)	2	0	0	0	0	0	0	0	0	2	▲ 0	0.0%
Board Total	4,650	1,974	1,312	172	526	0	6	16	2,032	4,592	▼ -58	100.0%

% Decisions					
Affirmed	Affirmed-in-Part	Reversed	Panel Remand	Admin Remand	Dismissed
64.6%	8.5%	25.9%	0.0%	0.3%	0.8%

EX2012, 4 (annotated).

To reduce the average time to final decision, the 411 currently pending *ex parte* appeals in technology center 2100, the 12% backlog growth in the 2100 technology center during FY25, and the 4,592 currently outstanding *ex parte* appeals overall, the PTAB should focus its efforts on the pending *ex parte* appeals—not this IPR, especially since the district court is already scheduled to adjudicate validity months *before* the Board reaches its final decision.

In total, the other considerations also favor discretionary denial.

III. THE BOARD SHOULD DENY INSTITUTION UNDER § 325(D).

The Board should also deny institution under 35 U.S.C. § 325(d) because the

grounds rely on the same or substantially the same art previously presented to the Office, and Petitioners have not established that the Office erred in a manner material to the patentability of the challenged claims.

A. Legal Framework

The Board may deny institution if the grounds in the petition are based on the same or substantially the same art or arguments previously presented to the Office. 35 U.S.C. § 325(d). “Previously presented art includes art made of record by the Examiner, and art provided to the Office by an applicant, such as on an Information Disclosure Statement (IDS), in the prosecution history of the challenged patent.” *Advanced Bionics, LLC v. Med-El Elektromedizinische Geräte GMBH*, IPR2019-01469, Paper 6 at 7-8 (P.T.A.B. Feb. 13, 2020) (precedential).

When deciding whether to deny institution under § 325(d), the Board uses a two-part framework: “(1) whether the same or substantially the same art previously was presented to the Office or whether the same or substantially the same arguments previously were presented to the Office; and (2) if either condition of first part of the framework is satisfied, whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics*, IPR2019-01469, Paper 6 at 8. Under the first part of the framework, the Office considers the following factors: the similarities and material differences between the asserted art and the prior art involved during examination;

the cumulative nature of the asserted art and the prior art evaluated during examination; and the extent of the overlap between the arguments made during examination and the manner in which petitioner relies on the prior art. *Advanced Bionics*, IPR2019-01469, Paper 6 at 9-10 (citing *Becton, Dickinson & Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper 8 at 17-18 (P.T.A.B. Dec. 15, 2017) (precedential)).

When the first part of the *Advanced Bionics* framework is satisfied, the Board determines whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims. *Advanced Bionics*, IPR2019-01469, Paper 6 at 8. The following factors relate to whether a petitioner has demonstrated a material error: the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; whether petitioner has pointed out sufficiently how the examiner erred in its evaluation of the asserted prior art; and the extent to which additional evidence and facts presented in the petition warrant reconsideration of the prior art or arguments. *Advanced Bionics*, IPR2019-01469, Paper 6 at 9-10 (citing *Becton, Dickinson*, IPR2017-01586, Paper 8 at 17-18).

“At bottom, this framework reflects a commitment to defer to previous Office evaluations of the evidence of record unless material error is shown.” *Advanced Bionics*, IPR2019-01469, Paper 6 at 9.

B. The grounds in the petition rely on the same or substantially the same art considered during prosecution.

In this case, Petitioners rely on the same or substantially the same prior art that the examiner already considered during prosecution. Petitioners raise three grounds that rely on four references: (1) U.S. Patent Application Publication No. 2010/0262979 to Borchers *et al.*; (2) PCI Local Bus Specification Revision 3.0; (3) PCI Express 2.0 Based Specification Revision 0.9; and (4) U.S. Patent Application Publication No. 2011/0197003 to Serebrin *et al.* Pet., 18. Petitioners refer to references (2) and (3) collectively as the “PCI Standards.” *Id.*

Grounds	Claims	Basis
#1	1-18	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Borchers
#2	1-18	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Borchers and the PCI Standards
#3	1-18	Obvious under 35 U.S.C. § 103 (Pre-AIA) over Borchers, the PCI Standards, and Serebrin

Pet., 18.

Borchers—the primary reference in every ground—was already considered by the Office during prosecution. The applicant submitted Borchers in an IDS, which included only three references. EX1002, 107-10. A primary examiner then initialed the IDS entry for Borchers, indicating that he considered the reference. EX1002, 120.

When a primary reference was cited in an IDS and considered during prosecution, the Board has determined that the grounds rely on the same or substantially the same art previously presented to the office. *Google LLC v. Valtrus Innovations Ltd.*, IPR2022-01197, Paper 9 at 22 (P.T.A.B. Jan. 3, 2023); *Google LLC v. Valtrus Innovations Ltd.*, IPR2022-01197, Paper 18 at 28-29 (P.T.A.B. June 13, 2023). This should itself satisfy the first part of the *Advanced Bionics* framework. *Id.* However, the other references cited in the grounds are also the same or substantially the same art previously presented to the Office.

The PCI standards include substantially the same art previously presented to the Office. During prosecution, the examiner considered numerous revisions of the NVM Express (NVMe) specification. EX1002, 116, 157. The examiner first considered Revision 1.0b, but this version was dated July 12, 2011—after the ’968 patent’s priority date. *Id.* The examiner then asked the applicant to provide Revision 1.0, which was published earlier. *Id.* The applicant provided the examiner with Revision 1.0. EX1002, 129, 144. “After close review of the document,” the examiner determined that “it does not show the details of the steps performed by the memory controller as claimed.” EX1002, 157.

The relevant portions of the PCI standards that are cited in the petition are closely related and substantially similar to the NVMe specifications the Office considered during prosecution because NVMe was designed to operate over the

PCI Express (PCIe) bus and builds directly on top of the PCIe architecture.

EX2019, 8 (“This interface is optimized for Enterprise and Client solid state drives, typically attached to the PCI Express interface.”). In fact, the NVMe specification references PCI/PCIe over 150 times. *See* EX2019. The NVMe also leverages the same features of the PCIe standards that Petitioners rely on, including its register-level interface, interrupt mechanisms such as Message Signaled Interrupts (MSI/MSI-X), and doorbell registers. EX2019, 8-9 (“The interface has the following key attributes: . . . Support for MSI/MSI-X and interrupt aggregation” and “This specification defines a streamlined set of registers whose functionality includes: . . . Doorbell registers for scalable number of Submission and Completion Queues.”). Accordingly, when Petitioners cite to features of the PCI standards such as MSIs (Pet., 37, 42, 48, 77-79) or doorbell registers (Pet., 23, 44-45), the examiner already considered those features when examining NVMe. *See* EX2019, 8-9. The Office would have also considered the PCI/PCIe functionality when considering the other references in the prosecution history, which cite the PCI standards extensively. *E.g.*, EX1001, 1:15-25, 3:63-66, 10:1-3, 10:39-42, 16:61-67; EX1005, ¶¶110, 115; EX2020, 3:14-19, 5:48-58, 6:34-43, 9:45-49, 10:33-38; EX2021, 1:21-31, 3:43-52; EX2022, ¶¶12, 204; EX2023, ¶¶1, 24, 165, 169. The teachings that Petitioners rely on in the PCI standards are therefore cumulative to features in the NVMe specifications.

The only other reference is Serebrin, which is used in Ground 3. But Serebrin is cumulative to Borchers because, according to Petitioners, “Ground 3 is substantially the same as that of Ground 1,” which relies on the same Borchers reference that was overcome during prosecution. Pet., 87. Petitioners used Serebrin merely to show that an interrupt processor can use memory. See Pet., 34, 40, 56-57, 85-87. Yet the art considered during prosecution—including the NVMe specification—describes memory in the context of interrupt signaling. See, e.g., EX2019. Petitioners provided no reasons why Serebrin’s specific teachings about memory are somehow different and non-cumulative to the references considered during prosecution. See Pet., 89-91 (analysis under § 325(d) not mentioning Serebrin). To the contrary, Petitioners allege that Serebrin is “substantially the same” as Borchers. See Pet., 87.

Borchers is the same art considered previously, the PCI standards are substantially the same art, and the teachings in Serebrin are cumulative and insignificant. The first part of the *Advanced Bionics* framework is satisfied.

C. Petitioners have not established that the Office erred in a manner material to the patentability of the challenged claims.

When the first part of the *Advanced Bionics* framework is satisfied, the Board determines “whether the petitioner has demonstrated that the Office erred in a manner material to the patentability of challenged claims.” *Advanced Bionics*, IPR2019-01469, Paper 6 at 8. Petitioners have raised two arguments for why the

Office erred. Pet., 90-91. Both arguments fail.

First, the Petitioners alleged that “Borchers’ inclusion in an IDS does not show that Borchers was given serious evaluation by the Examiner.” Pet., 90. The Board has rejected this argument when, like here, the examiner indicates that it “considered” the reference. *Google*, IPR2022-01197, Paper 9 at 18-19. Even though the examiner did not discuss Borchers in detail, the examiner indicated that Borchers was “considered” in a signed IDS confirmation. EX1002, 120. Thus, Borchers appears on the face of the ’968 patent along with eleven other references. Because Borchers was “considered” by the examiner during prosecution, this weighs slightly in favor of exercising discretion to deny institution under § 325(d). *Google*, IPR2022-01197, Paper 9 at 19.

The *Navistar* case Petitioners cite (Pet., 90) does not state otherwise. In *Navistar*, the examiner cited two of the IPR references “in a list of ‘prior art made of record and *not* relied upon,’ and characterized this prior art as ‘pertinent to applicant’s disclosure.’” *Navistar, Inc. v. Fatigue Fracture Tech., LLC*, IPR2018-00853, Paper 13 at 17 (P.T.A.B. Sept. 12, 2018) (emphasis added). These references were also cited in earlier family members as “prior art made of record and *not* relied upon.” *Id.*, 17 n.5 (emphasis added). In other words, the Office expressly stated, on multiple occasions, that the references were *not* relied upon. *Id.* Whereas here, the examiner considered Borchers in an IDS with only three

references.

Second, Petitioners alleged that the examiner erred by overlooking Borchers' teachings in combination with evidence in the PCI standards about a doorbell register and Dr. Min's associated testimony, which parrots the petition *verbatim*. See Pet., 90-91. Petitioners cite a case where the Board did not deny institution in part because the petitioner raised a new secondary reference that disclosed a key claim element that was missing in the art considered during prosecution. *Puma N. Am., Inc. v. Nike, Inc.*, IPR2019-01058, Paper 10 at 12-16, 19 (P.T.A.B. Oct. 31, 2019). But unlike the *Puma* case, Petitioners have not identified a teaching that was missing from and non-cumulative of the references the examiner considered during prosecution. During prosecution, the examiner considered Borchers. See EX1002, 120. The examiner also considered the NVMe specification, which refers to doorbell registers and the associated signaling at least 50 times. EX1002, 157; EX2019. In contrast, the PCI standards (EX1006 and EX1007) collectively refer to a doorbell register in only a single paragraph. EX1006, 308. Petitioners have failed to explain how this limited disclosure about a doorbell register is somehow different and non-cumulative of the NVMe specification, which refers to doorbell registers in far more detail.

Even if Petitioners were to show that the PCI standards are non-cumulative to the NVMe specifications, failure to consider the PCI standards' alleged

teachings about “doorbell updates” would not have been an error “material to the patentability of challenged claims.” *Advanced Bionics*, IPR2019-01469, Paper 6 at 8. “An example of a material error may include misapprehending or overlooking specific teachings of the relevant prior art where those teachings impact patentability of the challenged claims.” *Id.* at 8 n.9. But here, the examiner’s patentability determination did not hinge on the “doorbell update” limitation because he allowed claims without it. EX1002, 116 (allowing now-issued claim 8, which does not recite a “doorbell update”). Since the “doorbell update” did not impact his patentability determination, any error for failing to consider the PCI standards’ teachings about an alleged “doorbell update” was immaterial.

Petitioners failed to demonstrate that the examiner misapprehended or overlooked specific teachings in the relevant prior art such that the error by the Office was material to the patentability of the challenged claims. Because both parts of the *Advanced Bionics* framework are met, the Board should exercise its discretion under § 325(d) to deny institution. *See Advanced Bionics*, IPR2019-01469, Paper 6 at 21.

IV. CONCLUSION

Litigating the same or similar issues at the Board as the issues that are already scheduled to get resolved in the district court would be duplicative and contrary to the intent of IPRs for “providing a more efficient system for challenging patents” and “reducing unwarranted litigation costs.” H.R. Rep. No. 112-98 at 39-40 (2011); *see also NHK Spring*, IPR2018-00752, Paper 8 at 19-20. Moreover, the Office has already evaluated the same or substantially the same art and arguments. Accordingly, the Board’s limited resources would be better spent elsewhere.

Respectfully submitted,

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Case IPR2025-00517
U.S. Patent No. 8,554,968

CERTIFICATE OF WORD COUNT (37 C.F.R. § 42.24(d))

1. This Patent Owner's Brief on Discretionary Denial complies with the type-volume limitation of 14,000 words, comprising 10,706 words, excluding the parts exempted by 37 C.F.R. § 42.24(a)(1).

2. This Patent Owner's Brief on Discretionary Denial complies with the general format requirements of 37 C.F.R. § 42.6(a) and has been prepared using Microsoft® Word 2016 in 14-point Times New Roman font.

Respectfully submitted,

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Case IPR2025-00517
U.S. Patent No. 8,554,968

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

I certify that the above-captioned **PATENT OWNER'S BRIEF ON
DISCRETIONARY DENIAL** and associated Exhibits 2001-2024 were served in
their entireties on April 25, 2025, upon the following parties via electronic mail:

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND
WESTERN DIGITAL TECHNOLOGIES, INC.
Petitioner,

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner.

IPR2025-00517
U.S. Patent No. 8,554,968

**PETITIONER'S OPPOSITION TO PATENT OWNER'S
REQUEST FOR DISCRETIONARY DENIAL**

Opposition to Patent Owner's Request for Discretionary Denial
IPR2025-00517 (U.S. Patent 8,554,968)

I. Introduction

Petitioner respectfully requests that the Director decline to exercise her discretion to deny institution and advance the Petition to a merits panel for consideration.

Petitioners Western Digital Technologies, Inc. and Sandisk Technologies Inc. (together “Petitioner”) oppose Patent Owner’s Request for Discretionary Denial (Paper 9, “PO Brief”) The *Fintiv* factors and the additional factors set forth in the Acting Director’s “Interim Processes for PTAB Workload Management” (“Director Memo”), considered as a whole, do **not** warrant denial—the parallel litigation has been stayed at an early stage of the case pending the resolution of the Petition.

With respect to *Fintiv*, five of the six *Fintiv* factors strongly weigh against denial. Because the parallel litigation has been stayed and in view of Petitioner’s “*Sotera*” stipulation, this IPR is a “true alternative” to the parallel litigation.

The additional factors listed in the Director Memo similarly weigh against denial. Petitioner has a compelling interest in having access to cost-effective PTAB review when accused of infringement by entities that do not manufacture or innovate. Patent Owner (Polaris PowerLED) has no compelling interest or expectation sufficient to avoid PTAB review, because unlike the original owner of the '968 patent, Patent Owner is an assertion entity who appears to have acquired

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the patent three years ago solely for the purpose of litigation—which changes everything with respect to settled expectations. Further, the Petition does not rely on expert testimony for gap-filling any claim elements. Instead, all claim elements are shown in the printed publication prior art, and the petition relies upon expert testimony to the extent necessary under Federal Circuit precedent to show how a POSITA would read and understand these references.

This IPR is one of three IPRs challenging three patents asserted in the stayed parallel litigation. Ex.1032, 1. These three patents are from different families and address three distinct and well-established technologies associated with memory systems respectively: Error Correcting Coding (ECC), redundant array of independent disks (RAID), and interrupt handling. Therefore, they are better suited for PTAB review, where the Board's technical expertise is well-suited to assess the distinctions and technical details of the asserted claims and the prior art presented in the obviousness grounds. The District Court in the parallel litigation agrees, having stayed the litigation so that the PTAB can handle this accordingly.

II. Discretionary denial under *Fintiv* is not warranted.

The *Fintiv* factors, considered as a whole, do not warrant denial. *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 (Mar. 20, 2020) (precedential). Every factor either favors institution or is neutral.

A. Factor 1 weighs strongly against denial: A stay was granted.

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The parallel Litigation “is still in early stages of litigation” and has been stayed. Ex.1032, 4. The Court granted Petitioner's Motion to Stay Pending IPRs on June 24, 2025. *Id.*, 1. The stay remains in effect pending resolution of the IPR proceedings. With the parallel litigation stayed, this IPR is a true alternative to district court litigation. Thus, this factor strongly weighs against denial.

B. Factor 2 weighs strongly against denial: The parallel litigation was stayed.

While the scheduling originally indicated a trial date around the same time as the projected Final Written Decision (“FWD”), this previously scheduled trial date, together with other scheduled dates, was “**VACATED** and taken off the calendar.” Ex.1032, 9. No trial date is scheduled.

Accordingly, Factor 2 strongly weighs against denial in view of the stay in the parallel litigation.

C. Factor 3 weighs strongly against denial: Minimal relevant investment and diligent filing.

Factor 3 weighs strongly against discretionary denial because, at institution, investment by the court and parties will have been minimal as to the activities pertinent to *Fintiv*. Patent Owner's Request for Discretionary Denial includes a laundry list of activities allegedly showing substantial investment, but very few relate to invalidity of the '968 patent. *See* PO Brief, 7-9. Under *Fintiv*, “[i]f, at the time of the institution decision, the district court has not issued orders *related to*

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the patent at issue in the petition, this fact weighs against exercising discretion to deny institution.” *Fintiv*, 10. Not only is there no order, no claim construction briefing has been done. The Court confirmed that “the case is in its ***early*** stages and there is still more work ahead of the parties and the Court than behind them.” Ex.1032, 4 (citations omitted, emphasis added).

This factor also weighs against denial because the Petitioner worked diligently to file the instant petition after receiving Patent Owner's infringement contentions and diligently filed the now-granted motion for stay. *Fintiv*, 11. Petitioner received Plaintiff's infringement contentions on October 2, 2024 (Ex.1023), and worked diligently to file three IPR petitions, including the instant petition, ***within four months***. At the time of the filing, the parallel litigation was in its early stages and claim construction briefing had yet to begin. The Board has recently agreed that similar diligence is reasonable and weighs against denial. See *Samsung Elecs. Co., Ltd. v. Mullen Industries LLC*, IPR2024-01472, Paper 9 at 10 (Mar. 31, 2025) (“Petitioner's diligence in filing its Petition (a) less than five months after receiving Patent Owner's infringement contentions and (b) prior to the parties briefing claim construction issues weighs against exercising discretionary denial.”).

Accordingly, Factor 3 weighs strongly against denial.

D. Factor 4 weighs strongly against denial: Petitioner's “Sotera” stipulation.

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Factor 4 weighs strongly against discretionary denial. First, the Court, in staying the parallel litigation, explained the benefits of PTAB review, including simplification of issues and trial in the parallel litigation. The Court reasoned that there is “a likelihood that ‘the outcome of the [IPR] could eliminate the need for trial if the claims are cancelled or, if the claims survive, facilitate trial by providing the court with expert opinion of the [Patent and Trial Office] and clarifying the scope of the claims.’” Ex.1032, 6. And “[i]f the PTAB cancels or narrows a portion of the asserted claims, the scope of this litigation may be significantly reduced.” Ex.1032, 5 (citations omitted).

Second, Petitioner has made a *Sotera* stipulation in district court. *See* Ex.1019 (stipulation filed in parallel district court proceeding). Specifically, Petitioner stipulated that:

[I]f the PTAB institutes an IPR in response to Defendant's petition against Plaintiff's U.S. Patent No. 8,554,968 (IPR2025-00517), Defendant will not pursue in this litigation against the claims challenged in IPR2025-00517, (i) the specific grounds raised in IPR2025-00517, or (ii) any other grounds that could have reasonably been raised before the PTAB in that instituted proceeding (i.e., any ground that could have reasonably been raised under §§ 102 or 103 on the basis of prior art patents or printed publications).

Ex.1019, 1-2.

Petitioner's *Sotera* stipulation was timely under the procedures in place

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when the petition was filed. At the time of filing on January 23, 2025, PTAB precedent provided that the “appropriate time for a petitioner to offer a stipulation related to the *Fintiv* factor 4 analysis is prior to the Board’s decision of whether to institute review.” *NXP USA, Inc. v. Impinj, Inc.*, IPR2021-01556, Paper 13 at 4 (Sept. 7, 2022) (de-designated precedential Apr. 25, 2025); *see also Nike, Inc. v. ADIDAS AG*, 955 F.3d 45, 52 (Fed. Cir. 2020) (“In interpreting the APA’s notice provisions in the context of IPR proceedings, we have cautioned that an agency may not change theories in midstream without giving respondents reasonable notice of the change and the opportunity to present argument under the new theory.”) (citation and quotation marks omitted).

Patent Owner argues that this stipulation is “too late” under the procedures defined in the FAQs. PO Brief, 13. The FAQs state: “A petitioner should file a *Sotera* or *Sand* stipulation as soon as practicable, so that a patent owner may address the impact of the stipulation in its discretionary denial brief.” Ex.1021, FAQ 14. Petitioner filed this *Sotera* stipulation as soon as practicable on April 28, 2025—three days after the FAQs were issued. In an apparent attempt to preclude consideration of a stipulation, Patent Owner filed their brief on April 25, 2025—almost one month before their due date of May 24, 2025. Had Patent Owner filed on their actual due date, Patent Owner would have had nearly one month to consider and brief the *Sotera* stipulation—provided there is anything to be said.

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Patent Owner's early filing should not preclude consideration of Petitioner's

Sotera stipulation. And Patent Owner had ample opportunity to brief the expected *Sotera* stipulation in their discretionary denial brief or any supplemental briefing they could have asked for.

Petitioner respectfully submits that this stipulation outweighs all other *Fintiv* factors as it eliminates overlap with invalidity issues raised in the parallel proceeding. Petitioner's stipulation is consistent with the scope of estoppel under 35 U.S.C. § 315(e)(2). *See Ingenico Inc. v. IOENGINE, LLC*, No. 2023-1367, 2025 WL 1318188, at *8 (Fed. Cir. May 7, 2025) ("IPR estoppel did not preclude Ingenico from relying on the DiskOnKey System with related printed publications at trial...").

This case is distinguishable from the *Motorola Solutions* case cited by Patent Owner. PO Brief, 14. In *Motorola Solutions*, the Director found that the *Sotera* stipulation did not outweigh the substantial investment in the district court proceeding, where "the parties had served extensive infringement and invalidity contentions, served opening and rebuttal expert reports, filed claim construction briefs, and conducted several deposition," and the "court also had held a claim construction hearing and construed the disputed claim terms," before the litigation was stayed after institution. *See Motorola Solutions, Inc. v. Stellar, LLC*, IPR2024-01205, Paper 19 at 3-4 (P.T.A.B. Mar. 28, 2025). In contrast and as noted by the

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judge, "[t]his case is still in early stages of litigation." Ex.1032, 4. Accordingly, Petitioner's *Sotera* stipulation weighs strongly against denial.

Also weighing against denial under Factor 4 is that Petitioner's challenge encompasses claims 4-5 and 12-13, which are not at issue in the litigation. And only the asserted claims are the subject of Petitioner's invalidity contentions on the parallel litigation. See Ex.2008, 1 (asserting invalidity "***only to the asserted claims identified by Polaris in its Infringement Contentions.***"). Petitioner elected to challenge additional, unasserted claims for efficiency reasons—for example, to avoid filing a second IPR in the event Patent Owner asserts additional claims in the parallel litigation.

These additional challenged (but unasserted) claims differ in claim scope from the asserted claims, meaning that key issues in the petition will not be resolved by the district court—further reducing the degree of overlap under Factor 4. See *Fintiv*, 13 (examining whether the district court will "resolve key issues in the petition").

Petitioner's *Sotera* stipulation also moots Patent Owner's argument that "Petitioners appear to have strategically omitted the defendant Western Digital Corporation—the parent corporation of Western Digital Technologies, Inc.—from the petition to evade estoppels." PO Brief, 15. Western Digital Corporation has explicitly agreed to be bound by Petitioner's *Sotera* stipulation. Ex.1019, 1.

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Additionally, Western Digital Corporation has explicitly “agree[d] to be bound by the estoppel effect of the IPRs” in its Reply for Motion to Stay. Ex.2011, 2 (“Western Digital Corporation agrees to be bound by statutory estoppel ***to the same extent as Western Digital Technologies***”). Western Digital Corporation’s agreement to be bound by estoppel effect of the IPR is not conditioned upon the stay being granted. Western Digital Corporation is thus not “evad[ing] estoppel” as Patent Owner argues. PO Brief, 15; Ex.1032, 6.

Accordingly, Factor 4 weighs strongly against denial because of (i) Petitioner’s *Sotera* stipulation and (ii) key issues in the Petition that will not be resolved by the district court.

E. Factor 5 is neutral: Petitioner is a defendant in the parallel litigation.

Petitioner Western Digital Technologies, Inc. is a defendant in the parallel litigation. That is true of most IPR petitioners, making this factor neutral. *See HP Inc. v. Slingshot Printing LLC*, IPR2020-01084, Paper 13 at 9 (Jan. 14, 2021); *see also NVIDIA Corp. v. Invensas Corp.*, IPR2020-00603, Paper 11 at 23 (Sept. 3, 2020) (this factor weighs against discretionary denial where the district court trial and IPR final written decision are expected “around the same time”).

F. Factor 6 weighs against denial: The merits of the Petition are particularly strong.

Factor 6 favors institution because the Petition plainly shows that the

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challenged claims of the '968 patent claims are unpatentable. In its PO Brief, Patent Owner does not raise any specific merits arguments other than stating that it will present merits arguments in its Patent Owner Preliminary Response (POPR). However, as discussed in detail below at III.A, Patent Owner's merits arguments in its POPR do not hold up under scrutiny. Thus the merits of the Petition are particularly strong, favoring institution.

G. The *Fintiv* factors as a whole weigh against denial.

In summary, each *Fintiv* factor is either neutral or weighs strongly against denial:

Factor	Weight	Reason
1 (stay)	against denial	a stay has been granted
2 (trial gap)	strongly against denial	A stay has been granted and thus there is no scheduled trial date
3 (investment)	against denial	Parallel litigation in early stages and no court orders regarding invalidity of the '968 patent
4 (overlap)	strongly against denial	<i>Sotera</i> stipulation; key issues not resolved by district court
5 (same party)	neutral	Petitioner is defendant
6 (merits)	strongly against denial	Strength of the patentability challenge is strong

In light of all the *Fintiv* factors as a whole, the Director should not discretionarily deny institution under §314(a).

III. The additional factors set forth in the Director Memo favor institution

The Director Memo invites the parties to “address all relevant [discretionary

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denial] considerations" and provides a list of potential factors. Director Memo, 2-3.

Each of the potential factors favors institution:

- The unpatentability challenges in the Petition are particularly strong given that the prior art shows the same interrupt coalescing techniques that are claimed.
- The Petition relies upon expert testimony to the extent necessary under Federal Circuit precedent, and such expert testimony is supported by evidence as required under 37 CFR § 42.65 and *Xerox*.
- Patent Owner cannot reasonably allege settled expectations regarding the '968 patent based on a few years of ownership and the lack of any post-issuance validity challenge.
- Neither the PTAB nor another forum has adjudicated the validity of the '968 patent.
- Patent Owner does not allege that any changes in the law or new judicial precedent issued since issuance of the claims affects patentability.
- The United States has a compelling economic and national security interest in ensuring Sandisk and Western Digital, leading domestic technology innovators, have access to efficient AIA proceedings when faced with meritless lawsuits by non-practicing entities.

Several of these factors are of particular importance to the Director's discretion and are addressed individually below.

- A. **The merits of the Petition are particularly strong because the prior art teaches the same interrupt coalescing technique that is claimed.**

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The '968 patent should not have issued because it claims no more than well-known concepts related to the interrupt coalescing techniques that are described and claimed in the '968 patent. The '968 patent is thus one of the patents Congress referred to when discussing the purpose of the America Invents Act—"improving patent quality and providing **a more efficient system for challenging patents that should not have issued.**" House Report (H.R. Rep. 112-98, 2011), 39-40.

As stated in the Petition, the purported novelty of the '968 patent is to delay sending the interrupt signal until certain conditions (e.g., by a timer or response counter) are met. *See* Ex.1001, 1:38-2:41. But this technique—referred to as interrupt coalescing—was already known as of the filing date of the '968 patent. *See generally*, Ex.1005. The Borchers reference, describes using a "ResponseNew Counter 280" and a "LastResponse Timer 282" to determine when to send an interrupt signal to the host. Ex.1005, Fig. 2. As shown in the petition, and supported by the declaration of Dr. Paul Min (Ex.1003), Borchers renders obvious the Challenged Claims of the '968 patent.

Patent Owner's merits-based arguments do not hold up under scrutiny and thus the merits of the case remain strong, favoring institution. Patent Owner argues that the director should consider their POPR arguments "when determining whether to exercise its discretion to deny institution." PO Brief, 6. But the POPR does not refute the analysis in the Petition.

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For example, Patent Owner alleges distinctions where there are none. Patent Owner states that “Borchers’ interrupt processor 124 does not ‘alert the host processing unit of the unprocessed completion status in the completion queue.’” But the Petition explained how Borchers’ “interrupt processor 124 is configured to **signal** the **host 106** with an interrupt when new responses are available in the response buffer 123 [“*completion queue*].” Ex.1005, [0035].

Because Patent Owner has not effectively disputed the Petition’s analysis, the strength of the patentability challenge remains strong. Petitioner respectfully requests that the Director pass this case to a merits panel and requests that the Board institute trial.

B. The Petition properly relies on expert testimony

The Petition’s compliance with Federal Circuit precedent should not be a reason for discretionary denial. And Dr. Min’s opinions are fully supported by the evidence of record.

1. Federal Circuit precedent requires that the Petition rely on expert testimony.

Petitioner’s reliance on expert testimony as required by Federal Circuit precedent should not be a reason for discretionary denial. The foundational decisions upon which patent law is based—*Phillips*, *KSR*, etc.—require the adjudicator to evaluate the patent and prior art from perspective of a POSITA. That perspective is established with evidence, often in the form of expert declarations.

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Attorney argument is insufficient.

It is well established that patent claims are construed based on the understanding of a POSITA. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (“We have made clear, moreover, that the ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application.”) (citing *Innova/Pure Water, Inc. v. Safari Water Filtration Systems, Inc.*, 381 F.3d 1111, 1116 (Fed. Cir. 2004) (“A court construing a patent claim seeks to accord a claim the meaning it would have to a person of ordinary skill in the art at the time of the invention.”)); *Home Diagnostics, Inc. v. LifeScan, Inc.*, 381 F.3d 1352, 1358 (Fed. Cir. 2004) (“customary meaning” refers to the “customary meaning in [the] art field”); *Ferguson Beauregard/Logic Controls v. Mega Sys., LLC*, 350 F.3d 1327, 1338 (Fed. Cir. 2003) (claim terms “are examined through the viewing glass of a person skilled in the art”); see also *PC Connector Solutions LLC v. SmartDisk Corp.*, 406 F.3d 1359, 1363 (Fed. Cir. 2005) (meaning of claim “must be interpreted as of [the] effective filing date” of the patent application); *Schering Corp. v. Amgen Inc.*, 222 F.3d 1347, 1353 (Fed. Cir. 2000) (same)).

Obviousness grounds are likewise evaluated from the perspective of a POSITA. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 401 (2007) (“If a person of

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ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.”), 418 (“[I]t can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does.”), 421 (“A person of ordinary skill is also a person of ordinary creativity, not an automaton.”).

The Federal Circuit has also made it clear that attorney argument alone is not evidence and should be given little weight. *Icon Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1043 (Fed. Cir. 2017) (“Attorney argument is not evidence.”) (citing *Gemtron Corp. v. Saint-Gobain Corp.*, 572 F.3d 1371, 1380 (Fed. Cir. 2009) (“[U]nsworn attorney argument . . . is not evidence and cannot rebut . . . other admitted evidence . . .”)); see also *Elbit Sys. Of Am., LLC, v. Thales Visionix, Inc.*, 881 F.3d 1354, 1359 (Fed. Cir. 2018) (“Elbit fails to present any evidence supporting this contention beyond attorney argument . . . and ‘[a]ttorney argument is not evidence’ and cannot rebut other admitted evidence.”).

Because attorney argument is not evidence, expert testimony is *necessary* to properly support a petition's claim construction and obviousness positions, which

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are evaluated from the perspective of a POSITA. This is precisely how the Petition presents and uses the testimony of Dr. Min. *See generally* Petition, (relying on testimony of Dr. Min to support obviousness grounds). The unpatentability grounds set forth in the Petition are fully supported by the references themselves—Dr. Min's testimony serves to confirm, support, and explain the disclosures of the references from the perspective of a POSITA. *See generally* Ex.1003.

Importantly, Dr. Min was a POSITA as of the critical date of the '968 patent. Ex.1003, ¶¶7-23. Dr. Min defines a POSITA as someone "knowledgeable and familiar with memory systems." Ex.1003, ¶22. Dr. Min has such experience, as he "implemented a number of semiconductor integrated circuit chips" including "switch fabrics, processors, high speed interfaces, protocol transposers, controllers, content search engine, pattern matching, and memory cells and arrays." Ex.1003, ¶18.

Patent Owner nevertheless questions that Dr. Min "has the requisite expertise specific to the memory controller interrupt techniques and PCI standards at issue in this IPR." PO Brief, 32. Patent Owner then states that "Dr. Min does not explain that he helped develop the standards. Nor does he identify which PCI-compatible products he developed or his role on those development teams." PO Brief, 33. But Dr. Min need not have contributed to developing the PCI standards in order to be considered a POSITA. And in any event, disputes over the definition

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of a POSITA should not be a reason for discretionary denial.

Further, Dr. Min's testimony is supported by corroborating evidence in the form of the disclosure of the references relied upon in the unpatentability grounds (e.g., Ex.1005, Ex.1006, Ex.1007, Ex.1008) and several tertiary references (e.g., Ex.1009, Ex.1011, Ex.1012, Ex.1013, Ex.1014). *See generally*, Ex.1003. Further still, Dr. Min repeatedly provides technical reasoning to support his statements and understandings of the references. *See generally*, Ex.1003.

Further, the Federal Circuit has recognized that "when the technology is complex and 'beyond the comprehension of laypersons,' expert testimony is 'sometimes essential.'" *Synopsys, Inc. v. Mentor Graphics Corp.*, 814 F.3d 1309, 1320 (Fed. Cir. 2016) (internal quotations removed); *see also Perfect Web Techs., Inc. v. InfoUSA, Inc.*, 587 F.3d 1324, 1330 (Fed. Cir. 2009) ("If the relevant technology were complex, the court might require expert opinions."). This is precisely the situation here. Dr. Min's expertise is utilized to explain the technical background of complicated concepts relevant to the '968 patent (*see, e.g.*, Ex.1003, ¶¶28-41). Dr. Min also provides detailed explanations regarding how a POSITA would have understood the technical descriptions found in the '968 patent and the prior art references (*see, e.g.*, Ex.1003, ¶¶28-230). Dr. Min's testimony serves these essential purposes and is a strength of the Petition.

2. Patent Owner's arguments based upon Xerox are misplaced.

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Patent Owner argues that “Dr. Min repeats, verbatim, the arguments from the petition.” PO Brief, 27 (citing *Xerox Corp. v. Bytemark, Inc.*, IPR2022-00624, Paper 9 at 15-17 (August 24, 2022) (precedential)). *Xerox*, however, does not stand for the proposition that a Petition and supporting declaration cannot be similar. *Xerox* instead focuses on whether the expert testimony cites to “supporting evidence or provide[s] any technical reasoning.” *Xerox*, 15. Expert testimony is only afforded less weight if it “adds little to the conclusory assertion for which it is offered to support.” *Id.* Here, Dr. Min’s analysis is fully supported by evidence, and does not rely on improper gap filling. Accordingly, the Petition’s proper reliance on expert testimony to support the unpatentability grounds favors institution.

C. Patent Owner’s purported intention to antedate Borchers is not a reason for discretionary denial.

Patent Owner believes that its purported plans to swear behind the Borchers reference make this case better suited for the district court, which has broader subpoena powers. See PO Brief, 19-23. But the district court’s subpoena powers are available to Patent Owner regardless of whether the Board institutes this proceeding. And it would be inappropriate to discretionarily deny this case based on Patent Owner’s “reason to believe” that sufficient documentation exists.

Patent Owner was first made aware of Petitioner’s reliance on the Borchers reference in the invalidity contentions filed December 16, 2024. Ex.1035, 52

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(Invalidity Contention Cover Pleading). Since then, Patent Owner has made no effort to antedate the Borchers reference. In fact, Patent Owner more recently represented to the district court, and Petitioners, that it does not have any “documents evidencing the conception, reduction to practice, design, and development of each claimed invention, which were created on or before the date of application for the patent in suit or the priority date.” Ex.1023, 3 (Patent Owner's infringement contention cover pleading).

Patent Owner nevertheless asserts in its discretionary denial brief that the provisional application for the '968 patent “contains 350 pages of specifications showing that the inventors had been developing a memory unit called the Delaware Non-Volatile Memory Host Controller Interface (NVMHCI) before Borchers' April 8, 2010 priority date.” PO Brief, 20. Patent Owner further states that it has “reason to believe that the inventors and other third parties have more documentation, including product specifications, source code, commit logs, emails, and other product-development documentation that supports an earlier invention date and diligence towards a reduction to practice.” PO Brief, 21.

But Patent Owner's “reason to believe” sufficient documentation for establishing conception, reduction to practice, and diligence exists is no reason for discretionary denial. The district court's subpoena powers are available to Patent Owner regardless of whether this IPR is instituted. And Patent Owner has not yet

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asked the court for any subpoenas, or otherwise indicated that it will have sufficient evidence to swear behind Borchers. And as demonstrated by the long list of cases cited by Patent Owner, the PTAB is well experienced in adjudicating this issue should Patent Owner present evidence for antedating Borchers to the merits panel. Accordingly, Patent Owner's speculative plans should not be a reason for discretionary denial.

D. Patent Owner's "settled expectations" argument is inconsistent with the purpose of the AIA.

Patent Owner has no compelling interest or expectation sufficient to avoid PTAB review because they only acquired the '968 patent three years ago and they appear to have done so solely for the purpose of litigation. Patent Owner notes that "the '968 patent issued on October 8, 2013—over eleven years ago." PO Brief, 33. But as a non-practicing entity, Patent Owner cannot claim it has any settled expectations arising from practicing the '968 patent. Patent Owner appears to have acquired the '968 patent in 2022 solely for the purpose of attempting to monetize it through litigation, significantly decreasing any potential relevance of this factor.

Moreover, Patent Owner has not alleged that the Petitioner was aware of the patent, nor have they alleged any meaningful attempt at engaging with Petitioner for licensing discussions. Instead, Patent Owner filed a complaint asserting the '968 patent against Petitioner only seven days after sending a notice letter, which predictably triggered this IPR challenge. Ex.1011, ¶45. The '968 patent is not

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entitled to immunity from IPR review. And regarding expectations of validity, no tribunal has ever adjudicated the validity of the '968 patent after it issued.

Accordingly, the lack of settled expectations weighs against denial.

E. The PTAB has sufficient resources to handle IPR proceedings and ex parte proceedings

The Board's statutorily defined tasks of handling both *ex parte* appeals and post-grant proceedings should not be a reason for discretionary denial. Patent Owner argues that the Board's "limited resources are better spent on the growing backlog of *ex parte* appeals." PO Brief, 30. Patent Owner further notes that the *ex parte* appeal backlog has increased. *See* PO Brief, 30-32. But Patent Owner has ignored the fact that *ex parte* appeals are at historic lows.

And Patent Owner has not provided any evidence to show that the Board cannot handle both its *ex parte* appeal docket and its post-grant proceeding docket. Nor could it, given that the Board has recently publicly acknowledged that "[w]e do have enough staff so we can handle both the appeals and the trials with the judges and staff on board." Ex.1033. Accordingly, the existence of an *ex parte* appeal docket (increasing or not) is not a reason to discretionarily deny this specific case.

F. Compelling economic and national security interests favor institution.

Petitioners Western Digital and Sandisk together play a multifaceted role in

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bolstering the US economy. As a leading provider of digital storage solutions, the companies drive significant revenue generation—with billions in annual sales that not only bolster its own financial health but also support a vast network of suppliers, service providers, and ancillary industries. Ex.1037, 4 (“Western Digital is a leading developer, manufacturer and provider of data storage devices and solutions based on both hard disk drive and NAND flash technologies. With a differentiated innovation engine driving advancements in storage and semiconductor technologies, our broad and ever-expanding portfolio delivers powerful hard disk drives (‘HDD’) and flash-based products (‘Flash’) storage solutions for everyone from students, gamers and home offices, to the largest enterprises and public clouds to capture, preserve, access and transform an ever-increasing diversity of data.”). This economic activity injects substantial funds into local communities through payrolls, tax revenues, and the multiplier effects that come with a robust manufacturing and technology ecosystem.

Moreover, Western Digital’s and Sandisk’s contributions extend to their impact on job creation and workforce development. With operations that span manufacturing, research and development, and engineering, the companies create skilled job opportunities and support local communities by fostering a demand for specialized talent. In doing so, they energize the broader US technology sector—promoting innovation in digital storage technologies that underpin critical

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infrastructure like data centers, cloud computing services, and enterprise IT systems. This technological backbone not only facilitates business operations nationwide but also reinforces American leadership in the rapidly evolving digital age. This type of advanced domestic engineering capacity is critical to U.S. economic interests.

The United States thus has a compelling economic and national security interest in providing Western Digital and Sandisk an opportunity to challenge the '968 patent under the more efficient IPR framework. As leading American technology companies, it is critical that Western Digital and Sandisk have the ability to invest and innovate without being encumbered by invalid patents. Petitioner's right to seek review of such patents by the U.S. Patent and Trademark Office is similarly critical.

It is vital that companies like Western Digital and Sandisk are provided an effective and efficient mechanism for challenging invalid patents asserted against them. Congress created the AIA for this purpose. 77 F. Reg. No. 157, 48612 (Aug. 14, 2012) ("The purpose of the AIA ... is to establish a more efficient and streamlined patent system that will improve patent quality and limit unnecessary and counterproductive litigation costs."); *see also General Plastic Industrial Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 16-17 (Sept. 6, 2017) ("[W]e recognize that an objective of the AIA is to provide an effective and

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efficient alternative to district court litigation.”). AIA proceedings create cost savings for its participants via “reductions in legal fees incurred and the greater probability of a settlement or early-stage resolution.” Ex.1039 (study of AIA economic benefits), 2, 8 (“[T]he total economic benefits of *inter partes* reviews resulting in stay of litigation in district court included **an increase in US business activity of \$1.87 billion in gross product and 8,530 job-years of employment**”; “In situations where an *inter partes* review was conducted parallel to a district court proceeding, the economic benefits of [*inter partes* reviews] include estimated **increases of \$135.4 million in US gross product and 617 person-years of employment**”).

Petitioners Western Digital and Sandisk are seeking review of the ’968 patent consistent with the purpose of AIA post-grant proceedings: an efficient, technically reliable assessment of validity. And Petitioner’s *Sotera* stipulation demonstrates that it desires a true district court alternative. Denying Petitioners access to IPR in this scenario would frustrate the purpose of the AIA and deny Petitioner the specific economic benefits envisioned by Congress.

These economic interests are particularly compelling as Petitioners have been accused of infringement by a non-practicing entity, Polaris. For these reasons, compelling economic and national security interests favor institution.

IV. The new Interim Process should not govern the decision to institute.

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Petitioner respectfully requests that the USPTO Director maintain the standards for institution that were in place when this Petition was filed. While the briefing above addresses the new Interim Process as best understood by Petitioner, this IPR should be governed by the procedures that were in place when it was filed, as in the June 21, 2022 Interim Procedure for Discretionary Denials issued by the Office (the "June 2022 Procedures").

Since the Petition was filed, the USPTO rescinded the June 2022 Procedures through a short posting on the USPTO website. The Office then followed up with the March 24, 2025 Memorandum of Chief Administrative Patent Judge Scott Boalick (the "Boalick Memo"). Two days later, on March 26, Acting Director Stewart issued a Memorandum (the "Director Memo") introducing an entirely new "interim procedure" that bifurcates institution between "(i) discretionary considerations and (ii) merits and other non-discretionary statutory considerations." Director Memo, 1. Three weeks after the Director Memo issued (and after approximately forty patent owners had filed briefs requesting discretionary denial), the USPTO held an oral webcast setting forth additional substantive details of the new interim procedure not found in the Director Memo. Then, eight days after the webcast, the USPTO posted on its website "FAQs for Interim Processes for PTAB Workload Management" with even more substantive details. The recission notice, the Boalick Memo, the Director Memo, the oral

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webcast, and the FAQs (together, the “Announcements”) fall short of satisfying the requisite statutory and constitutional obligations of the USPTO.

The Announcements make sweeping changes to PTAB procedures without going through notice-and-comment rulemaking. This is made more problematic given that the Office has represented to the public that they intend to make any further changes to the institution process through notice-and-comment rulemaking. See 88 Fed. Reg. 24,503 (April 21, 2023). The Announcements violate the notice-and-comment requirements under the APA and are arbitrary and capricious.

Moreover, the additional discretionary denial considerations proposed in the director memo are so broad and vague that they fail to set “forth the standards for the showing of sufficient grounds to institute review.” 35 U.S.C. § 316(a). For example, it is unclear as to how the director will consider “[s]ettled expectations,” “reliance on expert testimony,” “workload,” and “[c]ompelling economic, public health, or national security interests.”

The Director's justification for these announcements similarly falls short of statutory and constitution obligations. The Supreme Court has held that an agency's change in position must be accompanied by sufficient reasons for doing so. See *Food & Drug Admin. v. Wages & White Lion Invs., L.L.C.*, 145 S. Ct. 898, 906 (2025) (explaining that when an agency changes position, it must “offer ‘good reasons for the new policy’”); see also *F.C.C. v. Fox Television Stations, Inc.*, 556

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U.S. 502 (2009) (agency changing position must show “that the new policy is permissible under the statute, that there are good reasons for it, and that the agency believes it to be better, which the conscious change of course adequately indicates”).

The agency's purported justifications of “efficiency” and “workload management” do not hold up under scrutiny. Providing additional discretionary denial factors increases the Office's workload by investing their time in consideration of more issues other than the validity of the patents challenged in IPR. This additional workload becomes more problematic given that the Office appears to be voluntarily *reducing* the number of judges. Ex.1034 (Law 360 article). The Office cannot claim they are resource constrained and at the same time reducing the number of PTAB judges.

Applying the Announcements retroactively to petitions filed prior to issuance of the new policies unduly prejudices petitioners. Petitioner has based their district court and PTAB proceeding based on previously-in-place procedures in order to best seek review of the patents Petitioner believes to be invalid. In light of these and other deficiencies in the Announcements, Petitioner respectfully requests that the Board and Director consider whether to institute based on the standards articulated in the June 2022 Procedures until such time as the Board issues new regulations in accordance with 35 U.S.C. § 316 and the rulemaking

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procedures of the APA.

V. Denial under 325(d) would be inappropriate

While the Borchers reference was cited in an IDS, it was never given any attention by the Examiner. Patent Owner argues that Borchers' inclusion in an IDS "should itself satisfy the first part of the *Advanced Bionics* framework." PO Brief, 41. But Petitioner has already acknowledged that Borchers meets the first prong of the *Advanced Bionics* framework. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 at 7-8 (Feb. 13, 2020) (precedential).

The Petition instead argued that the Examiner "erred in a manner material to the patentability of challenged claims" under the second prong of the *Advanced Bionics* framework. In particular, the Petition explains that with respect to *Becton Dickinson* factors (c), (e), and (f), the Examiner erred by overlooking Borchers' teaching with respect to interrupt coalescing. While Borchers does not refer to certain items as a "doorbell update status," a POSITA would have recognized that Borchers' response head update is a "doorbell update" status as evidenced by at least the background knowledge of a POSITA evidenced in the PCI standards. Petition, 90. The Petition presents the PCI standards as additional evidence, along with Dr. Min's testimony, to show that Borchers teaches what is claimed. Petition, 90.

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By addressing *Becton Dickinson* factors (c), (e), and (f), the Petition's

325(d) analysis is consistent with the Board's recently designated precedential decision in *Ecto World LLC v. Rai Strategic Holdings, Inc.* IPR2024-01280 (May 19, 2025) (precedential). In short, neither Borchers nor any reference like Borchers was cited in a rejection. Nothing in the prosecution record shows the Examiner appreciated Borchers' teachings, particularly with the relevant perspective of a POSITA as evidenced by at least the PCI standards. And for the reasons explained in the Petition, Borchers presents a compelling case that the claimed interrupt coalescing concepts recited in the '968 patent were already known.

Patent Owner has failed to refute Petitioner's arguments on how the Office materially erred. Patent Owner argues that "[t]he relevant portions of the PCI standards that are cited in the petition are closely related and substantially similar to the NVMe specifications the Office considered during prosecution." PO Brief, 41. But similarities between the PCI standards (from Petition) and the NVMe standards (in prosecution) relate to prong one—not prong two. In other words, showing similarities does not address the Petition's explanation as to how the Office materially erred with respect to patentability.

Again, the PCI standards provide evidence of how a POSITA would have understood Borchers' disclosure of a response head update as a doorbell status update. Petition, 77. There is no evidence from the prosecution history that the

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Examiner appreciated Borchers' disclosure. And the Examiner's vague statements that the NVME standards do "not show the details of the steps performed by the memory controller as claimed" do not indicate that the Examiner considered the NVME teachings with respect to Borchers' response head update. Ex.1003, 157; PO Brief, 41.

Further, Patent Owner's reliance on the Examiner's review of the NVME standards is inconsistent with their position on the priority date. The Examiner looked at the NVME documents because he believed that the '968 patent was not entitled to its claimed priority date. Ex.1002, 116; Ex.1003, 30. The NVME standard that Patent Owner cites to (Ex.2019) was published on March 11, 2011. And while this predates the actual filing date of the '968 patent, it does not predate the provisional application date of August 16, 2021. See Ex.1001. Thus, Patent Owner's reliance conflicts with their stated intentions of seeking to antedate the Borchers reference.

VI. Conclusion

For the above reasons, Petitioner respectfully requests that the Director refrain from exercising her discretion to deny this petition, and instead pass it to a merits panel for consideration

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Respectfully submitted,

Date: June 24, 2025

/David M. O'Dell/

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PETITIONER'S EXHIBIT LIST

Ex.1001	U.S. Patent No. 8,554,968 to Onufryk et al.
Ex.1002	Prosecution History of U.S. 8,554,968
Ex.1003	Declaration of Paul Min under 37 C.F.R. § 1.68
Ex.1004	Curriculum Vitae of Paul Min
Ex.1005	U.S. Patent Publication No. 2010/0262979 to Borchers et al. ("Borchers")
Ex.1006	PCI Local Bus Specification 3.0 (February 3, 2004) ("PCI")
Ex.1007	PCI Express 2.0 Base Specification Revision 0.9 (September 11, 2006), ("PCIe")
Ex.1008	U.S. Patent Publication No. 2011/0197003 to Serebrin et al. ("Serebrin")
Ex.1009	U.S. Provisional Patent No. 61/301,937, ("Serebrin Provisional"), Ex.1009
Ex.1010	Excerpts from the IEEE Dictionary
Ex.1011	Complaint, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)
Ex.1012	District Court Trial Statistics
Ex.1013	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, June 22, 2022
Ex.1014	Internet Archive – PCI Express
Ex.1015	Internet Archive – PCI
Ex.1016	U.S. Patent Publication No. 2007/0245061
Ex.1017	U.S. Patent No. 7,924,914
Ex.1018	U.S. Patent Publication No. 2010/0185719

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Ex.1019 (New)	Notice of Sotera Stipulations, Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al. 2:24-cv-02864 (C.D. CA)
Ex.1020	Reserved.
Ex.1021 (New)	FAQs for Interim Processes for PTAB Workload Management, available at https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management (retrieved May 13, 2025).
Ex.1022 (New)	’968 Patent Assignment Recordation
Ex.1023 (New)	Plaintiff’s Disclosure of Asserted Claims and Infringement Contentions, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA) (Served October 2, 2024)
Ex.1024-1031	Reserved
Ex.1032 (New)	Order Granting Defendants’ Motion to Stay, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA) (issued June 23, 2025)
Ex.1033 (New)	“Chief Patent Board Judge Waves Off Workforce Attrition Concerns,” Bloomberg Law, May 7, 2025.
Ex.1034 (New)	“PTAB Judges Told To Get Ready For Layoffs,” Law 360 (March 21, 2025). https://www.law360.com/articles/2314328/ptab-judges-told-to-get-ready-for-layoffs
Ex.1035 (New)	Invalidity Contention Cover Pleading, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)
Ex.1036	Reserved
Ex.1037 (New)	Western Digital Investor Report
Ex.1038 (New)	Judge Wright Markman Orders
Ex.1039 (New)	“An Assessment of the Impact of the Inter Partes Review Process under the Patent Trial and Appeal Board on the US Economy,” The Perryman Group, available at

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	https://www.perrymangroup.com/publications/report/2021/9/23/an-assessment-of-the-potential-impact-of-expanding-inter-partes-review-ipr-under-the-america-invents-act-on-the-us-economy/

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IPR2025-00517 (U.S. Patent 8,554,968)

CERTIFICATE OF SERVICE

The undersigned certifies, under 37 C.F.R. § 42.6, that service was made on the Patent Owner as detailed below.

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Documents served **Petitioner's Opposition to Patent Owner's Request for Discretionary Denial; Exhibits Ex.1019, Ex.1021-Ex.1023, Ex.1032-Ex.1035 and Ex.1037-1039.**

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SANDISK TECHNOLOGIES, INC. AND
WESTERN DIGITAL TECHNOLOGIES, INC.,
Petitioner

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner

Case IPR2025-00517
U.S. Patent No. 8,554,968

**PATENT OWNER POLARIS POWERLED TECHNOLOGIES, LLC'S
REPLY BRIEF ON DISCRETIONARY DENIAL**

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Case IPR2025-00517
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I. INTRODUCTION

The Director should exercise discretion to deny institution. Settled expectations strongly favor denial for three reasons. First, the '968 patent issued over *eleven years* ago, and Polaris has owned it since April 2021. Second, Petitioners waited until Polaris relied on its property right before filing a challenge. And third, the technology was implemented in a commercial product and the patent has been licensed. The *Fintiv* factors also continue to favor discretionary denial. The district court is a better forum to resolve the parties' dispute.

II. POLARIS HAS SETTLED EXPECTATIONS TO ITS PROPERTY RIGHT IN THE '968 PATENT.

Petitioners' arguments on settled expectations miss the point—settled expectations are *not* based on when a patent was acquired. *Contra* Opp., 20-21. Rather, this factor is concerned with “the length of time the claims have been in force.” Interim Process Memo, 2. Indeed, “the longer the patent has been in force, the more settled expectations should be.” *Dabico Airport Solutions v. AXA Power Aps*, IPR2025-00408, Paper 21 at 3 (P.T.A.B. June 18, 2025).

The '968 patent has been in force since October 8, 2013—well over eleven years ago. And Western Digital was aware of it, having cited it in *ten* of its own applications. *See, e.g.*, EX2017.¹ Indeed, the patent has been publicly available and

¹ The '968 patent was also cited during the prosecution of U.S. Patent Nos.

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Petitioners could have easily located it from the time it issued. *See Dabico* at 3. Further, the patent was implemented in a commercial product (*see e.g.*, EX2015) and the patent has been licensed. *Cf. Intel v. Proxense*, IPR2025-00327, Paper 12 (P.T.A.B. June 26, 2025). Petitioners' failure to file an early challenge and decision to wait until Polaris asserted its property right by filing a complaint strongly favors denying institution. *See iRhythm Techs. v. Welch Allyn*, IPR2025-00363, Paper 10 (P.T.A.B. June 6, 2025) (denying institution based on settled expectations where Petitioner was aware of patent as early as 2013); *Dabico* (institution denied based on settled expectations; patent in force about eight years).

Additionally, Polaris has settled expectations in the two other patents involved in the district court proceeding and challenged in related IPR2025-00515 and -00516. In the -515 IPR, the challenged '085 patent has been in force since November 10, 2015, and SanDisk was aware of that patent, having cited it in two of its applications. *See, e.g.*, -515 IPR, EX2015.² And in the -516 IPR, the challenged patent has been in force since December 3, 2013. All three proceedings

10,452,278; 10,466,903; 10,509,569; 10,719,267; 10,725,835; 10,817,182; 11,169,704; 11,487,434; and 11,635,898. In the '835 patent, the Examiner identified the '938 patent as "pertinent art" in an June 26, 2018 Office Action.

² The '085 patent was also cited during the prosecution of U.S. 9,411,669.

warrant denial based on settled expectations.

III. THE *FINTIV* FACTORS FAVOR DENIAL.

Fintiv makes clear that the factors are evaluated holistically in view of “whether efficiency and integrity of the system are best served by denying or instituting review.” *Fintiv* at 6. Here, the factors favor denial.

The district court’s issuance of a stay should not be weighed strongly against denial here. The parties have an obligation to notify the court “after the PTAB issues **any** rulings” as to the pending IPR within seven days. EX1032, 9. Because the district court has indicated that the stay will be lifted soon after a denial of institution decision, factor 1 weighs, at most, slightly against denial.³

The expected date of the discretionary decision in this IPR is July 27, 2025. If institution is denied, the district court has indicated the stay will be lifted soon after denial by ordering the parties to apprise the court within seven days of

³ To the extent *Snap v. SRK Tech.*, IPR2020-00820, Paper 15 (P.T.A.B. Oct. 21, 2020) (precedential) dictates that a stay must always be weighed “strongly against” denial—making a “stay” an outcome determinative factor—Polaris requests the Director clarify or reconsider its designation. Weighing one factor as a “super factor” has no place in the balanced assessment of the relevant circumstances of a case. *Cf. Fintiv* at 5.

developments that warrant lifting the stay. *See* EX1032, 9. And prior to the stay, the case was moving faster than initially scheduled (*see* DD. Br., 3-5), making it likely the litigation will resume quickly.

The original trial date was set for June 16, 2026—over 2 months before the FWD. Because it is highly likely the stay will be lifted immediately upon denial, the trial is still likely to occur before, or around, the FWD date of August 27, 2026. In fact, given the accelerated pace of the litigation prior to the stay, the original trial date could even remain in place. Thus, factor 2 weighs in favor of denial.

Factors 3-6 strongly favor denial for the reasons discussed in Polaris’s initial brief. *See* DD. Br., 8-18. Although the district court noted there is more work ahead, that does not negate the substantial investment before the stay—including exchanging claim constructions and related expert reports. And Petitioners have no reasonable excuse here for waiting seven months to file the Petition.

Further, the *Sotera* stipulation should not be considered as Petitioners provide no reason it could not have been submitted earlier (e.g., with the Petition), but instead fault Polaris for filing its brief by the original deadline. *See* Opp., 6-7. And the *Sotera* stipulation does not mitigate concerns of duplicate effort, because Western Digital relies on system art in its invalidity contentions. *See* Opp., 7 (quoting *Ingenico* to signal it may assert invalidity based on systems). Thus, even if this IPR is instituted, the district court will still have substantial overlap.

Additionally, under factor six, the merits remain weak. Despite having Polaris's POPR in hand (which Polaris continues to request the Director consider), Petitioners give short shrift to those arguments and do not even attempt to address most of the weaknesses. *See* Opp., 12-13. Specifically, Petitioners address only the “interrupt processor” argument in Section III.A.2 of the POPR, but not the arguments in Sections III.A.1, III.B and III.C. *Compare* Opp., 13 with POPR, 21-34. Further, the district court remains a better forum for adjudicating the priority issues (*see* DD. Br. 19-24)—and even more so with the stay in place because the district court's subpoena power is not available to the Board (*contra* Opp. 18).

Considered as a whole, the *Fintiv* factors weigh in favor of denial. Five factors strongly favor, or favor, denial; and only one factor slightly weighs against denial. Instituting this IPR would result in duplicative effort and cause additional cost to litigate in two forums. Accordingly, the Director should exercise discretion to deny institution in view of the parallel litigation.

IV. CONCLUSION

Polaris has strong settled expectations that its property right to the claims of the '968 patent—which have been in force for well over eleven years—are enforceable. And because the *Fintiv* factors favor denial, institution of this IPR would be duplicative and an inefficient use of the Board's limited resources. Thus, this proceeding, and the related IPRs, should not be instituted.

Case IPR2025-00517
U.S. Patent No. 8,554,968

Respectfully submitted,

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Case IPR2025-00517
U.S. Patent No. 8,554,968

CERTIFICATE OF SERVICE (37 C.F.R. § 42.6(e))

I certify that the above-captioned **PATENT OWNER'S REPLY BRIEF**
ON DISCRETIONARY DENIAL was served in its entirety on June 30, 2025,
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UNITED STATES PATENT AND TRADEMARK OFFICE

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Petitioner,

v.

POLARIS POWERLED TECHNOLOGIES, LLC,
Patent Owner.

IPR2025-00517
U.S. Patent No. 8,554,968

**PETITIONER'S SUR-REPLY BRIEF ON DISCRETIONARY
DENIAL**

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00517 (U.S. Patent 8,554,968)

I. Introduction.

The Director should *not* exercise discretion to deny. Patent Owner has *no* settled expectations because (i) **Patent Owner acquired the '968 patent in August 2022¹** solely for the purpose of litigation—which changes everything with respect to settled expectations; (ii) there is no actual evidence of commercialization, marking, or licensing of the '968 patent, let alone any such activities before the filing of the IPR petition; (ii) the '968 patent had *not* been asserted for over 10 years after its issuance, and the IPR petition was filed within 1 year from its *first* assertion in 2024. Further, the District Court in the parallel litigation has found that “[t]his case is still in early stages of litigation,” and stayed the case because of the benefits of PTAB review for the litigation. Ex.1032, 4, 5-6.

II. Polaris has no settled expectations.

Polaris repeatedly asserts that “the patent has been licensed.” PO Reply, 1-2. However, Polaris failed to provide any supporting evidence of such a license,

¹ Patent Owner asserts that it “has owned it since April 2021” without any supporting evidence. PO Reply, 1. However, the public assignment record indicates the transfer to Polaris in August of 2022. Ex.1022, 1. Either way, the IPR petition was filed within 3-4 years from Patent Owner’s acquisition of the '968 patent, and within 1 year from the first assertion of the '968 patent.

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00517 (U.S. Patent 8,554,968)

especially **when** the patent was licensed. There is no public information of recordation of such licenses. There is, however, public information about a lawsuit over these patents between Polaris and Micron² that was filed after the present IPRs were filed, but has since settled. If this is the only license being referenced, it would actually weigh **against** discretionary denial, because it happened **after** the filing of the IPR petition. As the Director stated in *Intel-Proxense*:

[P]ersuasive reasons why the Board should review challenged claims several years after their issue date [include as] example, a patent may have been in force for years but may not have been commercialized, asserted, marked, licensed, or otherwise applied in a petitioner's particular technology space, if at all.

IPR2025-00327, Paper 12, 2-3 (P.T.A.B. June 26, 2025).

This example of persuasive reasons applies to the present case, because there is no evidence of commercialization, licensing, and marking at all, much less any such activities **before** the filing of the present IPR petitions. Patent Owner references the '968 patent's provisional application as evidence of commercialization. PO Reply, 2. However, PO fails to provide any details about

² *Micron Tech. Inc et al. v. Polaris PowerLED Techs., LLC*, No. 1-25-cv-00073 (D. Idaho), filed February 7, 2025 and voluntarily dismissed April 4, 2025.

Petitioner's Sur-Reply Brief on Discretionary Denial
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any specific commercial product, such as what the product is, when it was introduced in the market, or how the invention is used in the product. Further, the first assertion of the '968 patent was over 10 years after its issuance, after Polaris acquired it in 2022, and the IPR petition was filed within 1 year from the **first** assertion in 2024.

Additionally, Polaris argues that because Petitioner cited the '968 patent in its own applications, they should have considered challenging it earlier. PO Reply, 1-2. What Polaris does not point out is that Western Digital and Sandisk combined have had over 10,000 U.S. patent issue since 2010. If on average each of these patents have 25 prior art patent citations, that would be over 250,000 citations. Filing IPRs for even 1/100 of these would be untenable, and in the present case, should have no bearing on settled expectations. In fact, and contrary to Polaris' assertion, it would have been an inefficient use of the PTAB's resources to challenge these patents back then, because there was no active litigation. *Google et al. v. Mullen*, IPR2025-00227, Paper 13, 4 ("it is an inefficient use of Board resources to review [a] patent that has been dismissed from the litigation.").

Finally, Polaris's comparison of the already-vacated previously scheduled trial date and a FWD date "upon denial" is non-sensical, because there would be no projected FWD date with denial. PO Reply, 4.

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00517 (U.S. Patent 8,554,968)

Respectfully submitted,

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Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00517 (U.S. Patent 8,554,968)

PETITIONER'S EXHIBIT LIST

Ex.1001	U.S. Patent No. 8,554,968 to Onufryk et al.
Ex.1002	Prosecution History of U.S. 8,554,968
Ex.1003	Declaration of Paul Min under 37 C.F.R. § 1.68
Ex.1004	Curriculum Vitae of Paul Min
Ex.1005	U.S. Patent Publication No. 2010/0262979 to Borchers et al. ("Borchers")
Ex.1006	PCI Local Bus Specification 3.0 (February 3, 2004) ("PCI")
Ex.1007	PCI Express 2.0 Base Specification Revision 0.9 (September 11, 2006), ("PCIe")
Ex.1008	U.S. Patent Publication No. 2011/0197003 to Serebrin et al. ("Serebrin")
Ex.1009	U.S. Provisional Patent No. 61/301,937, ("Serebrin Provisional"), Ex.1009
Ex.1010	Excerpts from the IEEE Dictionary
Ex.1011	Complaint, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)
Ex.1012	District Court Trial Statistics
Ex.1013	Director Vidal Memorandum re: Interim Procedure for Discretionary Denials in AIA Post-Grant Proceedings with Parallel District Court Litigation, June 22, 2022
Ex.1014	Internet Archive – PCI Express
Ex.1015	Internet Archive – PCI

Petitioner's Sur-Reply Brief on Discretionary Denial
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Ex.1016	U.S. Patent Publication No. 2007/0245061
Ex.1017	U.S. Patent No. 7,924,914
Ex.1018	U.S. Patent Publication No. 2010/0185719
Ex.1019	Notice of Sotera Stipulations, Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al. 2:24-cv-02864 (C.D. CA)
Ex.1020	Reserved.
Ex.1021	FAQs for Interim Processes for PTAB Workload Management, available at https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management (retrieved May 13, 2025).
Ex.1022	'968 Patent Assignment Recordation
Ex.1023	Plaintiff's Disclosure of Asserted Claims and Infringement Contentions, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA) (Served October 2, 2024)
Ex.1024-1031	Reserved
Ex.1032	Order Granting Defendants' Motion to Stay, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA) (issued June 23, 2025)
Ex.1033	"Chief Patent Board Judge Waves Off Workforce Attrition Concerns," Bloomberg Law, May 7, 2025.
Ex.1034	"PTAB Judges Told To Get Ready For Layoffs," Law 360 (March 21, 2025). https://www.law360.com/articles/2314328/ptab-judges-told-to-get-ready-for-layoffs
Ex.1035	Invalidity Contention Cover Pleading, <i>Polaris PowerLED Technologies, LLC v. Western Digital Corporation et al.</i> 2:24-cv-02864 (C.D. CA)

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00517 (U.S. Patent 8,554,968)

Ex.1036	Reserved
Ex.1037	Western Digital Investor Report
Ex.1038	Judge Wright Markman Orders
Ex.1039	“An Assessment of the Impact of the Inter Partes Review Process under the Patent Trial and Appeal Board on the US Economy,” The Perryman Group, available at https://www.perrymangroup.com/publications/report/2021/9/23/an-assessment-of-the-potential-impact-of-expanding-inter-partes-review-ipr-under-the-america-invents-act-on-the-us-economy/

Petitioner's Sur-Reply Brief on Discretionary Denial
IPR2025-00517 (U.S. Patent 8,554,968)

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Stewart Says New Patent Policies Aim To Bring Stability

By **Ryan Davis**

Law360, San Diego (September 8, 2025, 12:33 AM EDT) -- Acting U.S. Patent and Trademark Office Director Coke Morgan Stewart said Sunday that new patent review policies the office has implemented are aimed at making the patent system more stable, saying that in her view, repeated patent challenges can result in "the antithesis of stability."

In a keynote address at the Intellectual Property Owners Association annual meeting in San Diego, Stewart explained why she believed previous policies on Patent Trial and Appeal Board reviews had left patent owners "so incredibly frustrated" and how the changes she has put in place since taking office in January, many of which restrict patent challenges, are designed to be an improvement.

The acting director said in her talk, which she described as "a bit of a State of the Union, but for the USPTO," that there have been disruptions to the patent system since the 2011 America Invents Act created the ability to challenge patents in fast-moving proceedings at the PTAB, which uses a lower burden of proof than district court.

"To have a stable economy, we need a stable patent system," Stewart said. "Repeated and expedited reconsideration of patent grants under the low preponderance of evidence standard is the antithesis of stability."

Under previous USPTO policies, many patents were frequently invalidated by the PTAB, and Stewart said "you can thus see why patent owners are so incredibly frustrated by the process that they must undertake simply to maintain the patent that the U.S. government issued to them at great time and expense."

Stewart asked the audience to imagine if their law, business or driver's license, or their college degree or the title to their home, "were constantly subjected to reconsideration by anyone at any time year after year after year, and that you had no presumption that the original decision was correct and no window of time that closes to stop these challenges."

"It's hard to think of a single example in all of government where such a system exists," she said. "And such a system is completely contrary to the exclusive right granted to patent owners in the Constitution, the presumption of validity granted by Congress, and the Article III court protections afforded to patent owners prior to the AIA."

"I hope most of you agree that the only way such a review scheme is workable is because Congress granted the director discretion at the institution stage to determine when to institute these reviews," she said.

Policy Overhaul

Throughout this year, Stewart has implemented **new policies** using the discretion granted to the USPTO director in the AIA that have resulted in numerous discretionary denials of petitions challenging patents.

She now issues most decisions on discretionary considerations herself and said Sunday that 425 decisions have been issued to date. They have cited an array of reasons why review is not warranted, including the status of related district court litigation and the **"settled expectations"** of patent

9/10/25, 1:23 PM

Stewart Says New Patent Policies Aim To Bring Stability - Law360

owners, based on how long ago the patent was issued.

"The office has focused on liberally permitting early challenges to patent validity, particularly [post-grant reviews]," Stewart said in her speech, referring to a type of proceeding that must be filed within nine months of when a patent is issued.

"Early challenges ensure that patents are more stable, thereby increasing investment, commercialization and job growth," she said. "On the other hand, the longer a patent has been in force, the stronger and more settled the patent owner's expectations should be."

She added that settled expectations have often been cited in denials when a patent was issued over six years ago, but "it does not mean that a patent owner cannot establish strong settled expectations on a younger patent. We invite patent owners to continue to make their case for settled expectations, as well as to present other reasons why PTAB review is not appropriate in their case."

That can include scenarios where a district court case will be decided before the PTAB's decision is due or where the patent owner has already fended off prior challenges, she said. She pointed to a case last year, where the board instituted review when there had been seven prior challenges to the patent, including one pending before the PTAB at the time of the decision.

For those challenging patents, Stewart recommended that they provide clear reasons for why review should be instituted, such as when the office made a "material error in examination, such as making inconsistent fact findings across related patents."

"We should use our administrative reviews to correct errors, as the AIA intended," she said.

Other situations that may warrant review include when a district court trial is scheduled long after the board's decision would be due, Stewart said, as well as when there has been "a change in law that disrupts settled expectations of the patent grant," and when the patent owner asserts numerous unrelated patents in one infringement case or is "unexpectedly shifting its invention into new areas of technology."

She issued **several decisions** over the past week involving some of those scenarios.

Patent Quality And Statistics

The acting director said the office will soon publish a study that she said will show that "patents being challenged at the PTAB are not the so-called low quality or bad patents that motivated the creation of the AIA," since "those patents seldom make it past a demand letter, a motion to dismiss, a motion for summary judgment or a nuisance value settlement."

Stewart added that "we cannot be lulled into a false sense of patent quality or lack of quality" based on statistics about how often the PTAB finds patents invalid, or how often those decisions are affirmed by the Federal Circuit. A large majority of PTAB final decisions have historically found most or all of the challenged claims invalid, and the board's finding are usually upheld on appeal.

Stewart said if 100 patent examiners or judges all looked at the same patent claim and most of them think it should be upheld, "it's only a matter of simple math that if you challenge the same claim over and over again, you will increase the odds that it will be determined to be unpatentable, even if a majority of examiners and judges think it is patentable."

A study found that in 2023, the Federal Circuit upheld the board's decisions **over 83% of the time**. Stewart noted that, absent an error of law, the appeals court only looks at whether the PTAB's decisions are reasonable and based on substantial evidence.

"So, if you take this logic to an extreme, it is theoretically possible that most of the decisions of PTAB on patentability are wrong, but not unreasonable, and therefore affirmed by the Federal Circuit," Stewart said.

Possible New Patent Fees

9/10/25, 1:23 PM

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Stewart, who is the USPTO deputy director but is running the office while director nominee John Squires awaits a Senate **confirmation vote**, also discussed **recent reports** that Commerce Secretary Howard Lutnick is considering a new patent fee structure based on the value of patents. She said she would leave it to him to provide more details.

Stewart noted, though, that Lutnick is an inventor on about 400 patents, so he "knows the value of strong patent rights" and also "knows that a modernized fee system can be used to add to the capacity of the USPTO," to make operations more efficient, add new technology, reduce the patent application backlog and increase patent quality.

There are multiple steps to implementing new patent fees, including public hearings and opportunities for comment, the acting director said, "so, I encourage you to think deeply and creatively about what kind of fee structure is best with the intellectual property system and best for the country, and engage in that discussion."

Stewart noted the office has been making progress in reducing the backlog, which she said went from an all-time high of 838,000 unexamined applications in January to about 800,000 now, and is in the process of hiring 1,100 new patent examiners this year.

She concluded by saying that "the entire team at USPTO knows that it is our responsibility to ensure a robust and stable IP system that fosters job growth and investment. We are committed to doing everything in our power to enhance and safeguard those rights."

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Data Undermines USPTO's 'Settled Expectations' Doctrine

By **Jonathan DeFosse, Samuel Smith and Kenzo Kasai** (August 29, 2025, 6:21 PM EDT)

The acting director of the U.S. Patent and Trademark Office, Coke Morgan Stewart, has issued a series of decisions discretionarily denying institution of inter partes review based, at least in part, on the assertion that IPR is unwarranted because a patent owner develops so-called settled expectations once a patent has been in force for six or more years.

To test the premise of the settled expectations doctrine empirically, we collected data from IPR petitions filed since 2012 to determine the age of patents challenged in those proceedings.

Our research indicates that a substantial volume of IPR proceedings — more than 8,000 petitions, representing more than 46% of IPR petitions filed since 2012 — challenged patents that were in force for six or more years.

Those petitions resulted in cancellation of at least one claim in over 80% of the proceedings that reached final written decisions. This data appears to refute the assertion that patent owners develop a strong settled expectation that their patents will not be challenged or invalidated once the patents are in force for six years.

The Doctrine

On March 26, Stewart **issued** a memorandum to all Patent Trial and Appeal Board judges announcing that decisions on whether to institute inter partes review would be bifurcated into two phases: (1) discretionary considerations; and (2) merits and other nondiscretionary statutory considerations.

In the same memorandum, Stewart listed relevant discretionary considerations, including "[s]ettled expectations of the parties, such as the length of time the claims have been in force."

The memorandum did not provide any precedential basis for the settled expectations doctrine. The memorandum also did not elaborate on the nature of the settled expectations.

For example, it is unclear whether Stewart was referring to a settled expectation in the underlying validity of a patent or, alternatively, a settled expectation that the validity of the patent will not be challenged.

In June and July, Stewart and the acting deputy chief administrative patent judge, Kalyan Deshpande, issued 113 decisions referencing the settled expectations of the patent owners.

On June 18, Stewart stated in *Dabico Airport Solutions Inc. v. AXA Power Aps* that "there is no bright-line rule on when expectations become settled," but, in general, "the longer the patent has been in force, the more settled expectations should be."^[1]

Despite the absence of a bright-line rule, Stewart has consistently found that patent owners



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developed strong settled expectations once their patents have been in force for six years.

Out of 113 discretionary denial decisions, 71 decisions addressed patents that had been in force for six or more years. In 90% of those cases — 64 out of 71 — Stewart discretionarily denied the petitions based, at least in part, on the patent owner's strong settled expectations.

She appears to have derived the de facto six-year period for developing strong settled expectations by way of analogy to the six-year statutory damages period.[2]

The de facto presumption of settled expectations after six years has been overcome in a few cases. Those cases offer several reasons why a patent owner may not have settled expectations.

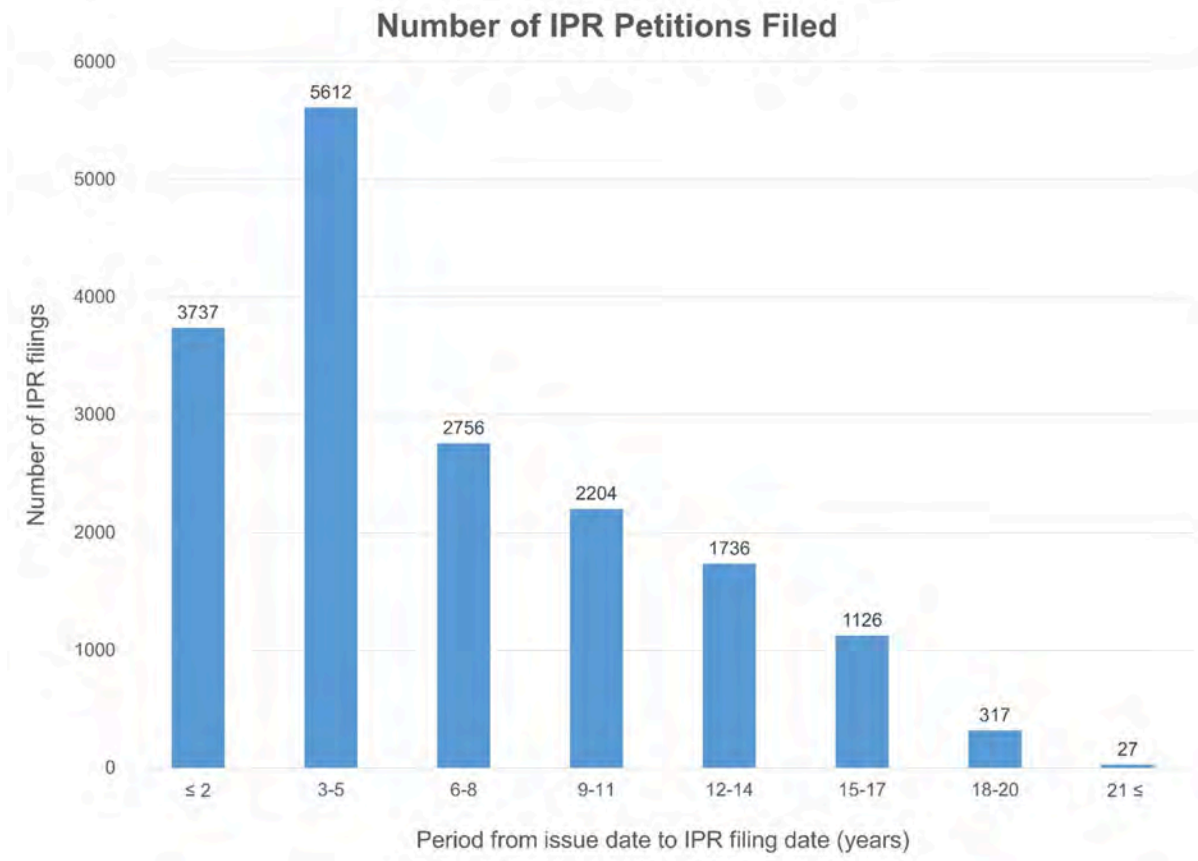
- In *Embody Inc. v. Lifenet Health*, decided June 26, the patent is part of a family and there is a related patent that is less than 6 years old.[3]
- In *Globus Medical Inc. v. Spinelogik Inc.*, decided June 12, the patent expired for nonpayment of maintenance fees.[4]
- In *Eusung Global Corp. v. Hydrafacial LLC*, decided July 10, the patent was issued after a material error during examination.[5]
- In *Shenzhen Tuozhu Technology Co. Ltd. v. Stratasys Inc.*, decided July 17, the patent owner did not invest in or seek to commercialize the patent.[6]

Empirical Analysis

To provide an empirical analysis for Stewart's reliance on a patent owner's strong settled expectations, we used Lex Machina to collect data from IPR petitions filed since 2012 to see whether those proceedings provide evidence of the settled expectations of patent owners.

Data collected from IPR proceedings indicates that it would have been unreasonable for patent owners to develop an expectation that their patents would not be challenged after six years.

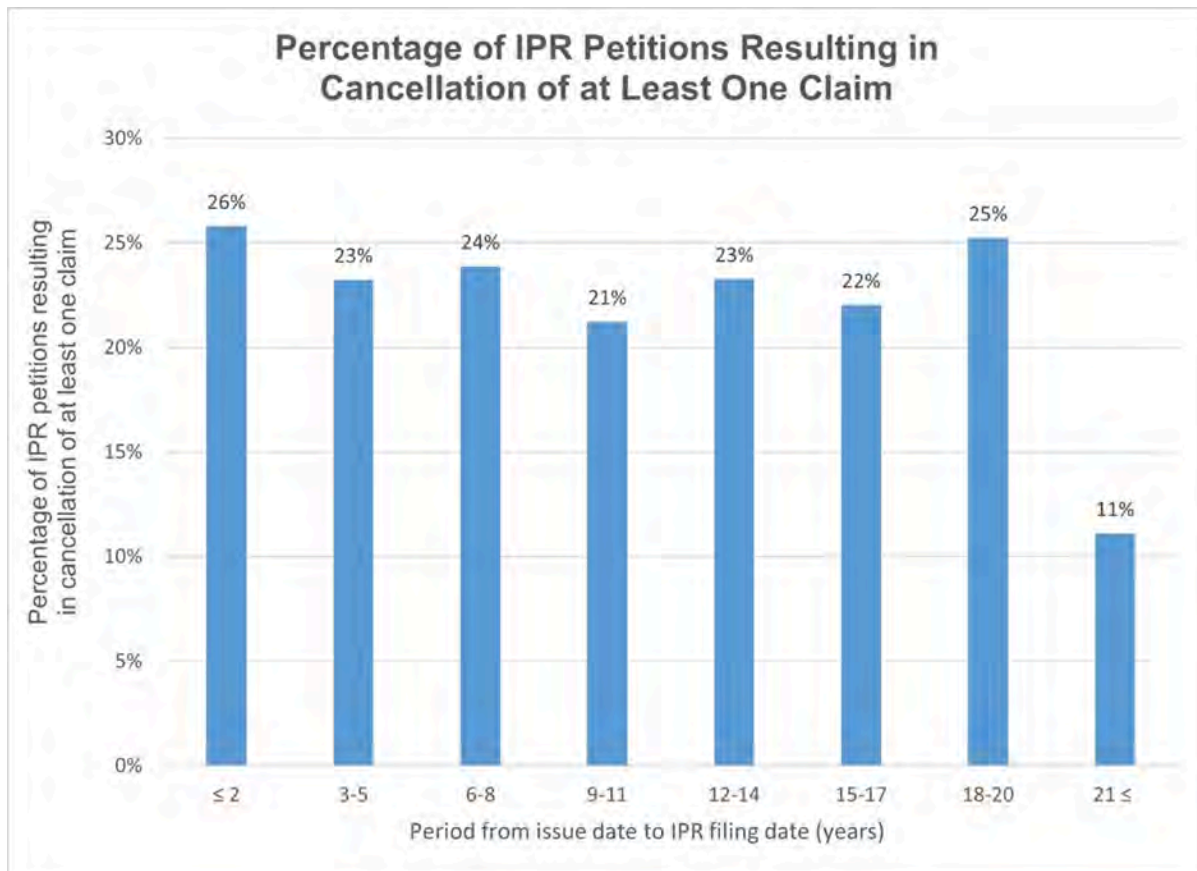
Out of 17,515 IPR petitions filed since 2012, 8,166 of those petitions challenged patents that had been in force for six or more years.[7] The age of the patents challenged is reflected in the following chart.



As reflected above, 46.6% of patents challenged in IPR proceedings since 2012 have been in force for six or more years. Indeed, the average age of patents challenged in IPR proceedings is greater than 6.7 years.

The data also indicates that claims that were in force for more than six years were routinely invalidated. Out of 8,166 petitions challenging patents in force for more than six years, 2,269 petitions reached a final written decision.[8]

Out of the 2,269 final written decisions, 1,861 — or 82% — resulted in cancellation of at least one claim. The percentage of petitions resulting in the cancellation of at least one claim was also steady regardless of the age of the challenged patent, as shown in the following chart.



Thus, based on the history of IPR proceedings, patent owners would not appear to have any reasonable settled expectations either (1) that that patents will not be challenged after six years; or (2) that, if challenged, the claims will be found valid based on "the length of time the claims have been in force."

To the contrary, patent owners could reasonably expect their patents to be challenged, and the claims invalidated regardless of the age of the patents.

Under these circumstances — where the empirical data confirms that, historically, patents of all ages have been challenged and invalidated in IPR proceedings — a patent owner's hypothetical strong settled expectations counsel against discretionarily denying IPR petitions.

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[1] *Dabico Airport Solutions Inc. v. AXA Power Aps* , IPR2025-00408, Paper 21 at 3 (Acting Dir. Stewart June 18, 2025).

[2] See *Dabico*, IPR2025-00408 at 3 ("The approach aligns with other approaches to settled expectations and incentives, for example, for filing infringement lawsuits. Cf. 35 U.S.C. § 286 ('Except as otherwise provided by law, no recovery shall be had for any infringement committed more than six years prior to the filing of the complaint or counterclaim for infringement in the action.')").

[3] See **Embodry, Inc. v. Lifenet Health** , IPR2025-00248, Paper 13 at 3 (Acting Dir. Stewart June 26, 2025).

[4] **Globus Medical, Inc. v. Spinelogik, Inc.** , IPR2025-00225, Paper 8 at 2 (Acting Dir. Stewart June 12, 2025).

[5] See e.g., **Eusung Global Corp. v. Hydrafacial LLC** , IPR2025-00445, Paper 14 at 2 (Acting Dir. Stewart July 10, 2025).

[6] **Shenzen Tuozhu Tech. Co., LTD v. Stratasys Inc.** , IPR2025-00531, Paper 10 at 3 (Acting Dir. Stewart July 17, 2025).

[7] We have collected data for IPRs filed between September 16, 2012 and July 23, 2025.

[8] Additionally, the data indicates that, historically, institution decisions have shown no bias against patents that have been in force for more than six years. Since 2012, 20.1% of petitions challenging patents that had been in force for less than six years were denied institution. In comparison, only 17.9% of petitions challenging patents that had been in force for more than six years were denied institution.

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